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Process Variation and Pelgrom's Law

Welcome to "Circuit Intuitions!" This is the fourth article of a column series that appears regularly in this magazine. As the title suggests, each article provides insights and intuitions into circuit design and analysis. These articles are aimed at undergraduate students but may serve the interests of other readers as well. If you read this article, I would appreciate your comments and feedback, as well as your requests and suggestions for future articles in this series. Please send your e-mails to ali@ece.utoronto.ca.

The past three articles were related to the small-signal operation of MOS circuits. In this article, we step back and look at dc operation of a simple current mirror and how the process variation can affect the accuracy of the currents produced. We review this through a simplified design of a current-based digital to analog converter (also known as IDAC).

Figure 1 shows a simplified diagram of an IDAC that includes a current mirror and ideal switches. The current mirror consists of a reference current, I_{REF}, that feeds into a diode-connected transistor, M_0, and several identical mirroring branches (M_1 to M_N). Under ideal conditions, i.e., when M_0 to M_N are perfectly matched (and have the same V_{DS}), all the branch currents (I_1 to I_N) are equal to the reference current. These currents can then be added selectively based on a thermometer-coded digit (b_1 *to* b_N) to produce the output current:

$$I_{OUT} = \sum_{k=1}^{N} b_k I_{REF} = I_{REF} \sum_{k=1}^{N} b_k,$$

where we assume $b_k \in \{0,1\}$. Accordingly, a "1" contributes fully to the output current whereas a "0" contributes no current to the output. This equation shows that the output current is equal to the reference current scaled by the sum of the thermometer-coded bits.

In this article, we step back and look at dc operation of a simple current mirror and how the process variation can affect the accuracy of the currents produced.

In reality, due to process variation, I_1 to I_N do not match with I_{REF} and with each other. This will cause the output current to deviate from its ideal value. Let us briefly review the process variations that cause mismatch in the currents.

The current of an NMOS transistor in saturation region can be approximated by

$$I_{DS} = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{Tn})^2,$$

where μ_n is the electron mobility, C_{ox} is the gate capacitance per unit area, V_{Tn} is the threshold voltage of the transistor, and W and L are the width and the length of the transistor, respectively. In the above equation, we have assumed a square-law relationship between the drain current and $(V_{GS} - V_{Tn})$, but the arguments we put forward in the rest of this article are also applicable if we assume a linear relationship, which is the case in modern CMOS processes.

This equation clearly indicates that the drain current is a function of three variables: $\mu_n C_{ox}$, V_T, and W/L. If, for example, we assume $\mu_n C_{ox} = 600\,\mu A/V^2$, $V_T = 0.3\,V$, $V_{GS} = 0.5\,V$, and $W/L = 5$, then $I_{DS} = 70\,\mu A$; however, when the chip is fabricated, these variables may turn out to be slightly different than what was originally intended. As a result, two

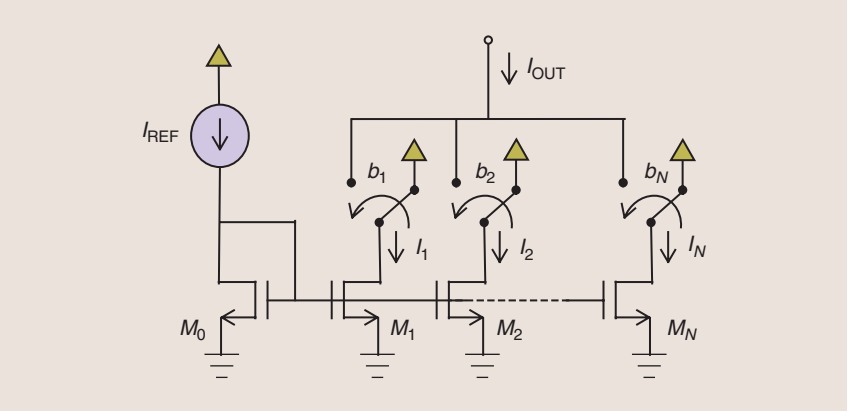

FIGURE 1: A simplified diagram of a current DAC (IDAC).

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adjacent transistors with the same W/L may exhibit, for example, a 5-mV difference in their threshold voltages. This threshold variation, or threshold mismatch, will result in a difference ΔI between the two currents that is 5% of their nominal value. In other words, $\Delta I/I = 0.05$. In general, we treat $\mu_n C_{ox}, V_T$, and W/L as *random* variables. Let us now focus on the effects of V_T variations while we assume the other two variables have no variation.

How could we reduce the variation of V_T so as to reduce the variation in the current without introducing changes to the underlying technology?

It was shown in a seminal paper by Pelgrom et al. in 1989 [1] that, in any given MOS technology, the variance of V_T among adjacent transistors reduces inversely with the gate area. This is known as Pelgrom's law:

$$\sigma^2_{VT} = \frac{A^2_{VT}}{2WL},$$

where A_{VT} is a constant that depends only on the process. Since the threshold mismatch between two adjacent transistors, ΔV_T, is the difference between two random variables, i.e., $\Delta V_T = V_{T1} - V_{T2}$, we can also write Pelgrom's law as follows:

$$\sigma^2_{\Delta VT} = \sigma^2_{VT1} + \sigma^2_{VT2} = \frac{A^2_{VT}}{WL}.$$

Note that this equation holds if we assume V_{T1} and V_{T2} are identical and independent.

We now apply Pelgrom's law to our example. Assume the initial $\sigma_{\Delta VT}$ is 6 mV. If we multiply W by a factor of four while keeping L constant, $\sigma_{\Delta VT}$ will be reduced by a factor of two, implying a tighter distribution (or less variation) among the threshold voltages of adjacent transistors. Let us see if this makes intuitive sense.

Assume a transistor with the gate area of WL has a threshold voltage V_{Tk}, where V_{Tk} is a random variable with an expected value of μ_{VT} and a variance of σ^2_{VT}. As shown in Figure 2, if we put N such transistors in parallel,

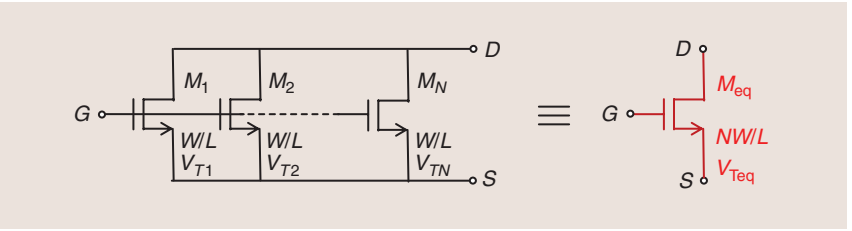

FIGURE 2: An NW/L transistor exhibits a threshold voltage with the same expected value as that of a smaller W/L transistor. The variance of the threshold voltage, however, is N times smaller in the larger transistor.

each with a V_T having the same statistics (i.e., having the same average and variance), we are effectively creating a transistor with NW as its width and L as its length. The threshold voltage of the parallel combination (V_{Teq}) is expected to be the average of the individual threshold voltages. In other words, we can write:

$$V_{Teq} = \frac{1}{N}\sum_{k=1}^{N} V_{Tk}.$$

Pelgrom's law states that the threshold mismatch between two adjacent identically drawn transistors reduces inversely with the gate area.

V_{Teq} is now a new random variable with the following properties:

$$\mu_{VTeq} = \mu_{VT}$$
$$\sigma^2_{VTeq} = \frac{1}{N}\sigma^2_{VT},$$

where we have assumed the V_{Tk}s are independent. This equation simply states that when we average N identical, independent random variables, the variations of the average is lower than the variations of the individual variables.

In the example of the current DAC, we usually begin our design by assuming a fixed power budget and a fixed overdrive voltage ($V_{GS} - V_{Tn}$). This will in turn dictate a fixed current, I_{REF}, and a fixed W/L for the transistors. If it were not for the variation, we could simply choose the minimum L and accordingly find the proper W. However, to reduce the variation among the currents in different branches, we will increase both W and L by the same factor so as to maintain the original W/L (and hence the original overdrive voltage) while reducing the mismatch according to Pelgrom's law. This will of course increase the area and the load capacitance of the IDAC, but that is the price we pay to average out (reduce) the variation among the output currents!

We now return to the other two random variables affecting the current: $\mu_n C_{ox}$ and W/L. Interestingly, Pelgrom's law [1] also applies to these random variables: the variations in these two variables are also reduced by increasing WL in the same way.

In conclusion, Pelgrom's law states that the threshold (or other process-related) mismatch between two adjacent identically drawn transistors reduces inversely with the gate area. While we choose W/L of transistors to achieve a target bandwidth and power, we choose WL to maintain accuracy in the face of process variation and mismatch.

Acknowledgement

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References

[1] M. J. M. Pelgrom, C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits*, vol. 24, no. 5, pp. 1433–1440, Oct. 1989.

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