# A Low-Voltage CMOS Filter for Hearing Aids using Dynamic Gate Biasing

L. Pylarinos, N. W. Wong, and K. Phang
Edward S. Rogers Sr. Department of Electrical and Computer Engineering
University of Toronto

**Abstract - In this paper we discuss the design of a low-voltage (1.5V), continuous-time, biquadratic CMOS filter based on Dynamic Gate Biasing (DGB). We begin by discussing the filter's structure and its tuning mechanism. The filter uses transconductance-C cells and implements low-pass, bandpass and high-pass transfer functions. The transconductances are tuned using the gate voltages of MOSFETs operating in the triode region. We review the principle of DGB, and discuss the design of the charge pump based on the filter's performance and tunability requirements. Circuit details of the filter elements and the charge pump are presented along with SPICE simulation results of the overall filter.**

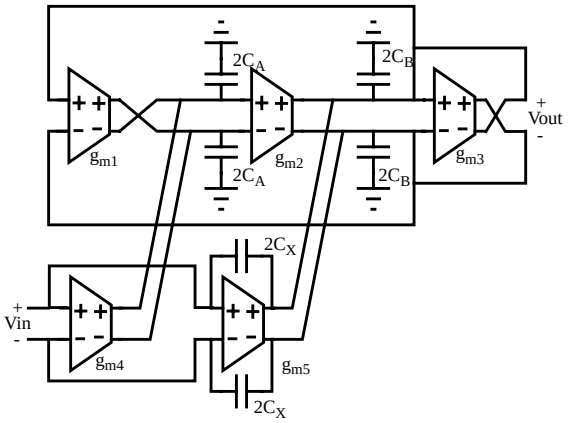


**Fig.1** A fully differential biquadratic filter using $g_m$-C technology.

## I. INTRODUCTION

Programmable filters in modern hearing aids perform a variety of functions including ambient noise rejection, equalization to compensate for particular hearing deficiencies, and the suppression of ringing that can arise from acoustic feedback. Low power dissipation is essential in maximizing battery life. A primary method of reducing power is to reduce the supply voltage. Low voltage operation around 1.5V is particularly attractive because it reduces power consumption and allows operation from a single battery.

In practice, designing filters capable of low-voltage operation is a challenge. In some designs, an on-chip charge pump is used to generate a second supply voltage with which to power the circuits. Unfortunately, low-voltage integrated charge pumps exhibit poor power efficiency[1]. Dynamic gate biasing[2] is an experimental approach to low-voltage analog circuits. In this scheme the charge pumps are not used to power circuits. Instead, they are used to provide a stable bias voltage to the gates of MOSFETs. Since the gates of MOSFETs draw no current, a charge pump used in this manner ideally supplies no power, and so power efficiency is no longer an issue. As such, DGB is a potential approach to developing reduced power filters for hearing aids.

In this paper we discuss the design of a tunable, continuous-time, biquadratic (i.e., second-order) CMOS filter based on DGB. We discuss the filter's structure and means of tuning using MOSFETs dynamically biased in the triode region. We present SPICE simulations of the filter's performance for a 0.35$\mu$m CMOS technology.

## II. FILTER DESIGN

There are many techniques for implementing analog filters in CMOS, such as active-RC, switched-capacitor and transconductance-C ($g_m$-C) structures. Of these techniques, $g_m$-C based filters are often preferred for low-voltage design because of their superior low-distortion performance[3].

A general second-order, fully differential filter using $g_m$-C elements is shown in Fig. 1 [4]. The transconductor cell [5] used by the filter is shown in Fig. 2. The current through $Q_1$ and $Q_2$ is set to a constant value of $I_2$. This results in a dc bias current of $I_1$-$I_2$ through $Q_3$ and $Q_4$ which is consequently mirrored to $Q_5$ and $Q_6$. Since a constant current of $I_2$ is forced through $Q_1$ and $Q_2$, the individual gate-source voltages of these transistors remain fixed. Any differential voltage appearing at the p-channel

CCECE/CCGEI 2001 0-7803-6715-4/01/$10.00 ©2001 IEEE

inputs will also appear as a drain-to-source voltage across triode transistor $Q_7$. A current $i_{o1}$ will flow through $Q_7$ and be mirrored to the drains of $Q_5$ and $Q_6$. For small differential inputs, this current is given by

$$i_{o1} = (V_{i+} - V_{i-}) \cdot g_{m7} \tag{1}$$

where

$$g_{m7} = \mu_n \cdot C_{ox} \cdot \left(\frac{W}{L}\right)_7 \cdot (V_{gs7} - V_{tn}) \tag{2}$$

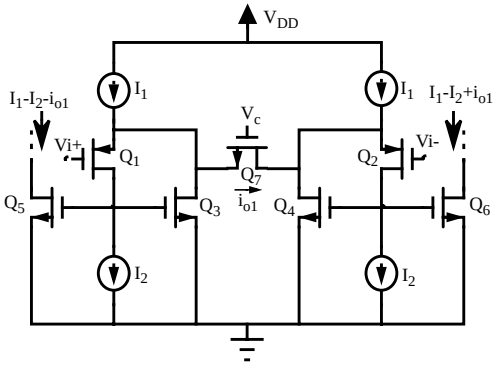


**Fig. 2** A CMOS transconductor cell ($V_{DD}$=1.5V)

The output resistance of this basic transconductance cell can be increased by augmenting the lengths of transistors $Q_5$ and $Q_6$ and operating these devices in their active regions. A large output resistance is necessary in order to realize integrators for the filter structure. Furthermore, these fully-differential $g_m$-C cells are used in a feedback configuration and therefore require common-mode feedback (CMFB) circuitry . For the filter simulations, the CMFB circuit was implemented functionally. A possible circuit implementation based on the use of switched-capacitor circuits is shown in Fig. 3[6][7].

Using Eq.(1) and assuming an infinite output resistance for each $g_m$-C element, the Laplacian transfer function of the filter in Fig.1 is given by

$$H(s) = \frac{s^2\left(\frac{C_X}{C_X + C_B}\right) + s\left(\frac{g_{m5}}{Cx + C_B}\right) + \left(\frac{g_{m2} \cdot g_{m4}}{C_A(C_X + C_B)}\right)}{s^2 + s\left(\frac{g_{m3}}{C_X + C_B}\right) + \left(\frac{g_{m1} \cdot g_{m2}}{C_A(C_X + C_B)}\right)} \tag{3}$$

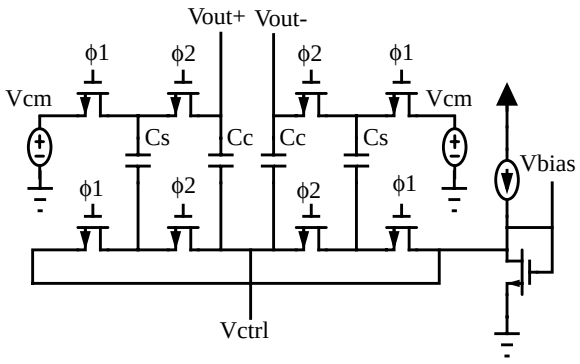


**Fig. 3.** CMFB circuit for biquad filter

This transfer function may be expressed in the standard form

$$H(s) = \frac{a_2 \cdot s^2 + a_1 \cdot s + a_0}{s^2 + s\left(\frac{\omega_0}{Q}\right) + \omega_0^2} \tag{4}$$

In this equation $\omega_0$ is the center frequency and Q is the quality factor which indicates the selectivity of the filter. These are the two basic parameters that describe the performance of a second-order filter. Equating the coefficients in Eq.(3) and Eq.(4) we have

$$\omega_0 = \sqrt{\frac{g_{m1} \cdot g_{m2}}{C_A(C_X + C_B)}} \tag{5}$$

$$Q = \sqrt{\left(\frac{g_{m1} \cdot g_{m2}}{g_{m3}^2}\right)\left(\frac{C_X + C_B}{C_A}\right)} \tag{6}$$

In order to gauge the tuning range of the filter it is helpful to derive the sensitivity of $\omega_0$ and Q from Eq. (5) and Eq.(6). If the variation of a quantity is denoted by the characteristic $\delta$, then the sensitivity of the center frequency, $\omega_0$, is given by a Taylor series expansion with respect to the dependent variables where second-order and higher-order terms are neglected (i.e., $\delta\omega_0 = \frac{\partial\omega_0}{\partial V_{gs1}} \cdot \delta V_{gs1} + \frac{\partial\omega_0}{\partial V_{gs2}} \cdot \delta V_{gs2}$). We have from the preceding equations,

$$\delta\omega_0 = \frac{\omega_0}{2}\left(\frac{\delta V_{gs1}}{V_{eff1}} + \frac{\delta V_{gs2}}{V_{eff2}}\right) \tag{7}$$

Similarly,

$$\delta Q = \frac{Q}{2}\left(\frac{\delta V_{gs1}}{V_{eff1}} + \frac{\delta V_{gs2}}{V_{eff2}} - \frac{2\delta V_{gs3}}{V_{eff3}}\right) \quad (8)$$

where $V_{effi} = V_{gsi} - V_{tn}$ and $V_{gsi}$ is the effective gate-to-source voltage of the triode transistor in transconductance cell $g_{mi}$. It can be seen from Eq. (7) that the tuning range of this filter is determined by the range of the gate-to-source bias voltages applied to the triode transistors in transconductor elements 1 and 2. From Eq. (8) it is obvious that the maximum spread in the Q-factor is also dependent on the range of the gate-to-source bias voltages for the triode transistors. If these gate-to-source control voltages are limited, then the tunability of the filter is severely restricted.

Other filter parameters such as gain range, are also sensitive to the range of the triode transistor control voltages. For instance, the gain of a low-pass filter is given by

$$G_{LP} = \frac{g_{m4}}{g_{m1}} \quad (9)$$

The sensitivity of the gain is thus,

$$\delta G_{LP} = G_{LP} \cdot \left(\frac{\delta V_{gs4}}{V_{eff4}} - \frac{\delta V_{gs1}}{V_{eff1}}\right) \quad (10)$$

which means that a wide variation in gain amplitude is only possible for a broad control voltage range. A similar result holds for the center frequency gain of a bandpass filter.

The sensitivity equations presented above clearly show that it is desirable to have a large and variable control voltage available for biasing the gates of the triode transistors. A greater control voltage range permits a larger $V_{eff}$ and reduces the nonlinear behavior of the triode transistors. Good linearity, along with a broad tuning range is highly desirable in many hearing aid applications where great flexibility is needed in the programmability of the frequency response of the filter. For a low-voltage filter design, this requirement poses a great challenge.

If an n-channel transistor is used for $Q_7$ as in Fig. 2, the minimum control voltage, Vc, required to turn on the transistor is

$$Vc > V_{icm} + |V_{tp}| + V_{tn} \quad (11)$$

where $V_{icm}$ is the input common-mode voltage level. Assuming $|V_{tp}| = V_{tn} = 0.75V$ this requires a gate voltage that exceeds the 1.5V supply. What is required then, is an efficient solution to increase the dynamic performance of the filter. The solution is provided by dynamic gate biasing which is presented next.

## III. DYNAMIC GATE BIASING

In Dynamic Gate Biasing (DGB), charge pump circuits are used for the stable biasing of MOSFET gates. There are many voltage doubler and multiplier circuits, but not all are suitable for low-voltage operation. Most of the traditional multiplier techniques used in nonvolatile memory circuits such as the Dickson charge pump [8] are extremely inefficient at low supply voltages because they suffer from a forward-bias diode voltage drop and are prone to large ripples at the output.

Another class of multiplier designs more suitable for low-voltage operation are those based on switched-capacitor techniques [9]. A high-efficiency CMOS voltage doubler with good accuracy is presented in [1]. This design is simple and power efficient and was chosen to demonstrate the principle of dynamic gate biasing.

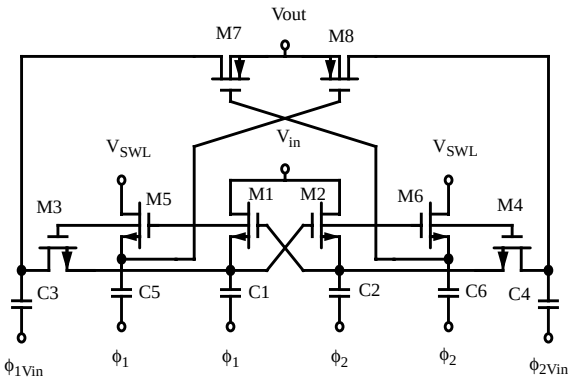


**Fig. 4** Proposed bias voltage doubler

The proposed bias voltage doubler circuit [2] is shown in Fig. 4. The circuit is a voltage doubler with two unique characteristics. First, the doubler has a separate input, $V_{in}$, because the bias voltage to be doubled is different from the supply. Second, the doubler can accept input levels that lie near the threshold voltage. This ability is important in low-voltage applications where the bias voltages are often only slightly higher than the device threshold voltage. The lowest voltage charge pump reported to date requires a supply voltage at least 0.5V above the threshold [10].

To overcome this limitation, the standard charge pump

must be redesigned to take advantage of the full supply voltage when driving switches. The voltage doubler consists of three tightly-coupled charge pumps. The innermost charge pump uses devices $M_1$ and $M_2$ to generate level-shifted clock signals with the full supply swing. These clock signals are used to drive the outermost charge pump that performs the actual doubling of the bias voltage using devices $M_3$ and $M_4$. The clock signals $\Phi_{1Vin}$ and $\Phi_{2Vin}$ have a reduced voltage swing that is equal to the input voltage. The final charge pump uses devices $M_5$ and $M_6$ to generate full-swing clock signals, but here the low level is shifted to $V_{SWL}$ that is optimized for driving the pMOS output switches $M_7$ and $M_8$. The full-swing clock signals $\Phi_1$ and $\Phi_2$ are generated from an integrated, non-overlapping, two-phase clock generator [11] that is shown in Fig. 5.

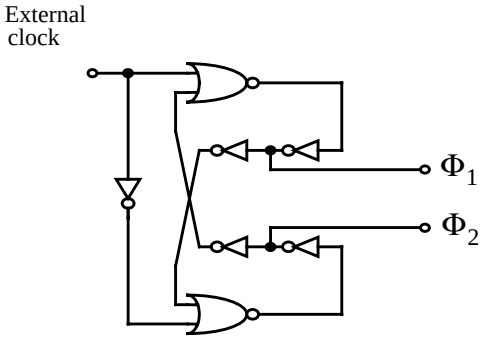


**Fig. 5** Non-overlapping clock generator

The use of this voltage doubler easily allows for dynamic gate biasing of MOSFETs in the triode region. Since the load consists of the gate capacitances of the transistors, no steady state current is drawn from the voltage doubler, and ideally no output ripple is generated. In practice, some ripple is generated through parasitic current leakage, charge injection and clock feedthrough. Such nonidealities can be minimized by setting the clock frequency of the voltage doubler beyond the frequency range of hearing (i.e., 20kHz). Still, the output voltage is quite accurate and controllable over a large enough range ($V_{DD}$ to $2V_{DD}$) to permit good linearity and broad tuning. If the filter application demands even more tunability, then the voltage doubler can readily be converted into a general purpose multiplier.

It is worth noting from Fig. 1 that five voltage doublers would be needed for maximum programmability of the second order filter. In order to save die area, it may be desirable to use fewer doublers to set multiple control voltages at the cost of reducing the degrees of freedom in the filter implementation.

## IV. SIMULATIONS

The continuous-time filter was simulated with HSPICE, using the models for a 0.35μm CMOS technology. A tunable low-pass filter for a programmable hearing aid application was simulated and shown in Fig. 6.

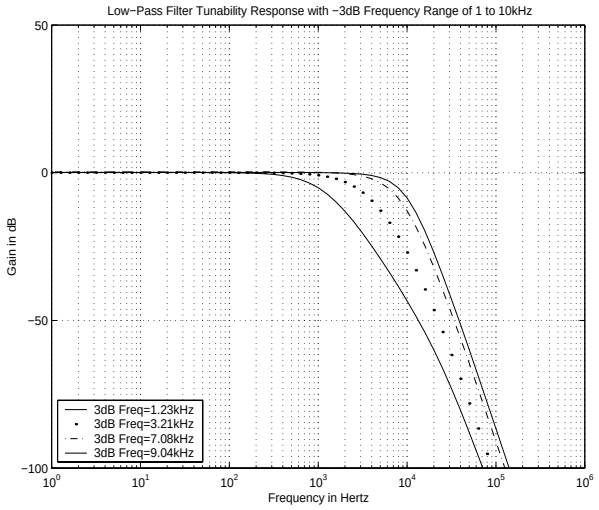


**Fig. 6** Low-pass filter simulations

The filter was tuned over the frequency range of 1kHz to 10kHz with a control voltage range between $V_{DD}$ and $2V_{DD}$. The center frequency $\omega_0$ was varied by adjusting $V_{gs1}$ and $V_{gs2}$ according to Eq.(7) and simultaneously adjusting the other control voltages such that $\delta Q = 0$ and $\delta G_{LP} = 0$. This latter restriction ensures that the gain and Q-factor selectivity remain the same over the swept frequency range. This is often a desirable property in a programmable hearing aid used for low frequency gain compensation [12]. If more flexibility is needed in the frequency response of the filter, then the filter gain and selectivity can be varied according to Eq.(8) and Eq.(10). A noise analysis simulation for the low-pass filter with a -3dB frequency of 3.21kHz showed that the signal-to-noise ratio was better than 70dB.

Simulations of low-pass, bandpass and high-pass filter responses are shown in Fig. 7.

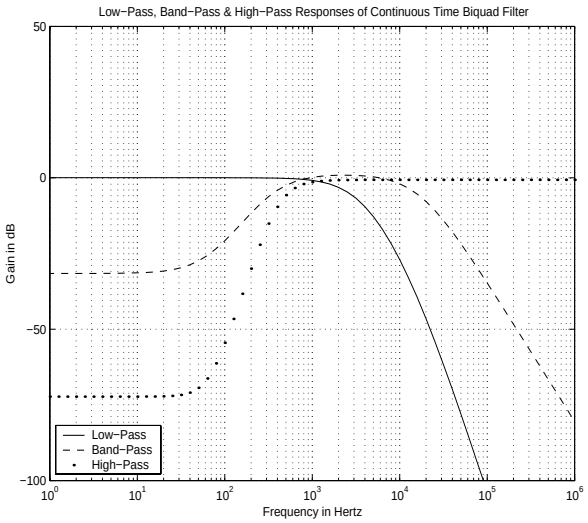


**Fig. 7** Prototype filter simulations

The center frequency and Q-factor selectivity were varied by adjusting the control voltages while maintaining unity gain. These filter characteristics are useful for accommodating a wide range of hearing deficiencies.

The performance of the voltage doubler circuit was simulated separately and shown in Fig. 8. The simulation used an input voltage of 1.5V and a small output load capacitance of 1.0 pF to speed up the transient response. The circuit exhibited hardly any undershoot and reached steady state quickly due to the reduced switch resistance afforded by the dedicated charge pump driving the output switches. Load currents during start-up and tuning were also observed as expected [13].

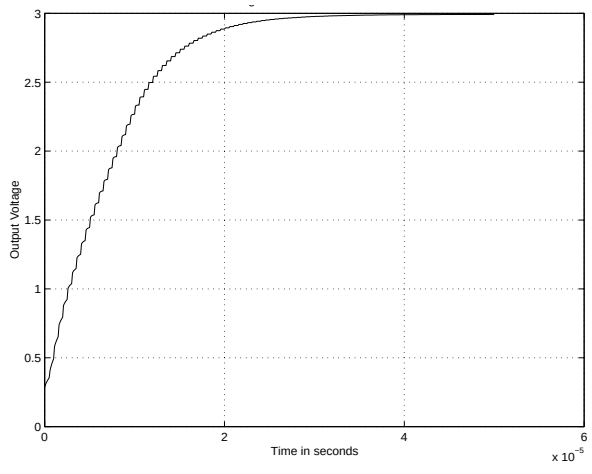


**Fig. 8** Simulation of step-up response for voltage doubler.

## V. CONCLUSION

In this paper we discussed the principle of dynamic gate biasing, an experimental approach to low-voltage / low-power analog circuit design. We described how this technique could be used to extend the linearity and useful tuning range of a second order continuous time filter for hearing aid applications. As analog designers look for new ways to meet the challenge of reduced supply voltages, dynamic gate biasing has the potential to establish itself as a general technique for realizing low-voltage analog circuits.

## VI. REFERENCES

[1] P. Favrat, et al., "High-Efficiency CMOS Voltage Doubler," *IEEE J. Solid-State Circuits*, vol. 33, no. 3, pp. 410-416, March 1998.

[2] K. Phang and D. Johns, "A 1V 1mW CMOS Front-End with On-chip Dynamic Gate Biasing for a 75Mb/s Optical Receiver," *IEEE Int. Solid-State Circ. Conf. Dig. Tech. Papers*, pp. 218-219 Feb. 2001.

[3] M. Steyaert et al., "Low-voltage analog CMOS filter design," *IEEE Int. Symp. Circ. and Syst.*, vol. 2, pp.1447-1450, 1993.

[4] D. Johns and K. Martin, *Analog Integrated Circuit Design*, Wiley, Toronto, 1997.

[5] T. Kwan and K. Martin, "An Adaptive Analog Continuous-Time CMOS Biquadratic Filter," *IEEE J. Solid-State Circuits*, vol. 26, no.6, pp. 859-867, June 1991.

[6] D. Senderowicz, et al., "A Family of Differential NMOS Analog Circuits for a PCM Codec Filter Chip," *IEEE J. of Solid-State Circuits*, vol. 17, no. 6, pp. 1014-1023, December 1982.

[7] R. Castello and P. Gray, "A High-Performance Micropower Switched-Capacitor Filter," *IEEE J. of Solid-State Circuits*, vol. 20, no. 6, pp. 1122-1132.

[8] J. Dickson, "On-chip High-Voltage Generation in NMOS Integrated Circuits Using an Improved Voltage Multiplier Technique," *IEEE J. Solid-State Circuits*, vol. 11, no. 6, pp. 374-378, June 1976.

[9] J. Silva-Martinez, "A switched Capacitor Double Voltage Generator," *IEEE Proc. Mid-West Symp. Circuits and Systems*, vol. 1, pp. 177-180, 1994.

[10] J. Wu and K. Chang, "MOS Charge Pumps for Low-Voltage Operation," *IEEE J. Solid-State Circuits*, vol. 33, no. 4, pp. 592-597, April 1998.

[11] K. Martin and A. Sedra, "Switched-Capacitor Building

Blocks for Adaptive Systems," *IEEE Trans. Circ. and Syst.*, vol. 28, no. 6, pp. 576-584, June 1981.

[12] D. Wayne et al., "A Single-Chip Hearing Aid with One Volt Switched-Capacitor Filters," *IEEE Proc. of Custom Integrated Circuits Conference*, pp. 7.5.1 - 7.5.4, 1992.

[13] G. Monna, et al., "Charge pump for optimal dynamic range filters," *IEEE Int. Symp. Circuits and Systems*, vol. 5, pp. 747-750, 1994.