A 15-Gb/s Preamplifier with 10-dB Gain Control and 8-mV Sensitivity in 65-nm CMOS

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***Abstract*— A broadband preamplifier with gain control and automated common-mode level regulation is presented. It is implemented in 65-nm CMOS as part of an analog front-end (AFE) that is especially suitable for wireline receivers incorporating digital signal processing or multilevel modulation. S-parameter measurements of the receiver show that the preamplifier remains well matched to the channel impedance across all gain settings with an S_{11} of less than -8 dB to frequencies beyond 25 GHz. The measured S_{21} of the receiver shows that the preamplifier is capable of achieving 10 dB of gain control. The preamplifier alone consumes from 16.7 mA to 56.7 mA from a 1.2 V supply, depending on its gain setting.**

I. Introduction

Electrical wireline communications suffer from frequency-dependent channel impairments such as dielectric loss and skin-effect. Multi-Gb/s CMOS transceivers designed to operate across such channels must therefore be capable of receiving signals with a small amplitude and severe intersymbol interference. An AFE including a preamplifier, a variable-gain amplifier (VGA) and equalizer (EQ) can help to optimize receiver speed, sensitivity, dynamic range and noise performance.

In DSP-based receivers, or any link employing multilevel signaling, the AFE must avoid introducing non-linear distortions to the signal before passing it to the multilevel slicer (ADC). In such applications adding gain control to the preamplifier, as illustrated in Figure 1, obviates the need for a separate VGA stage, which can help to minimize power and area consumption while maximizing the dynamic range.

Common methods currently used to provide gain control at the input stage are to use either a differential pair with source degeneration, as shown in Figure 2(a) [1], or to vary the size of the input transistors by turning differential pairs on or off, as shown in Figure 2(b) [2]. Both techniques achieve good dynamic range, but creating a broadband impedance match between the input devices and the channel requires a resistive matching network, which can be detrimental to the bandwidth and noise performance of the preamplifier.

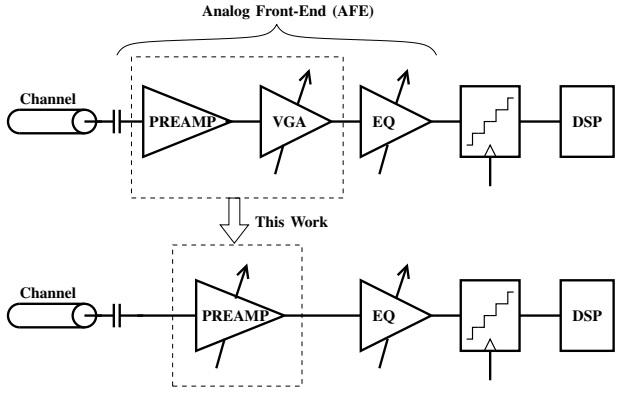

Fig. 1. A preamplifier with gain control replaces a fixed-gain preamplifier and VGA in applications requiring high linearity and wide dynamic range.

It is possible to eliminate these resistors with the use of the shunt-feedback configuration commonly associated with optical-input transimpedance amplifiers. This topology, displayed in Figure 2(c), is analyzed for electrical wireline applications in silicon technologies in [3] and is shown to outperform the preamplifiers in Figures 2(a) and 2(b) in terms of bandwidth and noise performance.

This paper introduces a high-bandwidth, low-noise, adjustable gain preamplifier based on this topology. It's single-stage implementation minimizes power consumption and maximizes linearity and dynamic range while the use of an automated control loop maintains a constant output common mode level. The amplifier demonstrates a good input match across all gain settings and exhibits bandwidth and sensitivity results that are competitive with previously reported work.

II. Preamplifier Design

The broadband preamplifier from Figure 2(c) was reduced to a single-stage amplifier in [4] in order to improve signal swing. Figure 3 shows the circuit presented in this paper, which builds upon this idea by introducing gain and CM level controls.

A. Gain Variation

A single-ended signal arrives at the preamplifier at $V_{channel}$ where two inductors are used to extend the bandwidth of the input impedance match. The feedback resistance R_f determines the low-frequency transimpedance gain of the preamplifier, R_T, which can be approximated by the equation

$$R_T = R_f \frac{A}{1-A} \tag{1}$$

where A is the open-loop voltage gain of the amplifying transistor. Hence, the preamplifier gain can be changed by adjusting R_f. This technique, however, also has the effect of changing the input impedance of the preamplifier, approximately given by

$$R_{in} = R_f \frac{1}{1-A} \tag{2}$$

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A common solution to this is to implement gain control in the second stage of the receiver chain, maintaining a fixed preamplifier gain [5] and impedance match. In this case non-linear distortions may be introduced before the variable gain stages are reached. The approach introduced in this work is to mitigate the impact of input impedance variations by decreasing $|A|$ along with R_f and by designing the input stage to be well matched to the channel when the received signal is smallest.

Bias levels at the input and output of the amplifying transistor are set by M_3, which pulls a DC current through R_f. This raises the CM level at V_{out} and obviates the need for a common-source level-shifting stage following the preamplifier [4]. This means, however, that varying R_f will also change the CM levels of the preamplifier.

B. Output CM Control

A copy of the preamplifier (M_1^D - M_3^D) is used to replicate DC biasing. The resulting pseudo-differential signal (V_{out} - V_{out}^D) is passed to subsequent differential stages providing power supply and common-mode noise rejection. However, in this topology changing R_f will impact the CM levels of the preamplifier. To control this, the opamp in Figure 3 monitors the output level at V_{out}^D and fixes both V_{out} and V_{out}^D to V_{ref} by manipulating the current sourced by M_2.

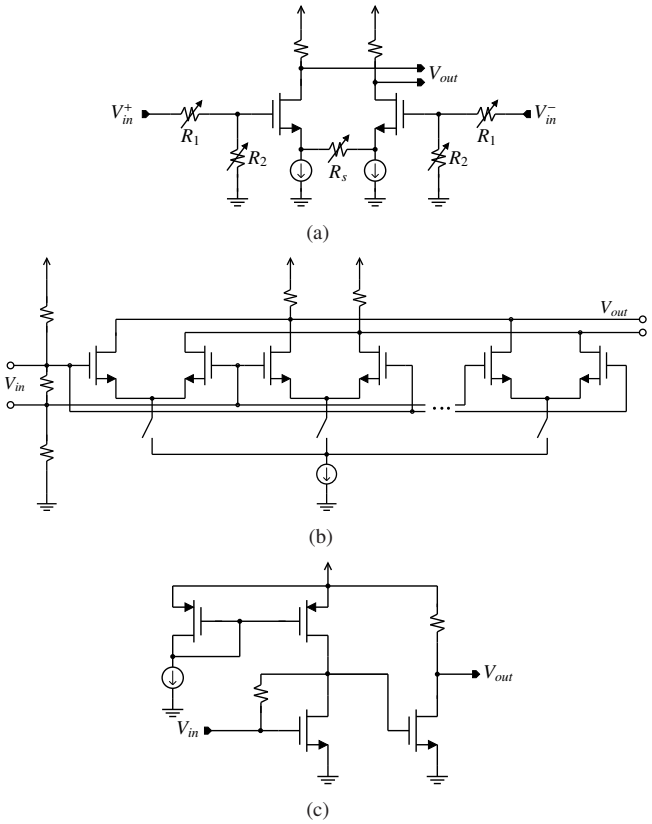


Fig. 2. Existing variable gain input stages include (a) source degeneration [1], (b) width control [2], (c) shunt-feedback configuration [3].

By reducing the effective impedance of M_2 and M_2^D at low gain settings the control loop also has the effect of reducing the magnitude of the open-loop gain, $|A|$, of the preamplifier. This helps to mitigate the change in input impedance according to equation (2) and also further reduces the transimpedance gain according to equation (1). Since this reduction in gain occurs without impacting the dominant pole of the amplifier, it also results in an increase in bandwidth for these low-gain settings. Simulated results in a standard 65-nm CMOS process show that this effect leads to an increase in bandwidth by a factor of 1.6x when compared to a preamplifier with no CM level control.

The CM stabilization also adjusts the current density of M_1. For low gain settings its gate voltage is increased providing a large overdrive voltage and, hence, high linearity. Simulated results show that this setting results in a total harmonic distortion (THD) of less than -34 dB. For high gain settings the gate voltage of M_1 is decreased, improving its noise performance. In total, the measured current drawn by 60 μm wide transistor M_1 ranges from 4.9 mA at the high-gain setting, to 24.3 mA at the low-gain setting.

The opamp used in this control loop is a simple single stage amplifier with NMOS inputs and an active, current mirror load. Simulated results show that the compensation provided by the gate capacitances of transistors M_2 and M_2^D is enough to ensure stability with a phase margin of at least 70^0.

III. Equalization

The AFE implemented in this work incorporates the split-path equalizer introduced in [6], which creates high-frequency peaking by decreasing low-frequency gain. This provides an additional stage of gain control for the receiver helping to ensure wide dynamic range in the AFE. Simulation results show that the equalizer's low-frequency gain can be varied from 4 dB to -9 dB producing a maximum possible high-frequency peaking of approximately 13 dB.

IV. Measured Results

The preamplifier was incorporated into a receiver with a 4-level slicer in a standard 65-nm CMOS process. The entire

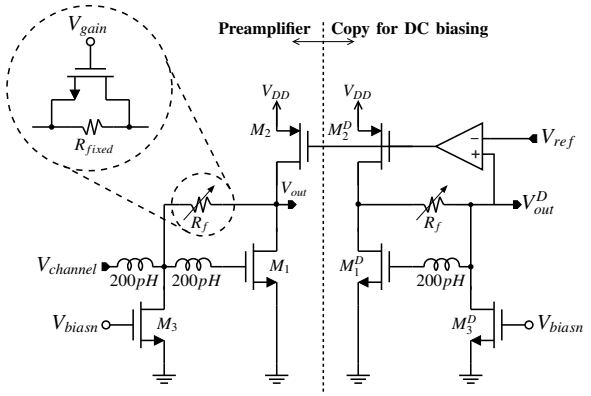


Fig. 3. Schematic of the preamplifier introduced in this work.

receiver occupies approximately 0.23 mm^2 (excluding pad frame) and has a measured power consumption of 252 mA from a 1.2 V supply. The AFE accounts for 67.1 mA of this total, with the rest being used in the output drivers and current-mode logic of the digital back end. A die photo is displayed in Figure 4. All measurements were made on-wafer.

A. S-parameters

S-parameter measurements were taken to evaluate the input match of the receiver. The measured S_{11} results are shown in Figure 5 for various gain settings. For the highest preamplifier gain settings (V_{gain} = 0.8 to 1.2 V), which are used when the received signal is smallest and a good input match is critical, S_{11} remains below -12 dB to well beyond 20 GHz. For the lowest preamplifier gain settings (V_{gain} = 1.6 to 2 V) the input match remains below -8 dB to well beyond 20 GHz. For prototype testing, a dedicated, off-chip source was used to generate the preamplifier V_{gain} settings. High voltage devices are unnecessary as the gate-source and gate-drain voltages of the feedback transistor do not exceed 1.2 V. In later iterations a high-voltage generator might need to be used, or it might be possible to replace the NMOS feedback transistor with an equivalent resistance PMOS device and use low control voltages instead.

The gain variation of the AFE was measured using a network analyzer with very small input signals to keep the digital CML logic operating linearly. These measurements show that the preamplifier gain can be adjusted by 10 dB, while the low-frequency gain of the equalizer can be adjusted by 9 dB for a total low-frequency gain variation of more than 19 dB.

B. Time Domain

In order to verify that the AFE can avoid distortion, multilevel signaling tests were performed. Using the 4-PAM transmitter reported in [7], a 1 GS/s, 146 mV$_{pp}$, single-ended, 2^7-1 length 4-PAM signal, shown in Figure 6(a), was applied directly to the receiver input. The receiver output shows little signal distortion in Figure 6(b). These results include the digital back end logic and output driver. The AFE alone would be able to accept even larger input signals without introducing signal distortion, although there was no test point to permit measurement of this on the prototype.

To test the receiver's sensitivity a 1-Gb, 2^7-1 length PRBS signal with an amplitude of 8 mV peak-to-peak was applied to the receiver input. The corresponding receiver output was found to be error-free and is displayed in Figure 7(a), indicating that the preamplifier has a sensitivity of at least 8 mV and therefore has a dynamic range of 25 dB. To test the overall receiver speed, a 15 Gb/s, 2-PAM PRBS signal of pattern length 2^7-1 was sent to the receiver across a 10-m coaxial cable channel with a loss of 9 dB at 7.5 GHz. This loss was compensated for by the AFE and error-free retimed data at the prototype output is shown in Figure 7(b).

The measured and simulated results of the preamplifier are

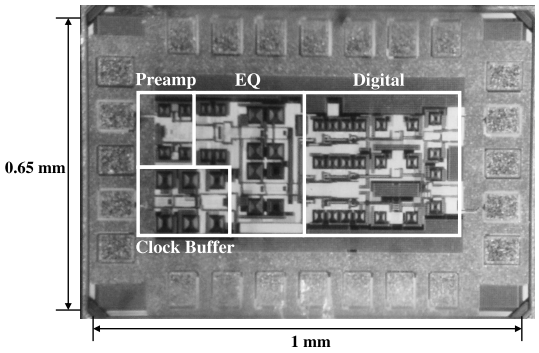


Fig. 4. Die photo of the receiver fabricated in 65-nm CMOS.

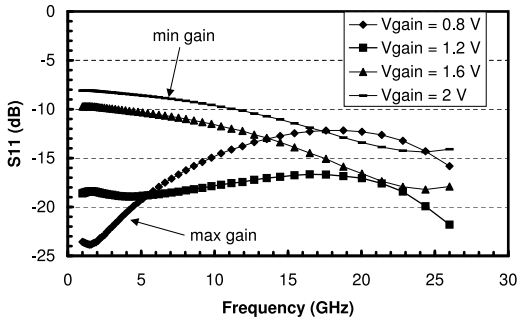
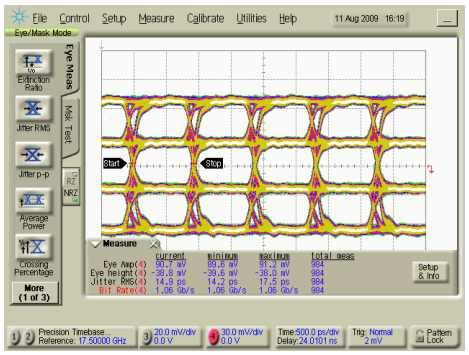
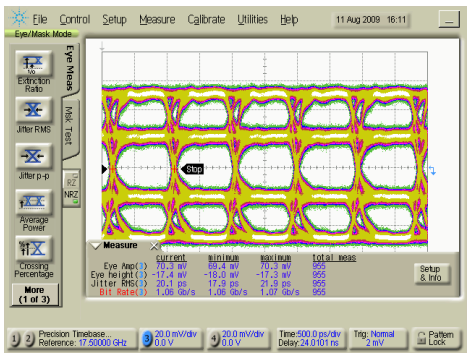


Fig. 5. Measured S_{11} shows broadband input matching for various preamplifier gain settings.



(a)



(b)

Fig. 6. (a) 4-PAM, 146 mV$_{pp}$, 1.1 GS/s test signal applied to the receiver input and (b) corresponding receiver output shows little distortion.

TABLE I

VARIABLE-GAIN BROADBAND PREAMPLIFIER PERFORMANCE SUMMARY AND COMPARISON.

Ref.	Technology	3-dB Bandwidth	THD	Gain Control	Elec. Sensitivity	Preamp Power
[1]	90 nm CMOS	7 GHz*	-45 dB*	31 dB*		
[2]	65 nm CMOS	5 GHz	-38 dB*	23 dB	-7 dBm	
[5]	90 nm CMOS	22 GHz		2 kΩ**	-20 dBm	75 mW
[8]	0.18 μm CMOS	3.9-7.6 GHz		52 dBΩ**	-19 dBm	34 mW
This Work	65 nm CMOS	30-36 GHz*	-34 dB*	10 dB	-29 dBm	20-68.1 mW

* simulated result

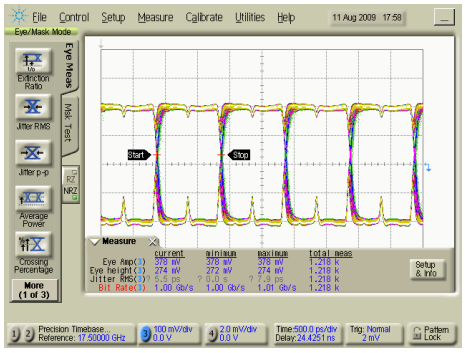
** fixed gain input stage

summarized in Table I, along with a comparison to other recently reported variable-gain preamplifier designs. This helps to illustrate the preamplifier's ability to provide a very high bandwidth, without sacrificing linearity or input sensitivity.

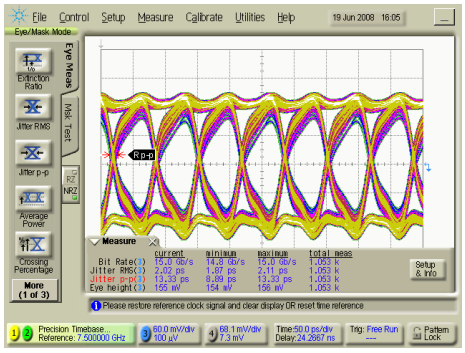
V. CONCLUSION

In order to avoid non-linear distortions receiver front-ends require gain control, which must begin in the first stage in the receiver chain. This paper has introduced a preamplifier that is suitable for this task with 10 dB of gain control and automated regulation of its output common-mode level. It is implemented as part of an AFE that is able to produce a total of up to 19 dB of gain control.

The preamplifier provides a broadband match with a measured S_{11} of less than -8 dB up to 25 GHz and across all gain settings. Simulation results show a bandwidth of at least 30 GHz and high linearity with a THD of -34 dB. Its fabrication in 65-nm CMOS as part of a complete receiver design was used to verify its ability to avoid non-linear distortions and to operate at speeds of at least 15 Gb/s. The design (including pad frame) consumes a total chip area of 0.65 mm x 1 mm and dissipates 302 mW from a 1.2 V supply.



(a)



(b)

Fig. 7. Receiver output for PRBS inputs at (a) 1 Gb/s with a 6 mV_{pp} eye opening and (b) 15 Gb/s with a 50 mV eye opening demonstrate receiver sensitivity and speed.

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