An 81Gb/s, 1.2V TIALA-Retimer in Standard 65nm CMOS Technology

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Motivation

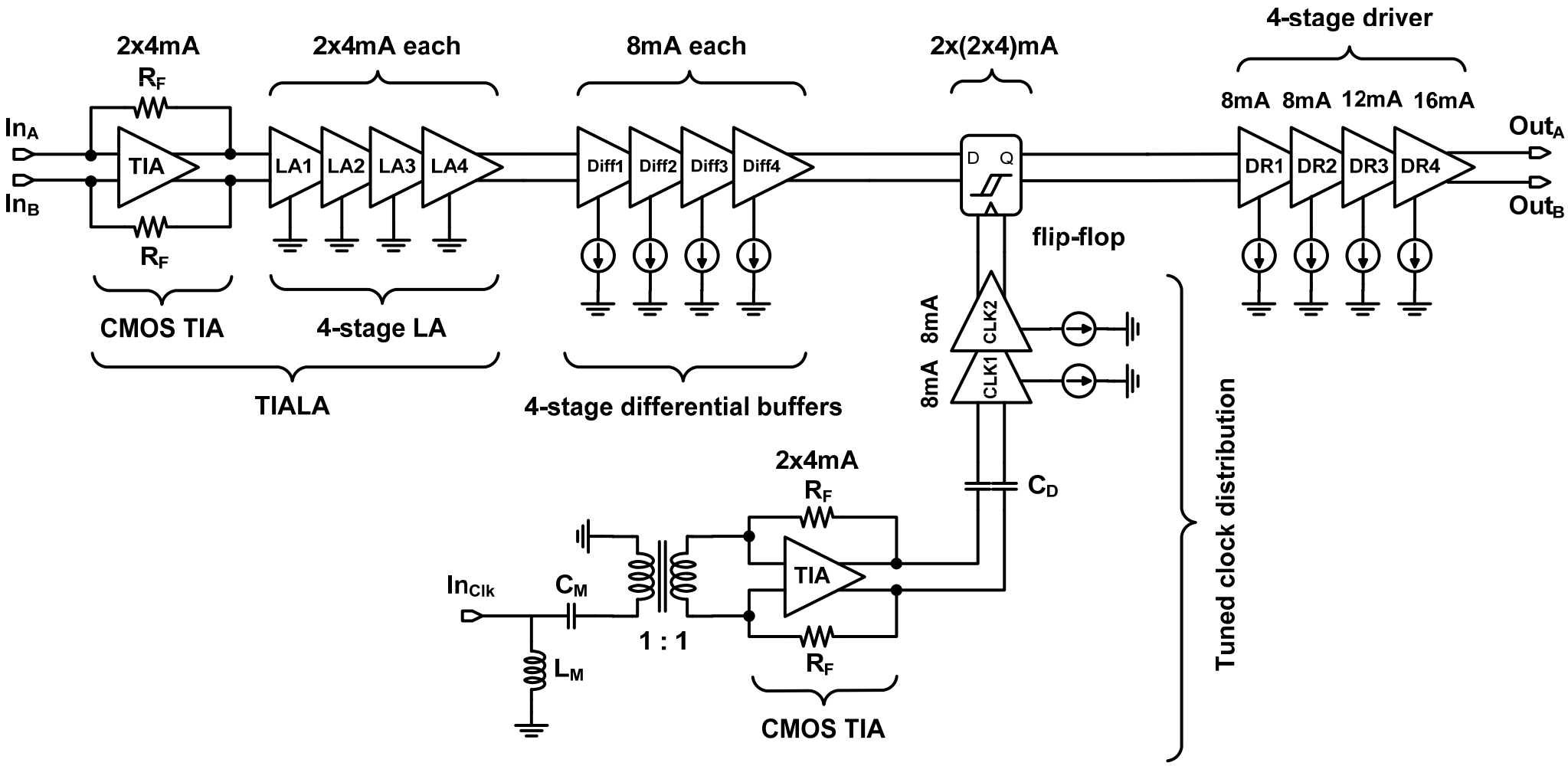
- Emerging nanoscale CMOS with f_T and f_{MAX} beyond 200GHz
- Low voltage operation and high levels of integration
  - Wireline, serial 110Gb/s applications in a single chip solution
- High speed retimers
  - Wireline transceivers, equalizers, ADCs and CML memory
- Static frequency dividers up to 100GHz in 65nm SOI CMOS
  - Retimer speeds lag behind SiGe and InP technologies

Goal and Design Methodology

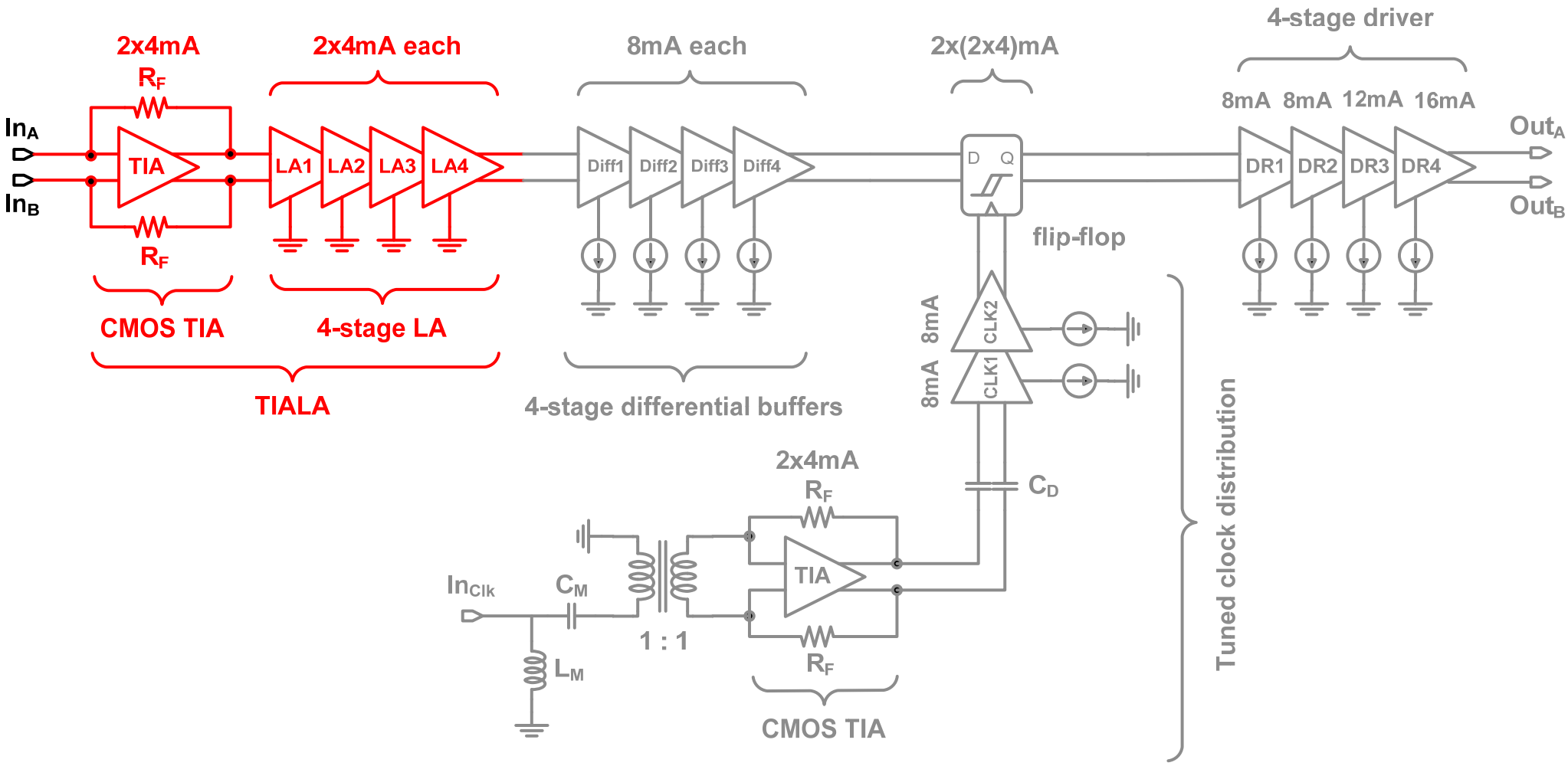
- Demonstrate a record speed TIALA-retimer in a standard 65nm GPLP process

- Low-voltage nanoscale CMOS topologies
- Optimally sizing and biasing devices
- Optimized circuit cell layout

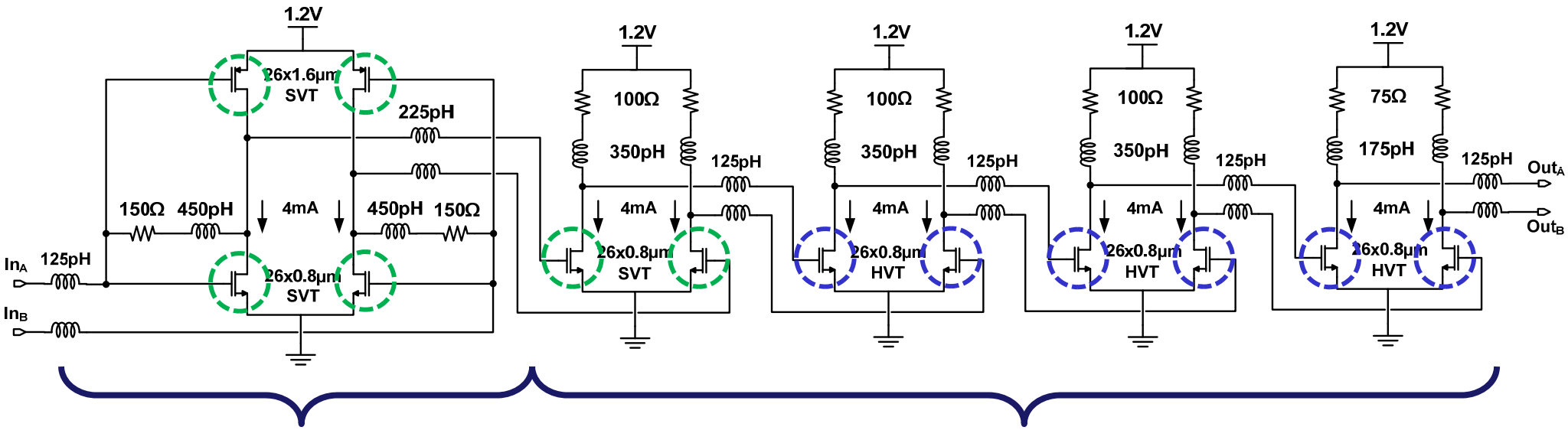
TIALA-Retimer Block Diagram



TIALA Front-end

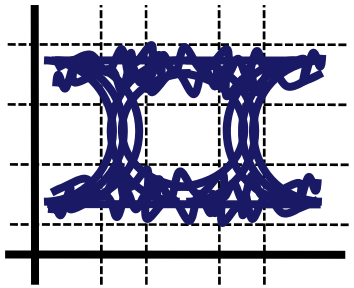


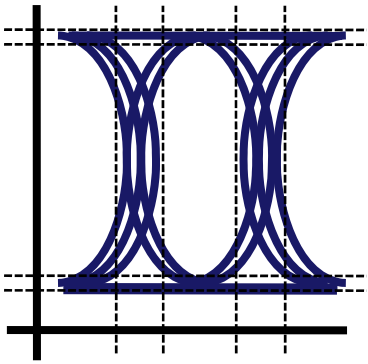
TIALA Schematics



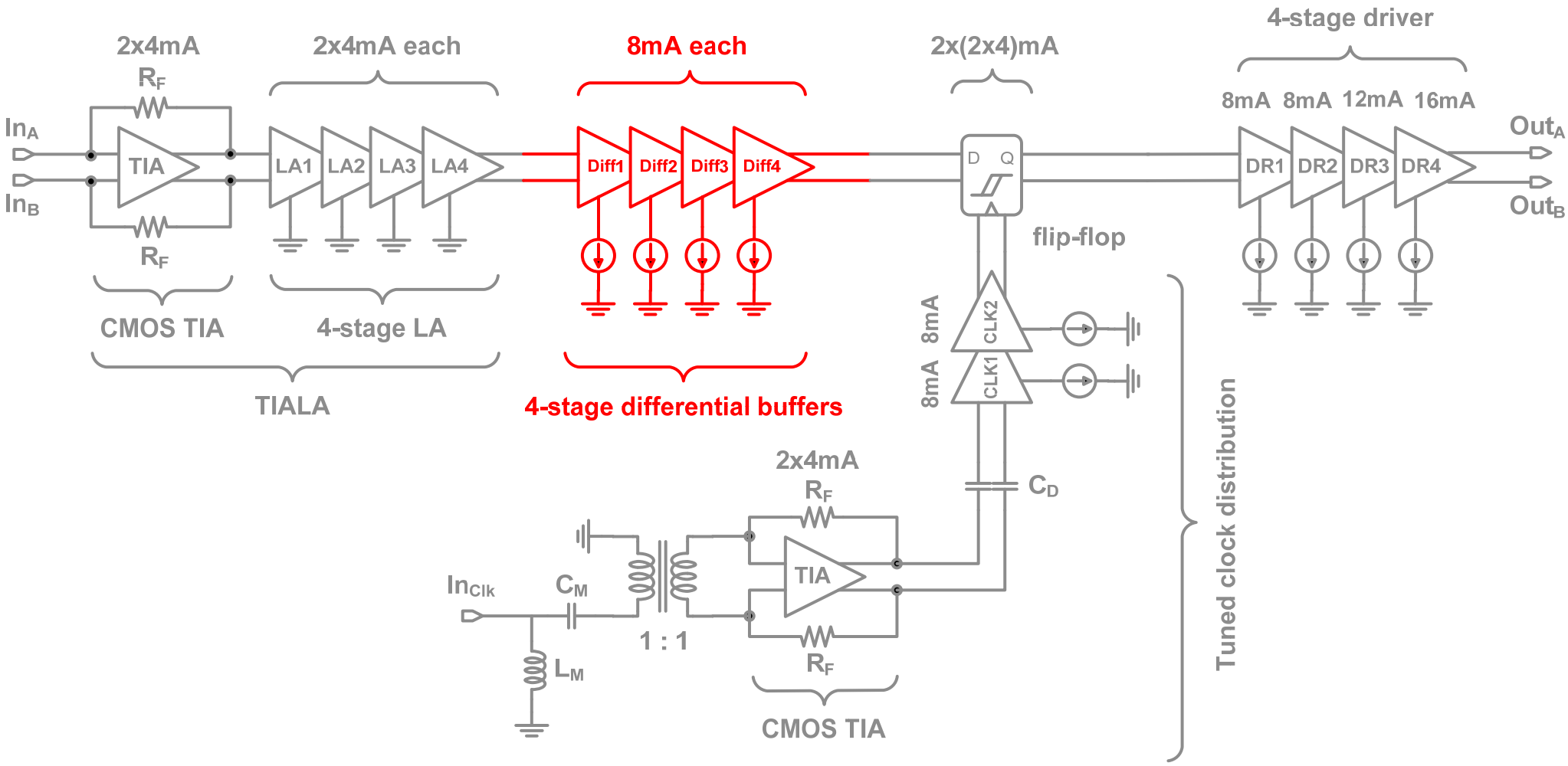
CMOS TIA **4-stage pseudo differential LA**

- Low-noise, broadband front-end
- Combination of SVT & HVT devices
- TIA: 7dB gain and 3dB BW of 80GHz
- TIALA: > 20dB of gain and 45GHz BW
- Overcome latch metastability

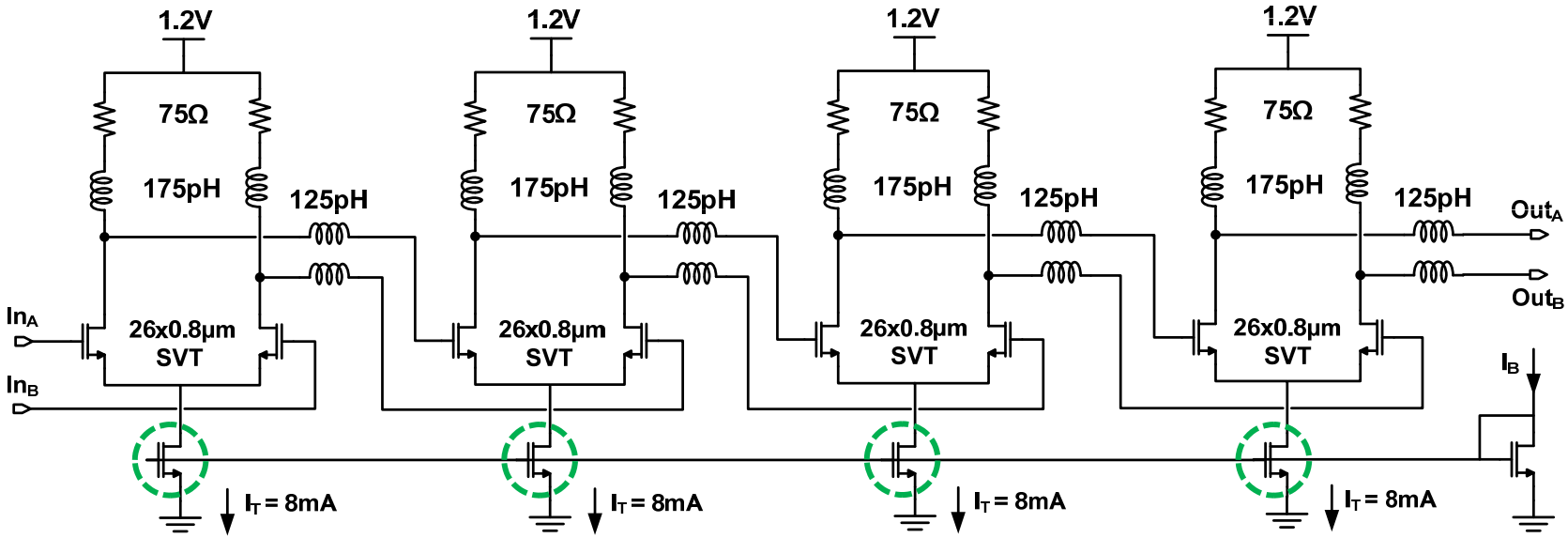




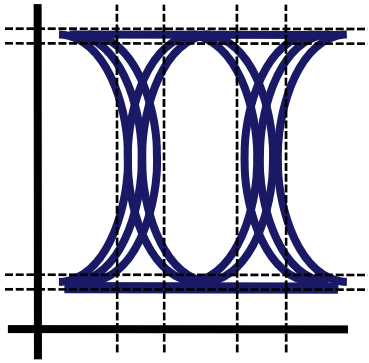
Single-ended to Differential Conversion

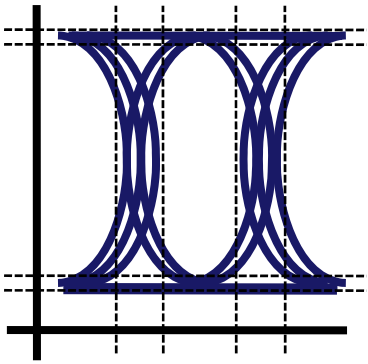


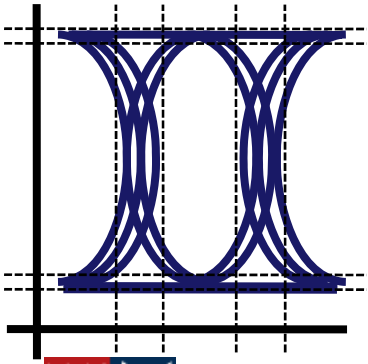
Differential Buffers Schematics



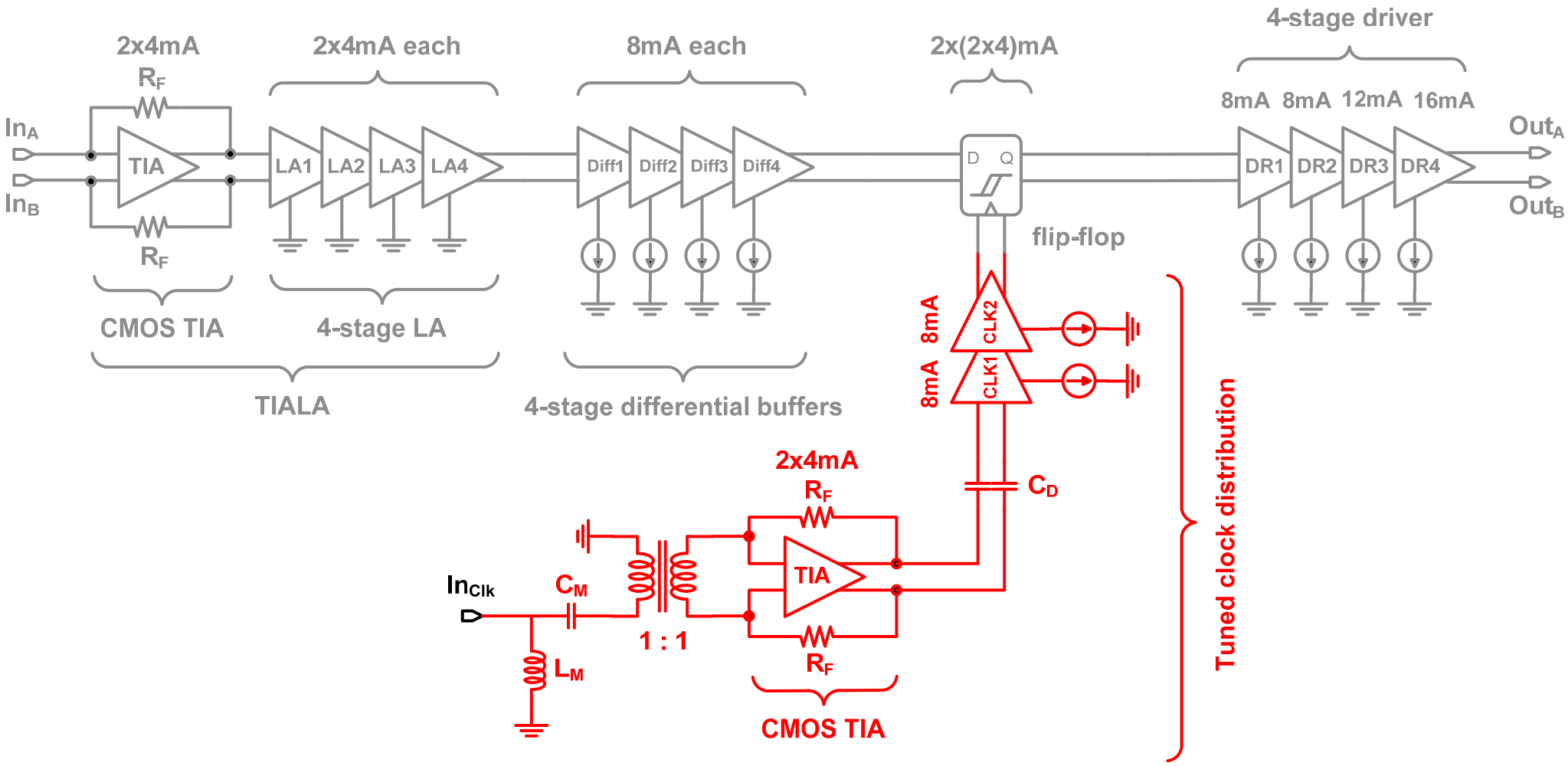
- Single-ended to differential conversion
- Operates in full switching mode
- Series-shunt peaking between stages



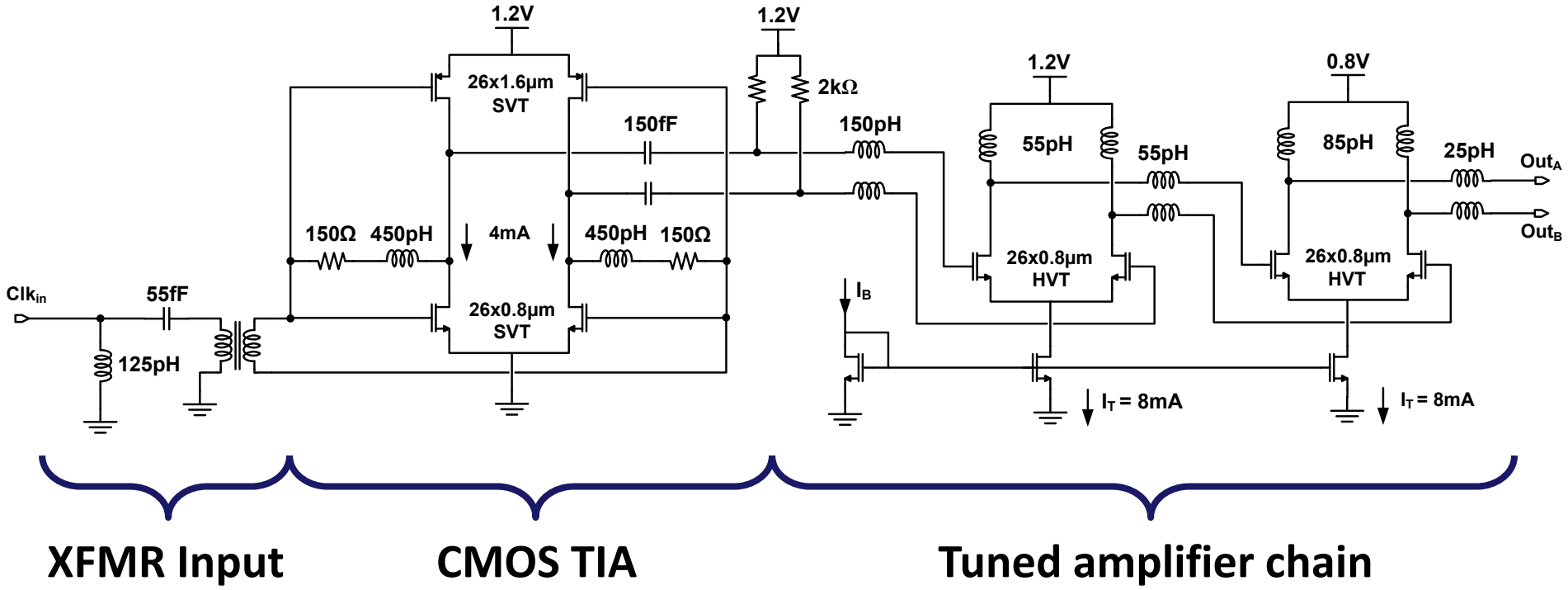


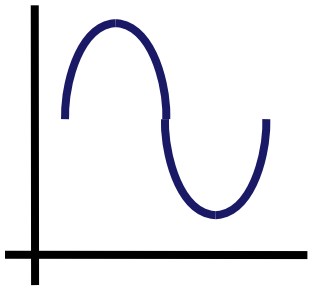


Clock Distribution

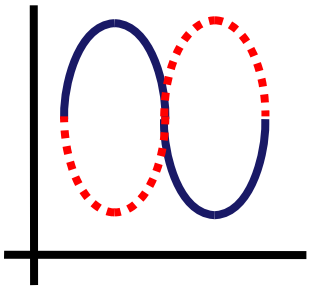


Clock Distribution Schematics

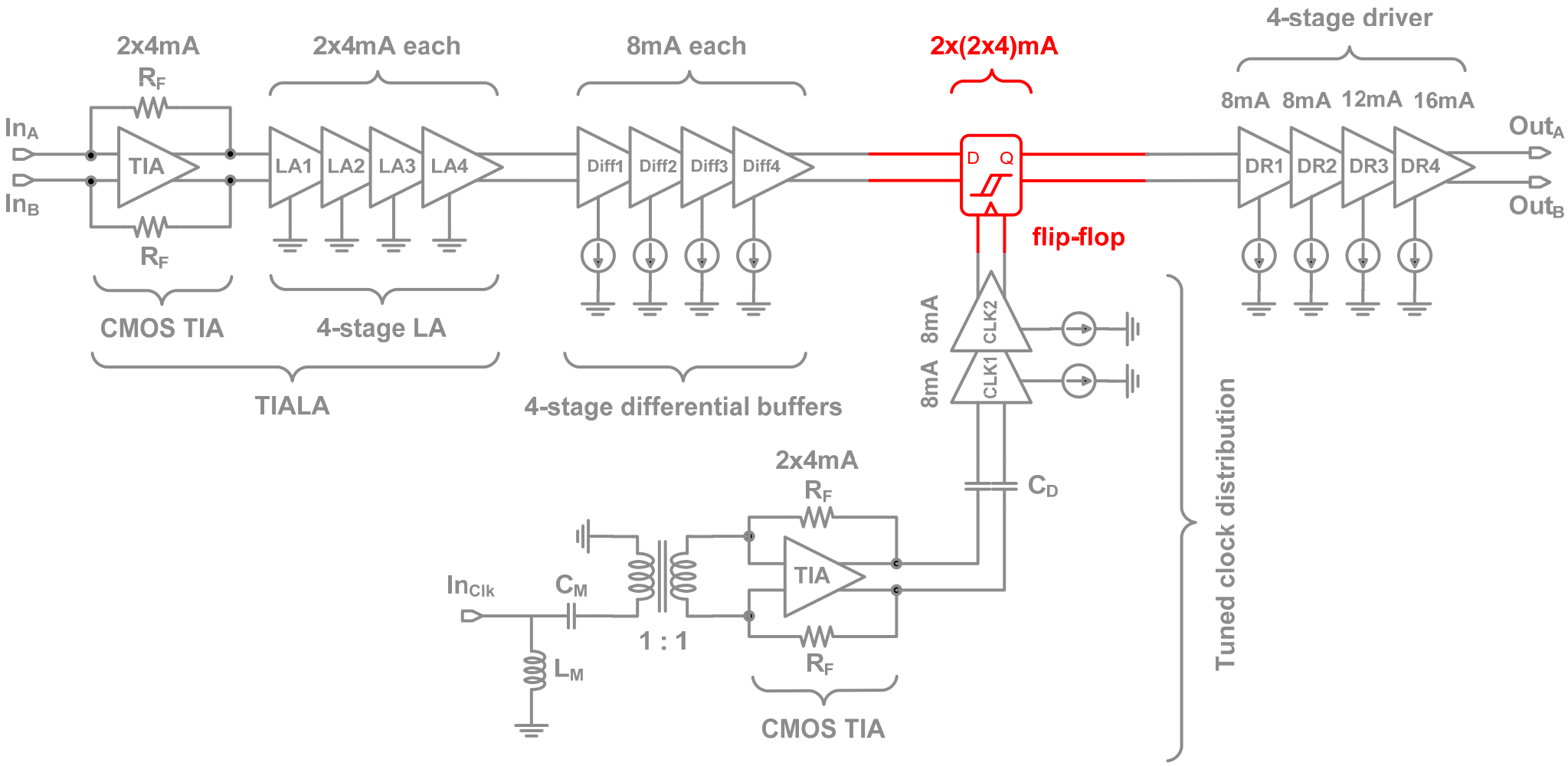




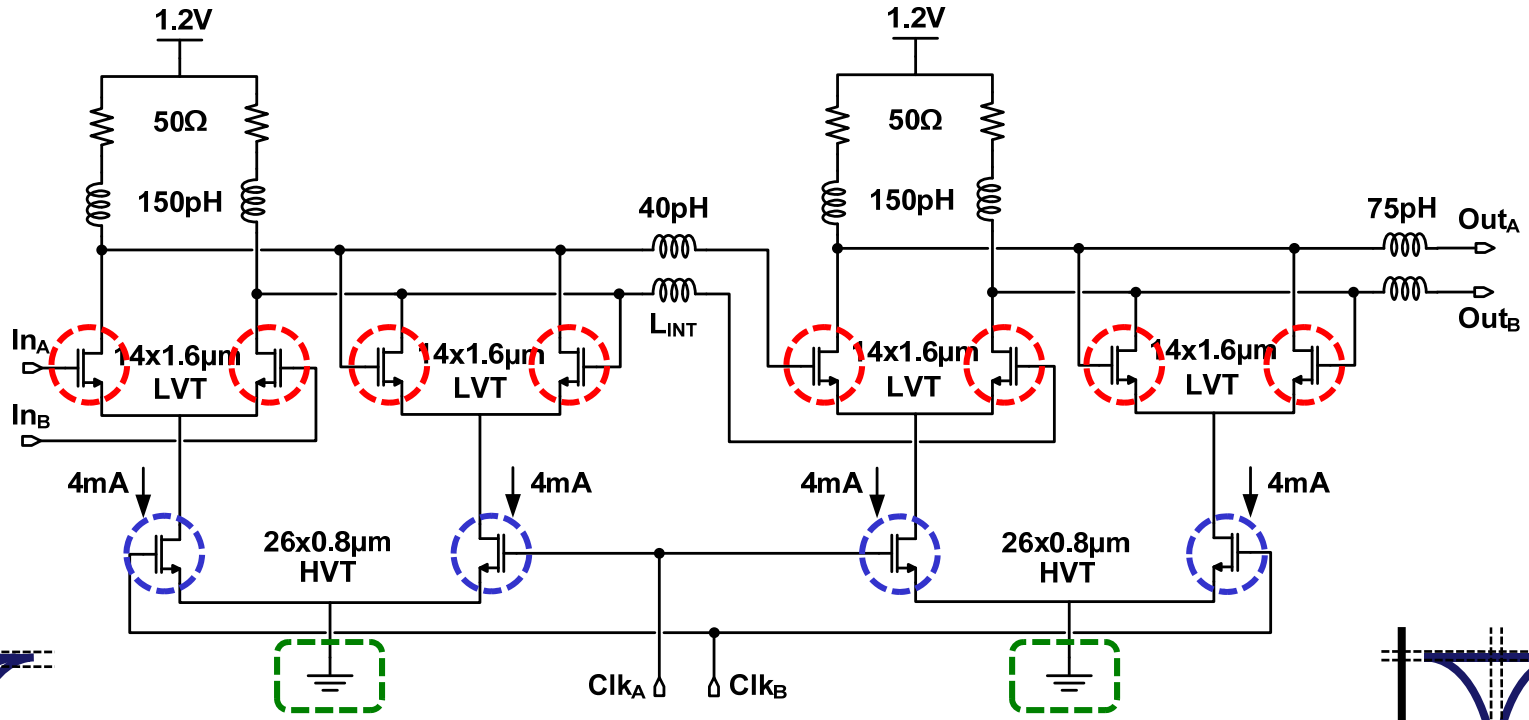
- Transformer for differential conversion
- CMOS TIA used in the 81GHz clock path
- Tuned differential amplifier chain
- > 6dB differential gain from 50G-85GHz

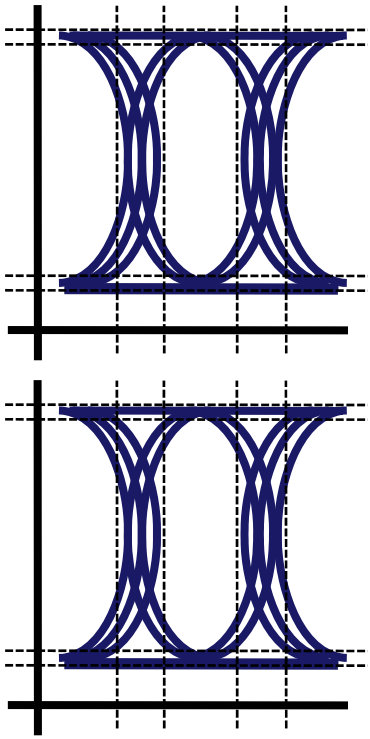


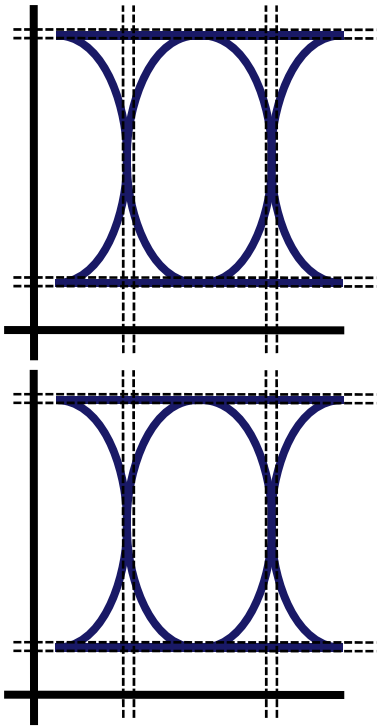
Flip-Flop (Retiming Block)



Flip-Flop Schematics

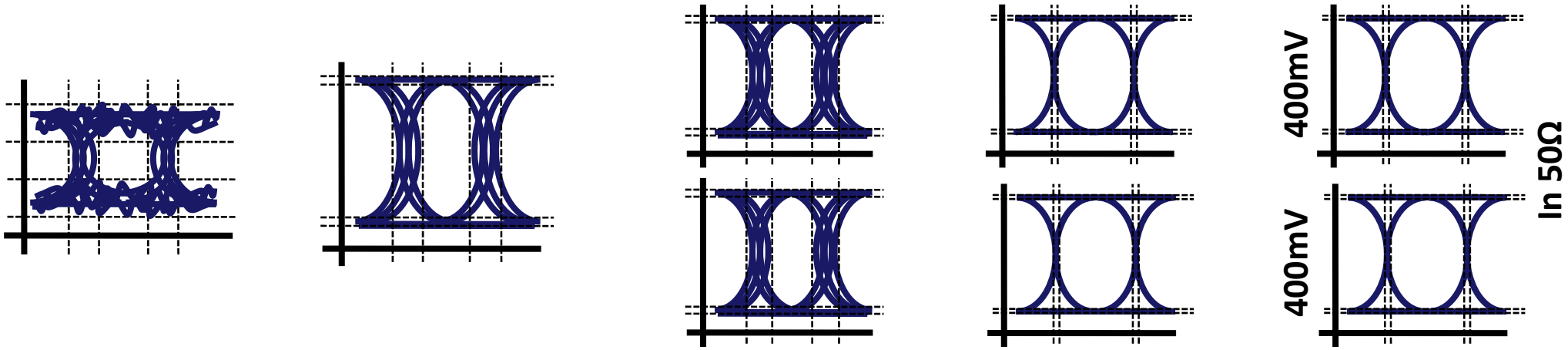


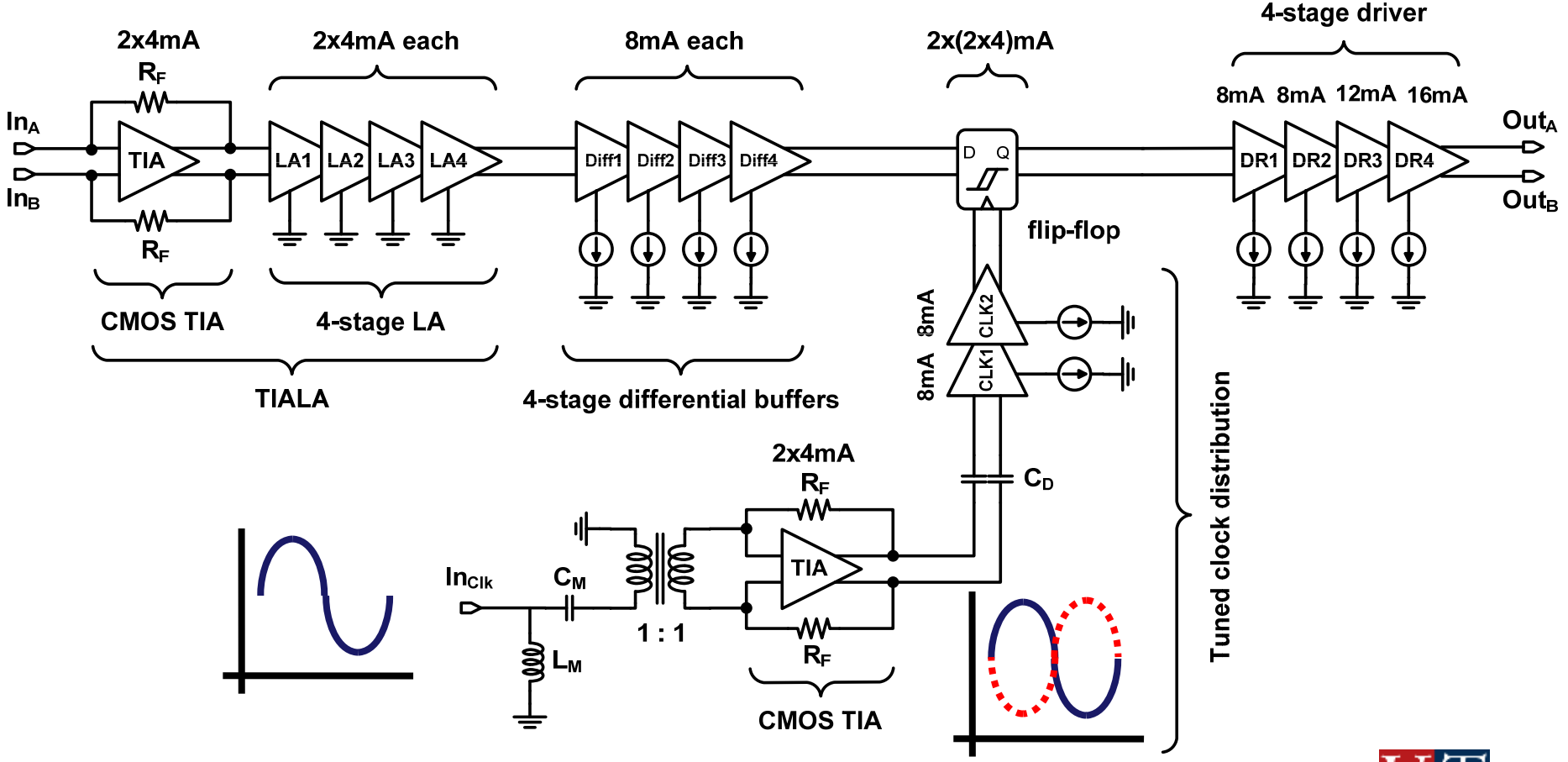




- Combination of HVT & LVT devices
- No current sources are used
- Operation from a 1.2V supply
- Layout is critical for 81Gb/s operation

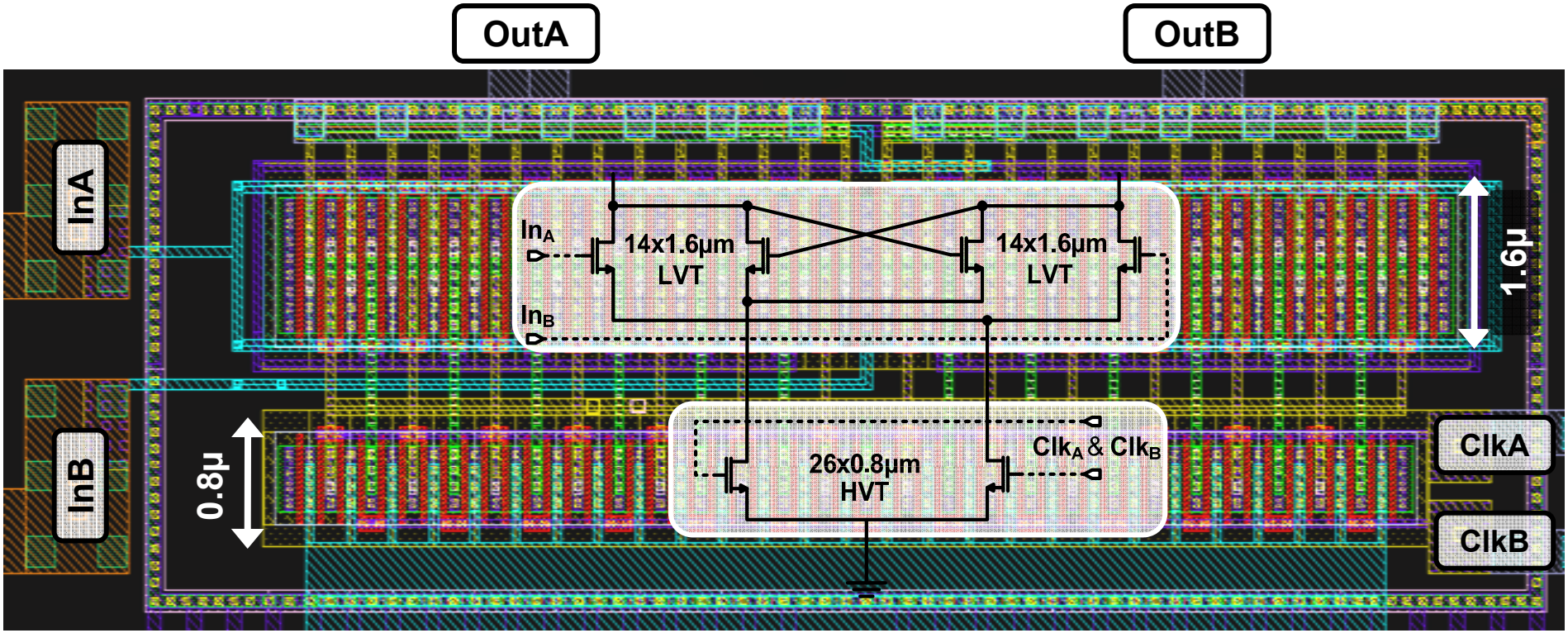
TIALA-Retimer Signal Flow



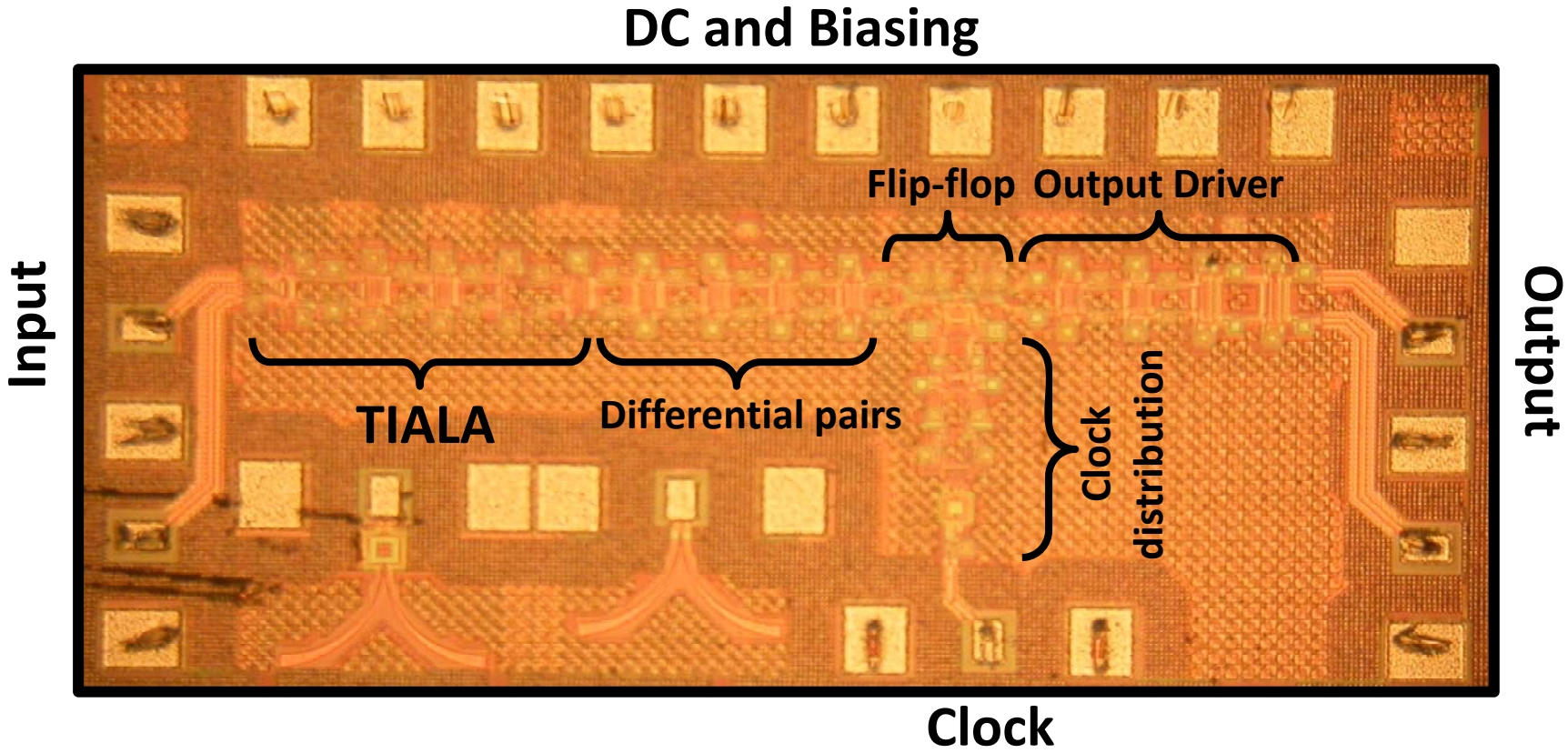


Layout Considerations

- Layout optimized by interdigitating and merging transistors with common sources or drains in a single well
- Latch example:

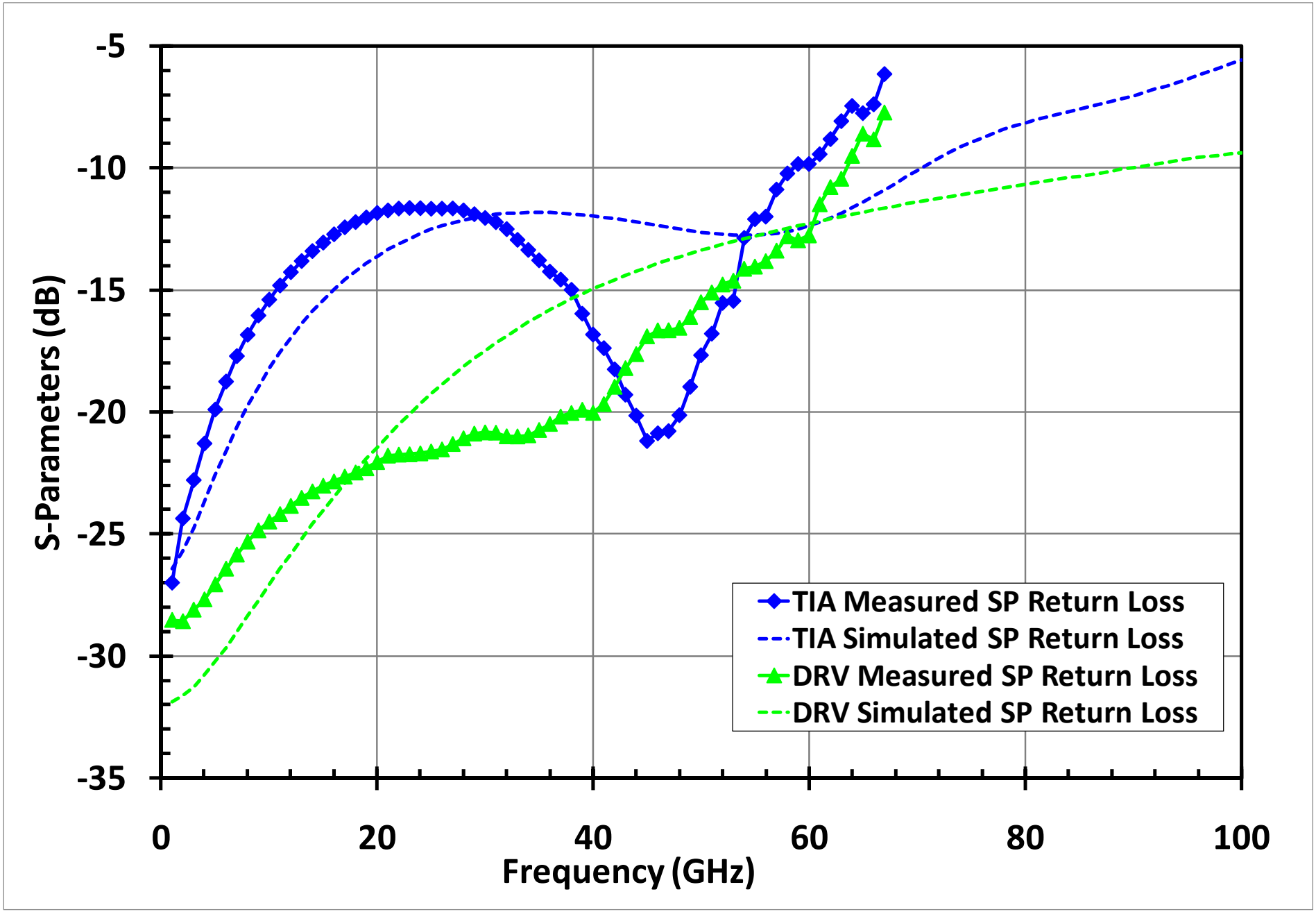


Chip Micrograph

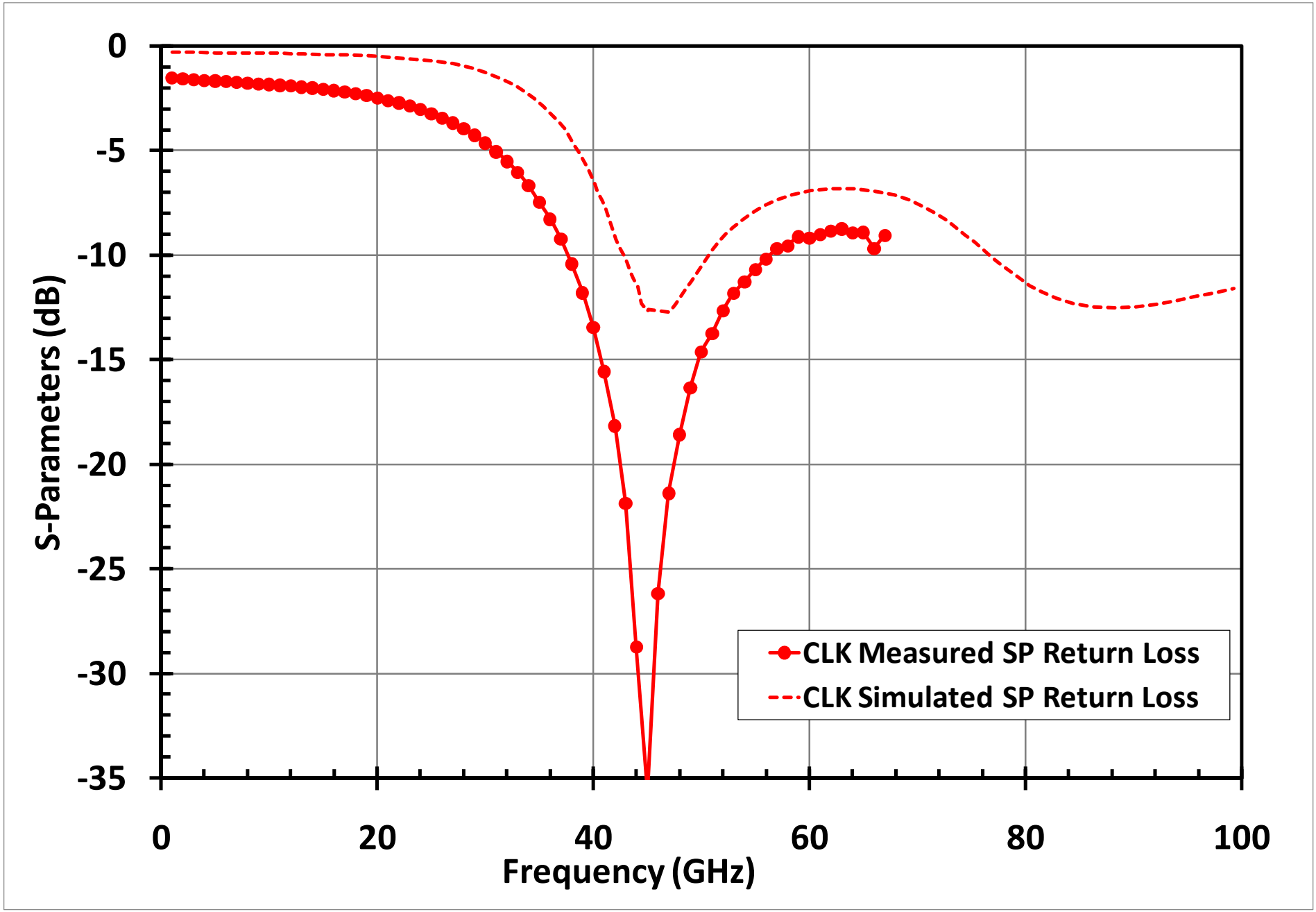


- Standard 65nm GPLP CMOS process
  - Measure f_T and f_{MAX} of an 80x1um x 60nm n-MOSFET is 170GHz and 250GHz respectively measured at V_{DS} = 0.6V
- Chip area is 0.56mm x 1.2mm including pads

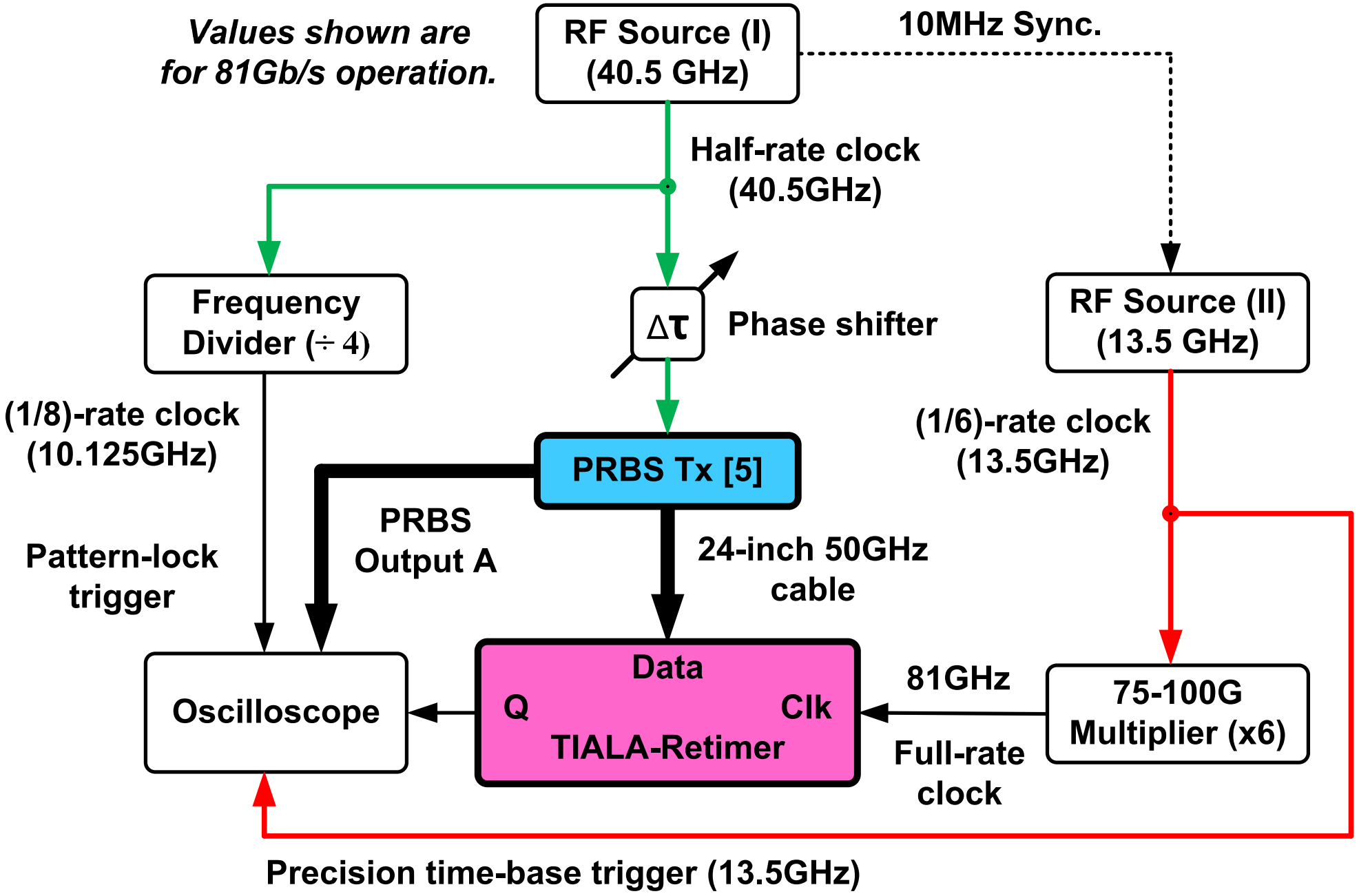
S-Parameter Measurement Results



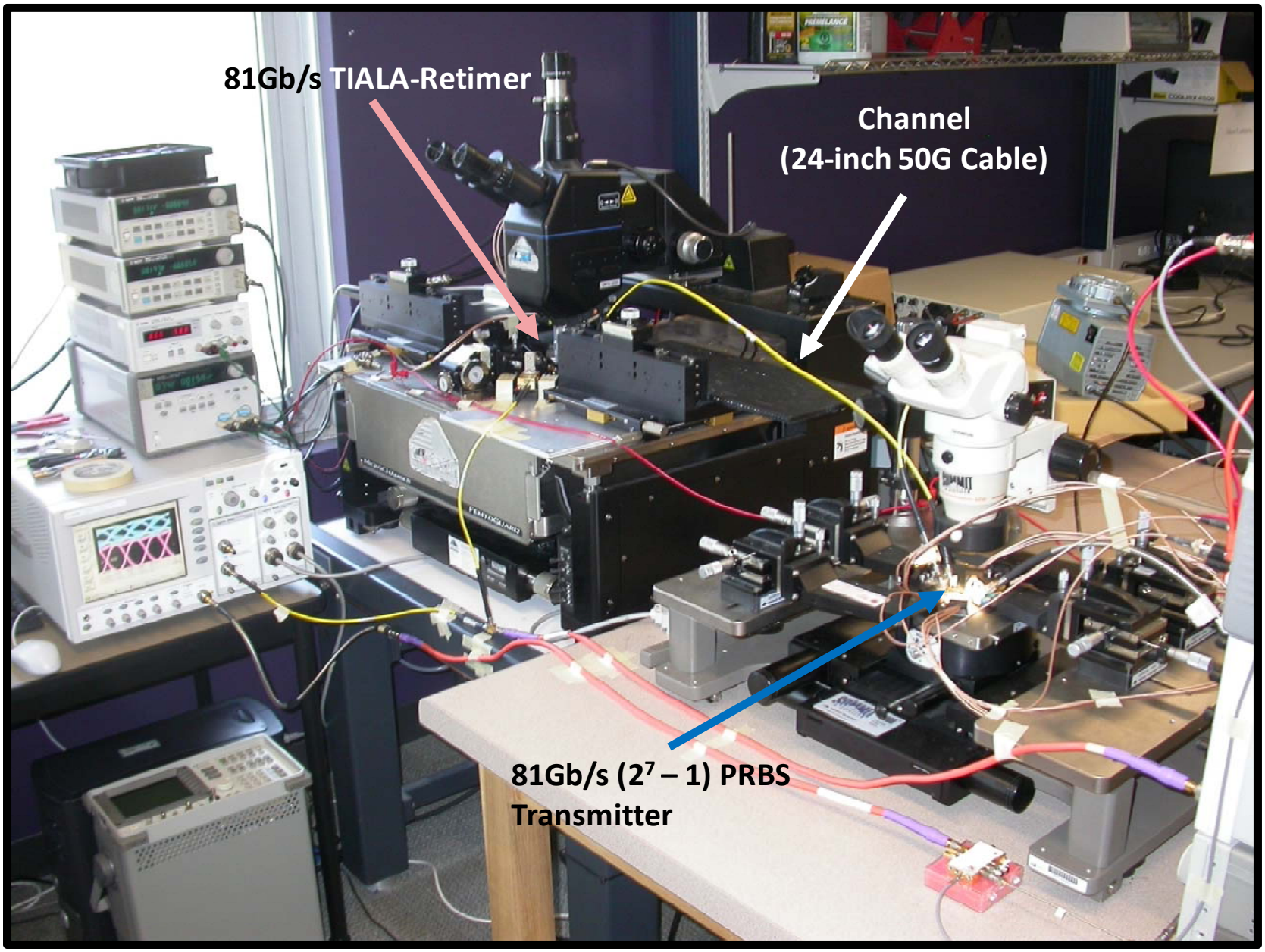
S-Parameter Measurement Results



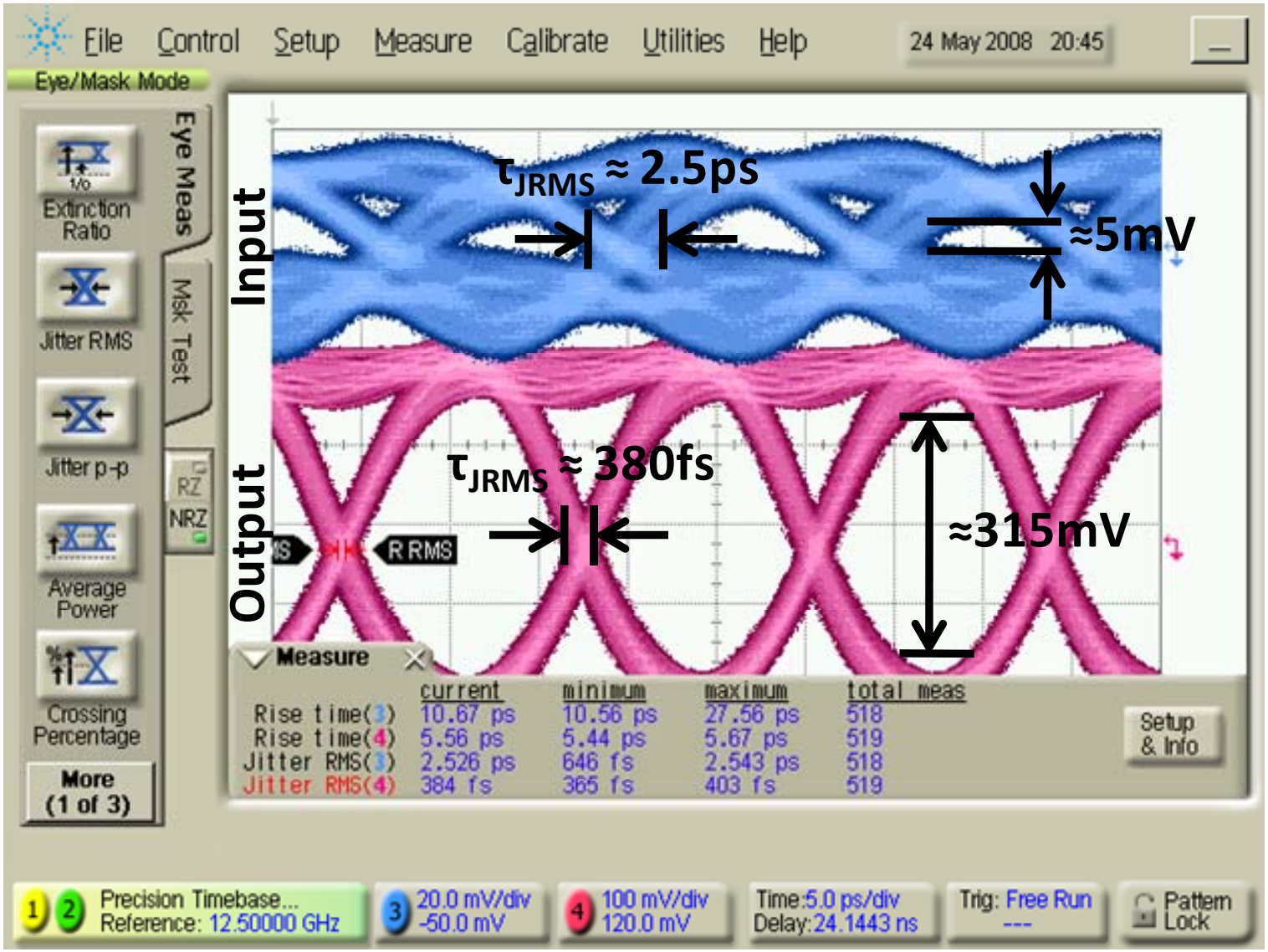
Transient Test Setup Block Diagram



Transient Test Setup Photograph

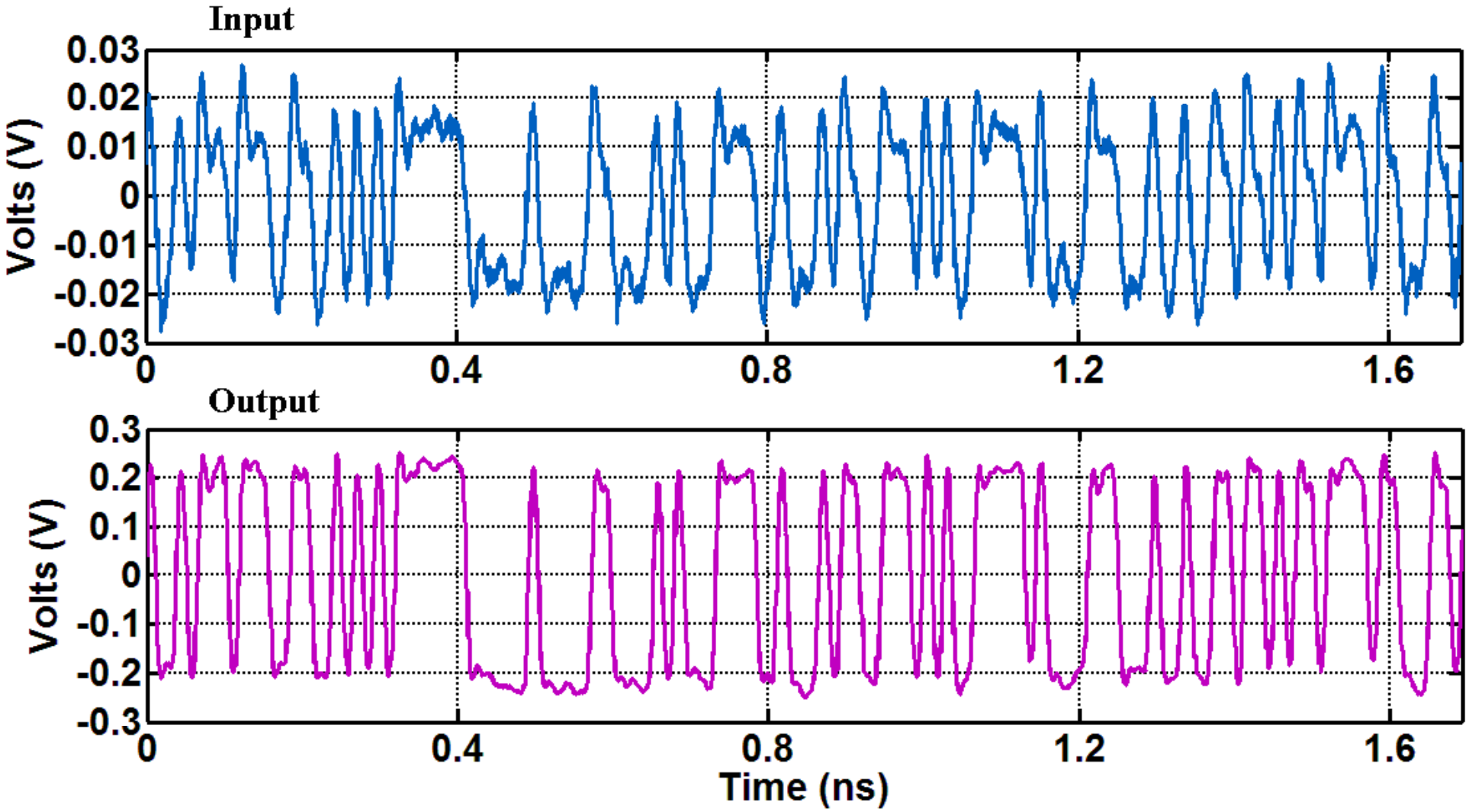


Measurement Results: 75Gb/s

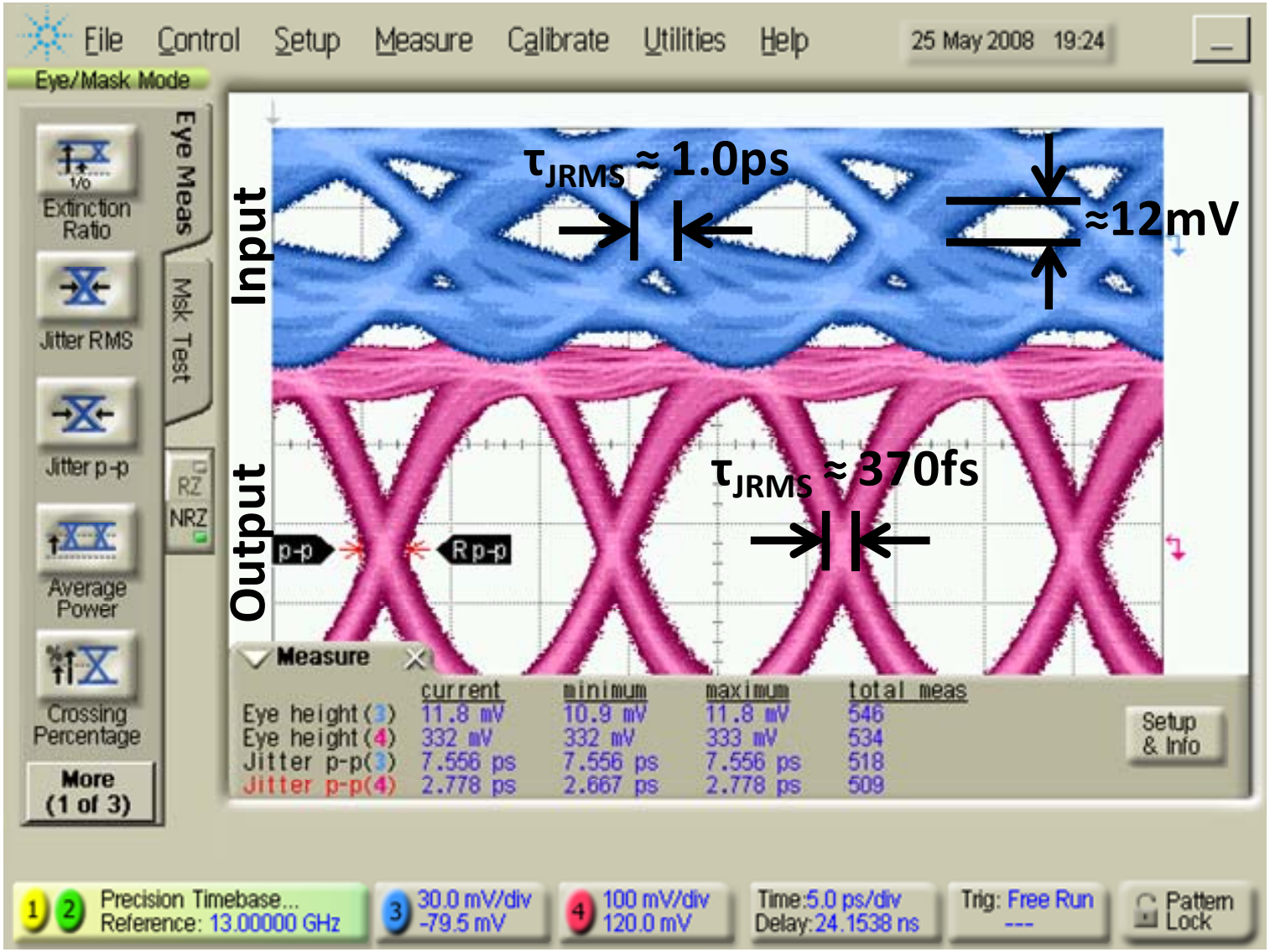


- Input eye amplitude is 40mV$_{pp}$, single-ended

Pattern Verification: 75Gb/s

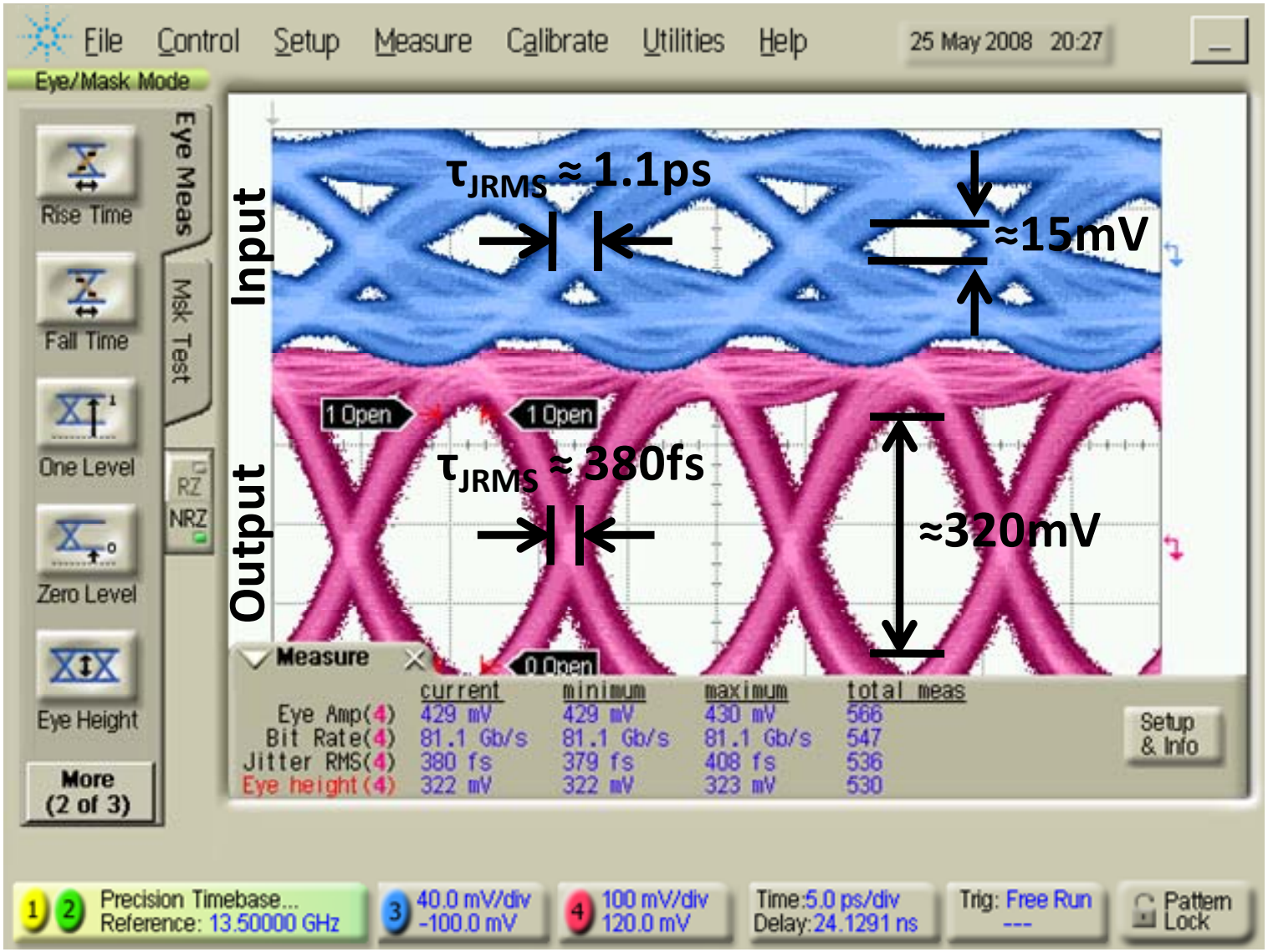


Measurement Results: 78Gb/s



- Input eye amplitude is 60mV$_{pp}$, single-ended

Measurement Results: 81Gb/s



- Input eye amplitude is 80mV$_{pp}$, single-ended

Pattern Verification: 81Gb/s

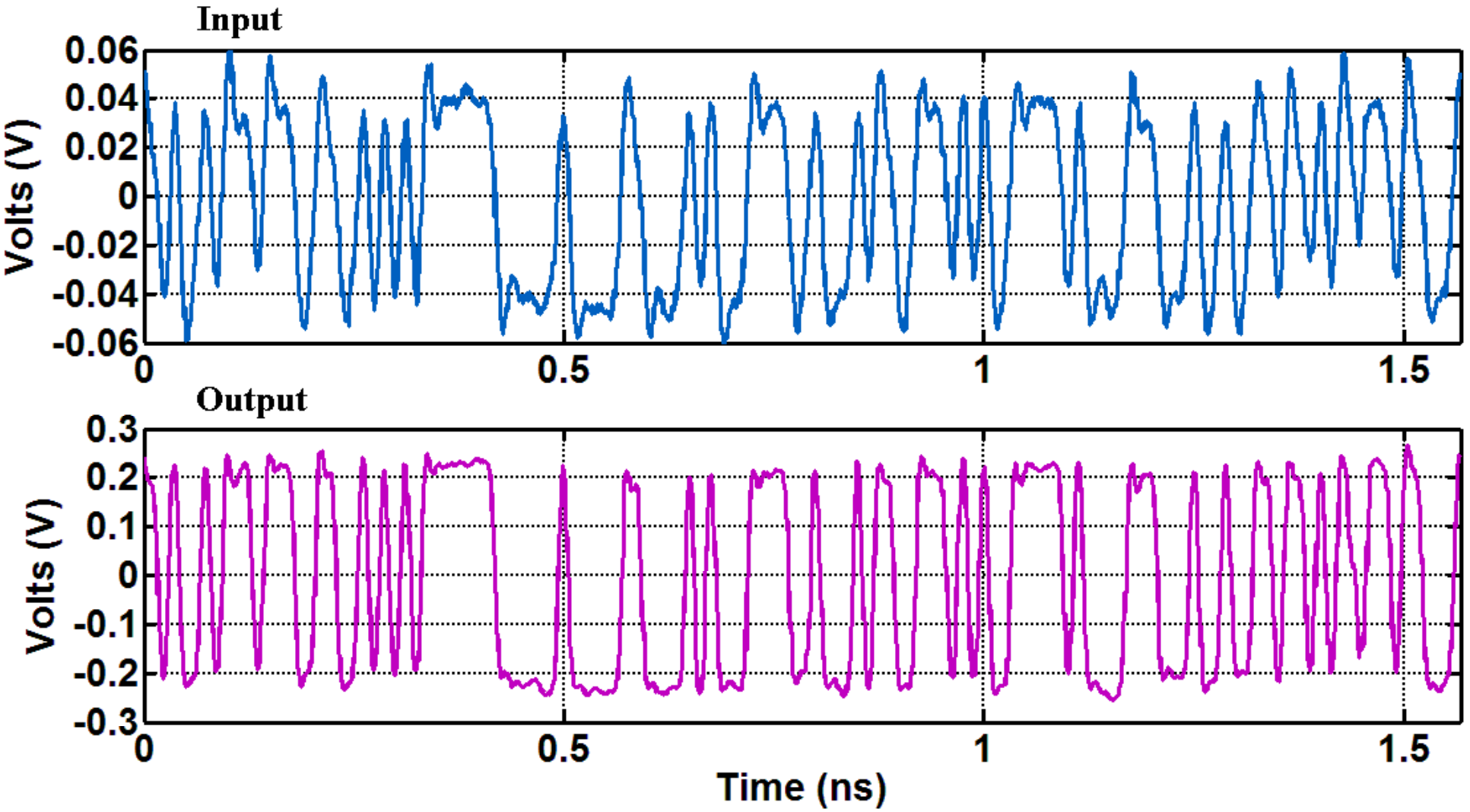


Table of Comparison

Ref.	Technology	Rate (Gb/s)	Supply (V)	P_{LATCH} (mW)	P_{Total} (mW)
[2]	InP HEMT *f_T = 245GHz*	80	-5.7	N/A	1200
[3]	SiGe BiCMOS *f_T = 150GHz*	48	2.5	23	288
[4]	90nm CMOS Process *f_T = 120GHz*	40	1.2	10.8	130
This Work	***65nm GPLP CMOS Process*** ***f_T = 170GHz***	***81***	***1.2***	***9.6***	***200***

Conclusions

- Fastest TIALA-retimer in any technology, operating at 81Gb/s
  - Latch power consumption is 9.6mW
  - TIA FoM is 118.5µW/Gb/s in differential operation

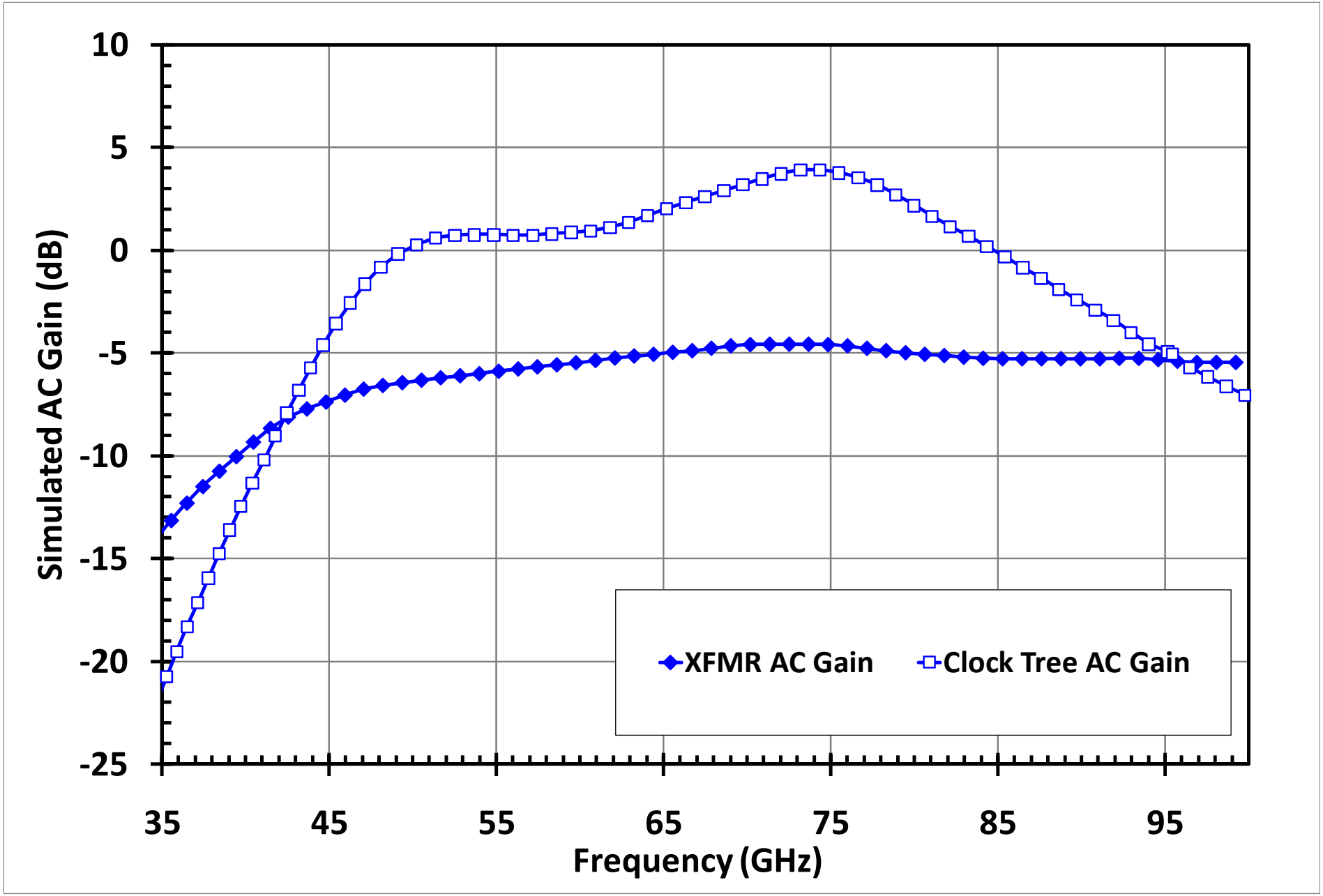
- Combination of LVT, SVT and HVT CMOS from 1.2V supply
- Low voltage CMOS nanoscale topologies
- Optimized transistor layouts and compact latch layout
- Combining low-noise, broadband CMOS TIA and high gain LA
- Optimized transistor sizing and biasing
- Series-shunt peaking techniques

Acknowledgments

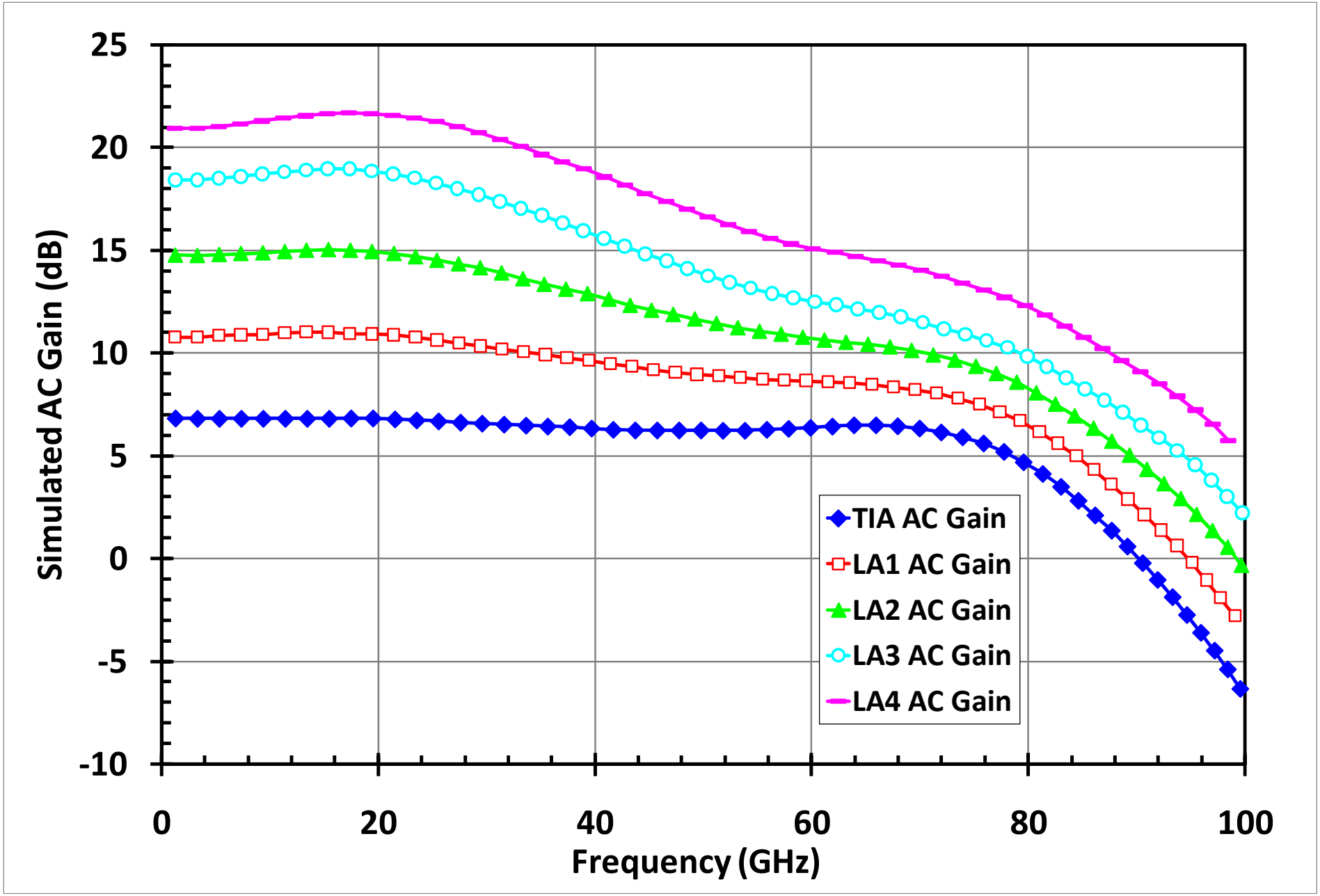
- We wish to acknowledge Nortel for funding and chip fabrication

Backup Slides

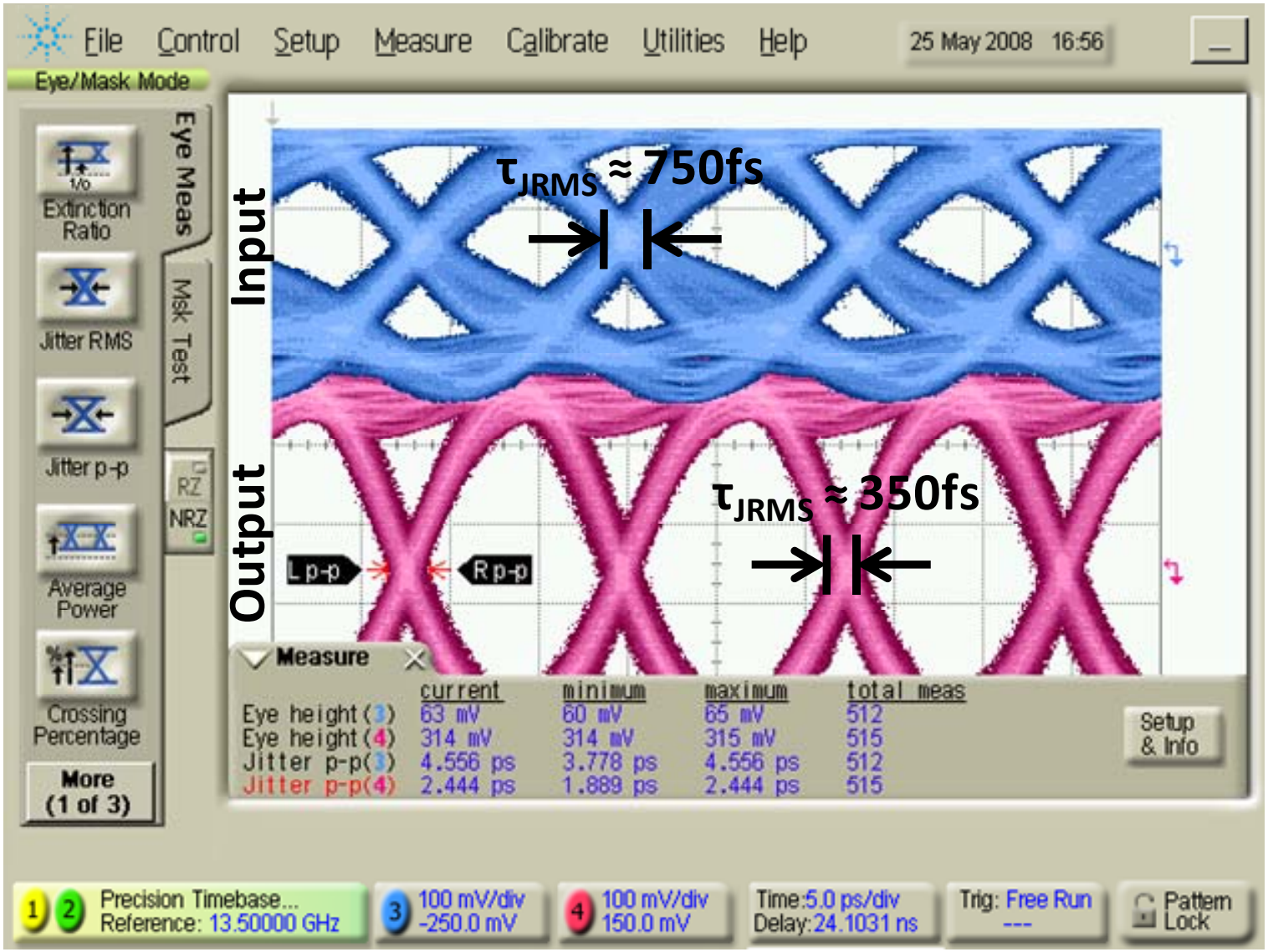
Simulated Clock Tree (Single-ended)



Simulated TIALA AC Response



Measurement Results: 81Gb/s



- Input eye amplitude is ~ 300mV$_{pp}$, single-ended