A Methodology for Accurate DFE Characterization

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***Abstract* — A simulation methodology to accurately characterize DFEs is introduced. The methodology relies upon a few short simulations with carefully contrived input waveforms to extract the DFE's effective response in situ capturing all non-linearities and speed limitations in the feedback circuits. The method is applied to a conventional 1-tap DFE and an infinite-impulse response (IIR) DFE. Measurement results from an IIR DFE in 65 nm CMOS technology verify the methodology.**

I. Introduction

Conventional approaches to DFE characterization are either not accurate or entail prohibitively long simulations. For example, to ensure proper settling of the feedback loop one may verify the delay of each subcircuit [1]. Alternatively, the complete DFE may be simulated with random input data while varying the channel ISI and observing output BER. However, such simulations are generally prohibitive, especially for post-layout extracted netlists. Here, a simulation methodology is described to rapidly and accurately quantify a DFE's nonidealities thus allowing for proper verification of a design, and for the construction of a behavioral DFE model that captures the nonidealities. This methodology is particularly important for several recently-researched unconventional DFE architectures whose timing requirements and effective tap weights are not obvious. For instance [2]–[5] do not use conventional summing nodes making it difficult to observe the true feedback signals.

The methodology presented here observes the input-referred decision-threshold of the entire DFE circuit using a series of relatively short transient simulations with carefully contrived input baud-rate pulse sequences. The timing and amplitude of the input pulses are swept thereby capturing the dependence of the decision threshold upon clock timing, and upon signal amplitudes. Since the simulations are performed on the full DFE circuit, they capture all nonidealities including layout parasitics if extracted netlists are used.

II. Methodoloy and Example 1-Tap DFE

Fig. 1 shows a simplified block diagram of a typical binary 1-tap FIR DFE. The input signal goes through a summer to a flip-flop. The bandwidth limitations of the summer and the finite sampling aperture of the flip-flop are captured by the lowpass filter (LPF) at the flip-flop input.[1] A typical CMOS regenerative latch has a delay that is a strong function of its input amplitude. This delay, and any incurred in the remainder of the feedback path, are included in a clock-to-Q delay modeled in the flip-flop. The flip-flop output proceeds through feedback circuits which may exhibit non-linearities. When the flip-flop fully settles, the non-linearity in the model feeds binary ± 1 signals back to the summer through the nominal tap weight A_{FB}. However, at speeds where the latch does not fully settle, the non-linearity may provide a smaller feedback signal to the summer, thus making the decision threshold dependent upon the settling behavior of the loop.

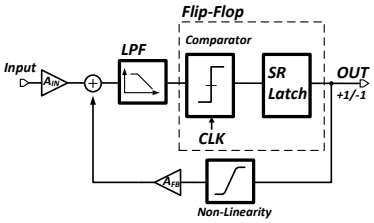


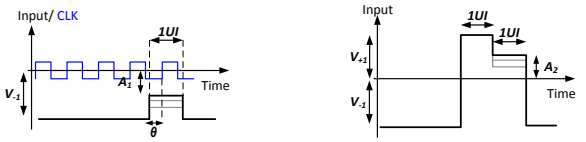
Fig. 1: A model of a conventional 1-tap DFE.

We first consider an exemplar implementation in 65 nm CMOS. A double-tail latch [6] is followed by an SR-latch for the flip-flop. Two parallel differential realize current-mode summing of the input and feedback. The summing node has a first-order lowpass response with 9 GHz bandwidth (τ=17ps). The latch and following SR-latch have a combined 50%-50% simulated clock-to-Q of 40-70 ps depending upon the differential latch input. The gain from the input to the summing node is 0.25V/V.

To characterize the behavior of the DFE for each particular setting (i.e. gain, tap weight, etc.) three simulations are required: a) single pulse test; b) double pulse test; and c) sensitivity test. The tests should be repeated at every DFE setting of interest.

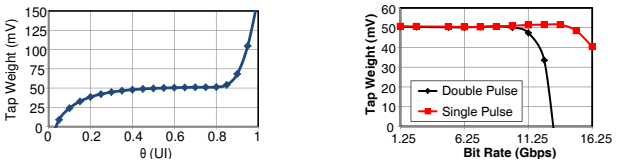
a) single pulse test: In this test a lone "+1" bit is applied after a long period of "-1" bits. The amplitude of the "-1" bits (V_{-1} in Fig. 2a) is chosen large enough so that the latch completely regenerates at the target data rate. The amplitude of the lone "+1" bit (A_1 in Fig. 2a) is swept to find the decision threshold, being the minimum value of A_1 for which the DFE output is positive. This value of A_1 is

[1] If the LPF responses for the input and feedback paths are different, this may be captured by additional pre-filters on the summing node inputs.



(a) (b)

Fig. 2: (a) Single pulse test waveforms. b) Double pulse test waveform.



(a) (b)

Fig. 3: a) DFE tap weight for different clock phases (θ) at 10 Gbps. b) Maximum and minimum input referred feedback from single and double pulse tests at different bit rates.

equal to the feedback signal gain, $\pm A_{FB}$, in our model and therefore represents the input-referred effective tap weight of the DFE under this condition. The timing requirements of the DFE are found by repeating this simulation with varying clock phase, θ, as in Fig. 3a. Note that for a clock phase $0.3 < \theta < 0.8$ UI, the feedback signal settles and the input-referred decision threshold is 50 mV, but outside that range a different effective tap weight is evident. Hence, Fig. 3a reveals the phase relationship between clock and data required for the DFE to operate properly. Moreover, any dependence of DFE tap weight upon clock phase indicates that jitter is converted to an equivalent noise at the DFE input with a gain given by the slope of the plot in Fig. 3a.

In this test, the output has not changed for a long period of time prior to the lone "+1" bit. Hence, we expect the feedback signal to settle to its strongest possible value. When the input data preceding the lone "+1" bit is random, the feedback signal may not completely settle. The resultant change in the DFE's decision threshold is observed in the "double pulse test".

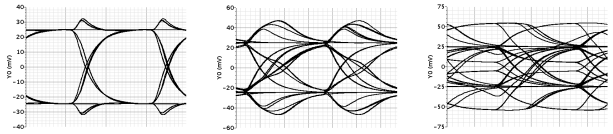
b) double pulse test: This test determines the DFE's decision threshold when the feedback loop is given only 1 UI to settle and is therefore expected to provide the weakest feedback signal. First, a long stream of strong "-1" input bits (amplitude V_{-1} as before) is applied to the input. Then a lone strong "+1" pulse 1 UI in duration (amplitude V_{+1} as shown in Fig. 2b) is applied to flip the output of the DFE. This strong "+1" is intended to ensure this lone bit will toggle the decision circuit. Following this, the next pulse is applied with amplitude A_2 swept to identify the maximum value that causes the comparator output to flip back to "-1". In this case the feedback loop has had the least amount of time to settle and we expect to observe the weakest possible feedback signal.

Fig. 3b plots the input referred decision threshold of the exemplar DFE obtained from the single and double pulse tests as a function of the bit rate. The sampling phase θ is kept constant at moderate values (around 0.5 UI) throughout. At low bit rates, the effective tap weight is equal for the two cases. As the duration of one UI decreases, the time available for the feedback loop to settle in the double pulse test is reduced. Hence, the feedback signal deviates from the single pulse value beyond 11 Gbps. The decision threshold in the single pulse test remains the same up to about 14 Gbps, beyond which the summer output does not settle in response to the input pulse prior to the coming clock edge. For a random input sequences the decision threshold lies somewhere between these two curves depending on the specific s equence of preceding bits.

The simple exemplar DFE allows the methodology to be corroborated by other simulations. Fig. 4 shows the voltage at the summing node at different bit rates to confirm the modeling of Fig. 2 and Fig. 3. A PRBS7 pattern with 100 mV amplitude is passed through a $1+0.5z^{-1}$ response. At 10Gbps the results of the single and double pulse tests coincide, and Fig. 4a shows the DFE fully cancels the post-cursor ISI. However, at 12 Gbps the double pulse test revealed a reduced effective feedback signal of 42 mV. Fig. 4b shows this results in incomplete cancellation of the ISI. At 14 Gbps the single pulse tap weights remains at 50 mV but the double pulse test result is reduced to -40 mV. Hence, the DFE is actually doubling ISI for some bit patterns, deteriorating the eye diagram (Fig. 4c).

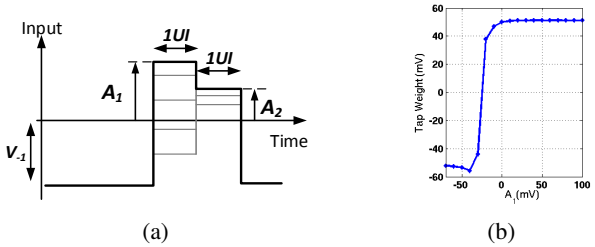
Although this simple circuit has an explicit summing node to illustrate these effects, other more complicated DFE circuits have no node voltages or branch currents that faithfully represent the signals of interest. In such cases, the methodology described here becomes invaluable in establishing the performance of a DFE using a short sequence of transient simulations that can be repeated during design and verification.

c) sensitivity test: Since the clock-to-Q delay of a flip-flop depends upon the signal amplitude at its input, small input amplitudes can result in incomplete settling of the feedback loop. Hence, the DFE feedback signal is somewhat dependent upon the amplitude at the latch input. Such behavior is reminiscent of an IIR filter rather than a true DFE, and can be characterized by a series of double pulse tests to find A_{FB} for different amplitudes of the first pulse, A_1 in Fig. 5a.



(a) (b) (c)

Fig. 4: Simulation of 1-tap DFE summer output with PRBS7 100mV amplitude input after $1+0.5z^{-1}$ channel: (a) 10 Gbps; (b) 12 Gbps; (c) 14Gbps.



(a) (b)

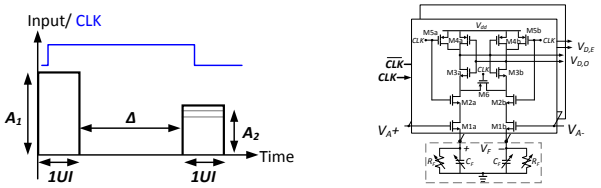
Fig. 5: (a) DFE sensitivity test waveform. (b) Tap weight as function of DFE input signal amplitude.

Fig. 5b shows the effective tap weight of our exemplar DFE for different values of A_1 at 10 Gbps. For very small input amplitudes ($A_1 < -50$ mV) the feedback is negative and therefore degrades the eye at the summing node. For $-50\text{mV} < A_1 < 0\text{mV}$, the DFE improves the eye opening, but the feedback signal becomes amplitude-dependent. For $A_1 > 40$ mV, the feedback signal becomes signal independent as expected in a DFE. This test may be particularly pertinent for "soft" DFEs such as [7] where an input eye openings larger than 70 mV was shown to be required.

III. Application to IIR DFE

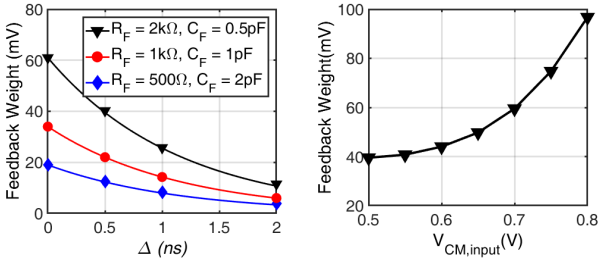
This section extends the simulation methodology to an IIR DFE where typically the IIR feedback waveform is continuously varying; since the decision circuit is sensitive to it over a finite window of time, the IIR response can't be inferred by simply looking at the waveform. To see how the DFE threshold varies over time, the double pulse and sensitivity test waveforms must be generalized to introduce a delay, Δ between the first and second pulse, as shown in Fig. 6a. By sweeping Δ in 1-UI increments, the DFE's IIR response may be found.

An example of an unconventional IIR-DFE is illustrated in Fig. 6b [5] wherein the differential voltage V_F provides the feedback signal, and DFE subtraction is performed by the input transistors M_1 whose drain current is related to V_{GS}. However, V_F is not precisely equal to the DFE's effective IIR response. Fig. 7a shows the DFE response in a 65 nm CMOS implementation plotted versus Δ obtained



(a) (b)

Fig. 6: (a) The input applied to the DFE to determine its feedback signal though time. b) IIR DFE schematic [5].



(a) (b)

Fig. 7: Extracted IIR-DFE responses at 20 Gbps: (a) For three different values of R_F, C_F for $V_{CM,input} = 0.7$ V; (b) response at $\Delta = 0$ for $R_F = 1k\Omega$, $C_F = 1$ pF versus input common-mode level.

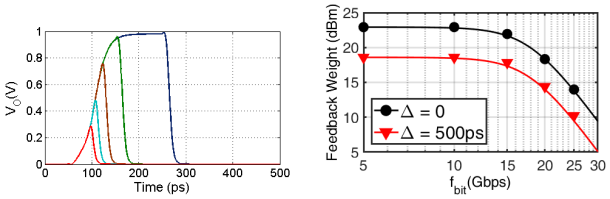
by keeping A_1 fixed and large and sweeping A_2 to find a value that trips the latch. It is also possible to vary A_1 in this test to show how the IIR response depends upon the input amplitude to the latch. The responses for three different values of $R_F C_F$ are shown. As expected, the responses are first-order lowpass with amplitudes decreasing as C_F is increased.

The methodology can also capture and quantify subtle effects. For example, as the common-mode input level rises, input transistors M_1 go deeper into triode, making their drain-source resistance a weaker function of $V_{GS,1}$. This in turn reduces the effect of V_A on the output decision. The resulting increase in effective tap weight is captured by the modeling and plotted in Fig. 7b.

Proper functionality of this IIR DFE requires full settling at the latch output to ensure complete charge transfer from the output nodes onto C_F. Fig. 8a shows the output waveforms as f_{bit} increases. At high f_{bit}, the output nodes cannot fully settle, as demonstrated in Fig. 8b which shows the effective IIR DFE decision threshold at $\Delta = 0$ and 500 ps as functions of f_{bit}. Both curves remain constant up to about $f_{bit} = 15$ Gbps.

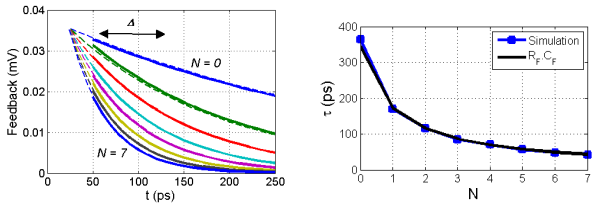
A. Simulation of the Prototype IIR DFE

The resistor R_F in Fig. 6b is implemented by activating (N+1) 360Ω resistors in parallel using NMOS switches,



(a) (b)

Fig. 8: (a)Output of the IIR DFE as f_{bit} increases (5G, 10G, 15G, 20G, and 25GHz). (b) DFE tap weight as functions of f_{bit}. Both curves show $f_{3dB} = 18GHz$ The solid lines are the result of fitting the simulated points (markers) to $A/(1 + j(f/f_P)^3)$.



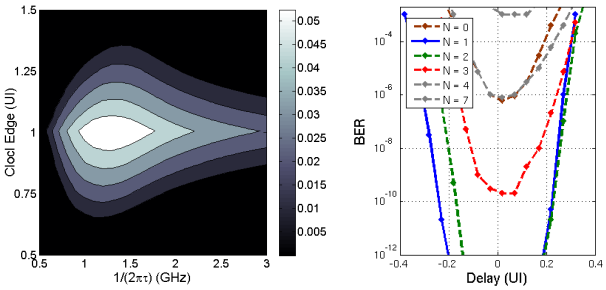
(a) (b)

Fig. 9: (a) Extracted effective feedback signals with $C_F = 1$ pF and $R_F = 360/(N + 1)$, $N = 0 \ldots 7$ (solid) and best fit single time constant responses (dashed). (b) Time-constants, τ, of the fit single time constant responses (blue markers) and the corresponding products $R_F C_F$ (black).

$0 \leq N \leq 7$. The input referred feedback of the IIR-DFE is simulated as in Section III and plotted in Fig. 9a for different values of N (hence R_F) keeping $C_F = 1pF$ at 20 Gbps. Note that extrapolating the feedback signals back in time showns an intersection at the point where all charge from the latch outputs has been transferred to C_F, after which V_F decays with first-order time-constants τ. Fig. 9b shows values of τ extracted from the responses in Fig. 9a along with the corresponding known values of the product $R_F C_F$, thus confirming the IIR-DFE time constant is determined predominantly by $R_F C_F$.

B. Measurement of the Prototype IIR-DFE

The IIR DFE is tested with 0.2 V input amplitude, $C_F = 1$ pF, and R_F swept to change $f_F = 1/(2\pi\tau)$. The simulation methodology is applied to an extracted netlist and combined with a peak distortion analysis [8] resulting in Fig. 10a, suggesting $1/(2\pi\tau) = 1.3$ GHz is best. This differs from the bandwidth of the ISI response (2 GHz) because only R_F is swept, so it is not possible to independently adjust the IIR tap gain and time-constant. In measurement, R_F is swept: $360/(N + 1)$ Ω, (N = 0,...,7) and the widest bathtub opening observed at N = 1,2 in Fig. 10b corresponding to f_F = 1.1GHz, 1.65GHz, in agreement with the modeling result.



(a) (b)

Fig. 10: Simulation and measurement of a prototype 65-nm CMOS IIR-DFE at 17 Gbps with 2-GHz first-order lowpass ISI. (a) Vertical eye opening from a peak-distortion analysis as a function of clock phase and extracted IIR-DFE time constant. (b) Measured bathtub curves with PRBS7 input.

IV. Conclusion

A simulation methodology to accurately characterize DFEs was introduced. The methodology relies upon a few short simulations with carefully contrived input waveforms to extract the DFE's effective response in situ, allowing it to capture of all non-linearities and speed limitations in the feedback circuits. The simulation results are validated by measurements of an IIR-DFE in 65nm CMOS.

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