

# Welcome to

# DESIGNCON<sup>®</sup> 2020

25<sup>TH</sup> ANNIVERSARY

WHERE THE CHIP MEETS THE BOARD

Conference

January 28 - 30, 2020

Expo

January 29 - 30, 2020

Santa Clara Convention Center



# A Statistical Modeling Approach for FEC-Encoded High-Speed Wireline Links

Ming Yang, University of Toronto

Shayan Shahramian, Huawei Canada

Hossein Shakiba, Huawei Canada

Henry Wong, Huawei Canada

Peter Krotnev, Huawei Canada

Anthony Chan Carusone, University of Toronto



# Outline

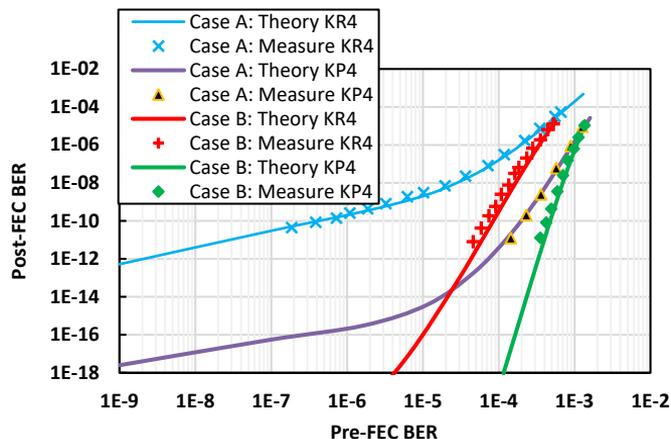
1. **Motivation**
2. **Statistical Model for BER Estimation**
  - a. Modeling DFE Error Propagation in 2-PAM
  - b. 4-PAM Statistical Model
  - c. Post-FEC BER Estimation for Non-Binary Linear Block Codes
3. **Common Coding Techniques in Wireline Links**
  - a. Interleaved FEC Code
  - b. MOD4 Precoding
4. **Modeling Other Type of Noise Sources**
  - a. Residual ISI
  - b. Jitter
5. **Experimental Verification**
6. **Conclusion**



# Motivation

- We want to confirm post-FEC BERs in simulation down to  $10^{-15} - 10^{-21}$  quickly and accurately
- To be accurate, the method must capture the statistics of errors
- Bit or symbol error occurrences are correlated; they sometimes occur in bursts due to DFE error propagation, low-frequency clock jitter, supply noise, etc.
- Error statistics strongly affect the performance of FEC

Example: Cases A & B are two different channels and DFE tap weights resulting in very different post-FEC BER for the same pre-FEC BER



# Signal Integrity Analysis Paradigms

## Monte Carlo

- *Simulate with random data, random noise, and track the state of the transmitter, channel, and receiver, including FEC encoder/decoder, as the simulation progresses*
  - Captures how “memory” in the link ultimately effects the error statistics
  - Impractical to capture post-FEC BER of  $10^{-15}$  –  $10^{-21}$

## Statistical

- *Determine the probability of pre-FEC errors*
  - Typical techniques consider ISI and other statistical correlations in the transceiver and channel
  - Accurate even for low probabilities
  - **The results generally do not capture the time-correlation of error events**
- *Apply the FEC-limit paradigm*
  - e.g. using a particular code, a pre-FEC BER of  $10^{-5}$  produces a post-FEC BER of  $10^{-18}$
  - **Does not account for the fact that FEC performance depends on the time-correlation of errors**



# This Work

## This Work

- *This work seeks Statistical methods to address these two shortcomings:*

- Capture time-correlation of error events (focusing on DFE errors)

- Capture how those error statistics impact FEC performance



## Statistical

- *Determine the probability of pre-FEC errors*
  - Typical techniques consider ISI and other statistical correlations in the transceiver and channel
  - Accurate even for low probabilities
  - **The results generally do not capture the time-correlation of error events**
- *Apply the FEC-limit paradigm*
  - e.g. using a particular code, a pre-FEC BER of  $10^{-5}$  produces a post-FEC BER of  $10^{-18}$
  - **Does not account for the fact that FEC performance depends on the time-correlation of errors**



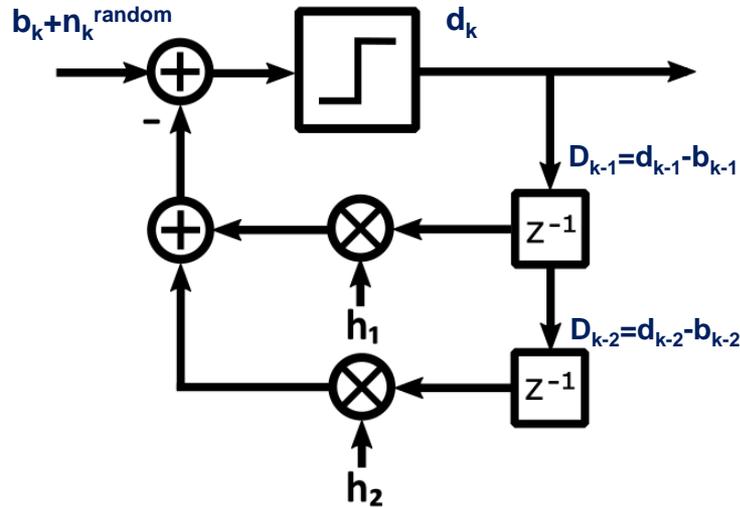
# Outline

1. Motivation
2. Statistical Model for BER Estimation
  - a. Modeling DFE Error Propagation in 2-PAM
  - b. 4-PAM Statistical Model
  - c. Post-FEC BER Estimation for Non-Binary Linear Block Codes
3. Common Coding Techniques in Wireline Links
  - a. Interleaved FEC Code
  - b. MOD4 Precoding
4. Modeling Other Type of Noise Sources
  - a. Residual ISI
  - b. Jitter
5. Experimental Verification
6. Conclusion



# Markov Model for DFE Error Propagation

- 2-Tap DFE Example

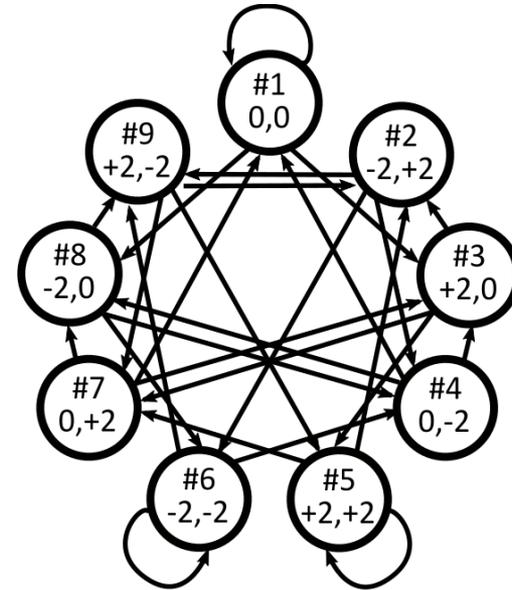


2-tap DFE, 2PAM [1 -1]

Error distance:  $D_k \in [2, 0, -2]$

9 possible states: (0,2) (0,-2) (2,0) (-2,0)

(2,2) (2,-2) (-2,2) (-2,-2) (0,0)

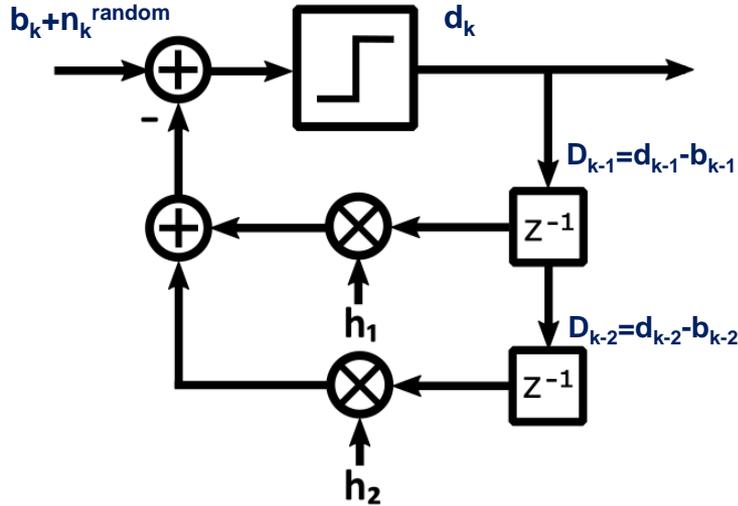


States are defined as possible combinations of error distance  $(D_{k-1}, D_{k-2})$



# Markov Model for DFE Error Propagation

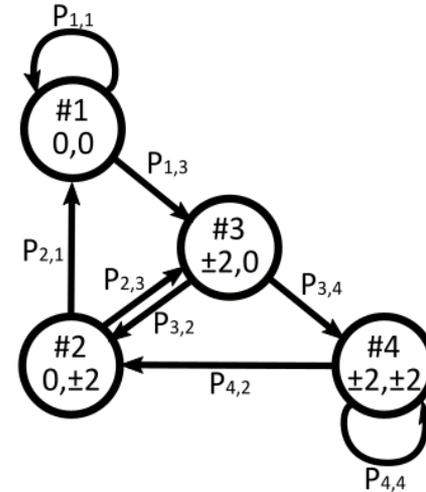
- Simplified Model using State Lumping



2-tap DFE

4 simplified states:

(0,0) (0, ±2) (±2,0) (±2, ±2)



- Reduced complexity due to symmetry of the situation
- Fine if we don't care about the polarity of the bit error

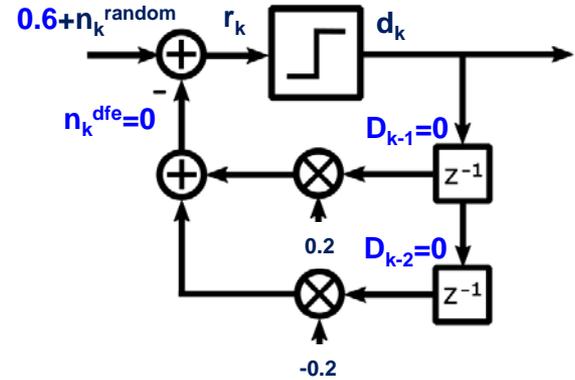
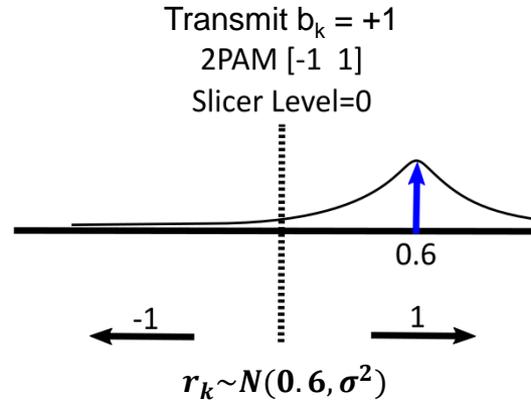
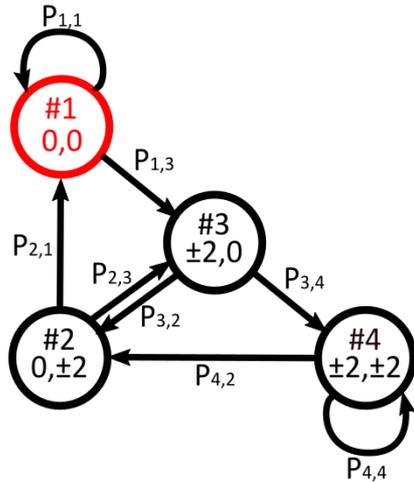


# Markov Model – State Transition Probability

Use conventional statistical analysis to find the branch probabilities,  $p_{ij}$

Example: Previous decisions were all correct

⇒ Current state #1: (0,0)



Channel: [0.6 0.2 -0.2]

$b_k$  Transmit: [ 1 -1 -1 ]

$d_k$  Detect: [ X -1 -1 ]

$n^{DFE=0}$

Markov chain state transitions  
(2-tap DFE)

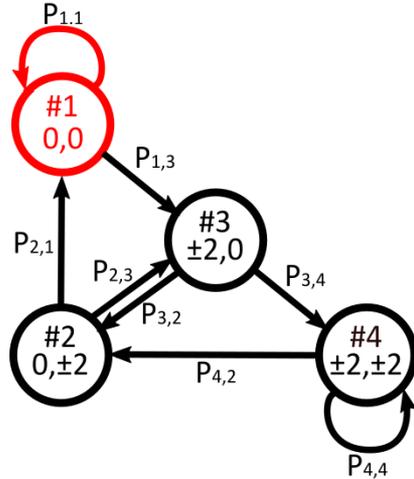


# Markov Model – State Transition Probability

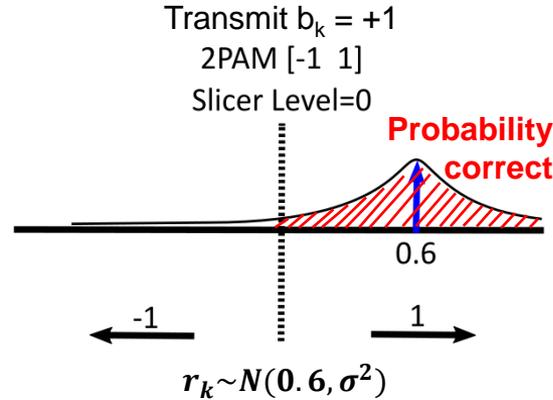
Use conventional statistical analysis to find the branch probabilities,  $p_{ij}$

Example: Previous decisions were all correct

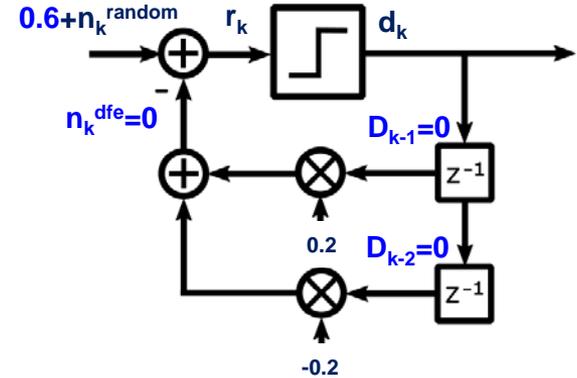
⇒ Current state #1: (0,0)



Markov chain state transitions  
(2-tap DFE)



⇒ Must also consider what happens when we transmit  $b_k = -1$  to calculate  $p_{11}$



Channel: [0.6 0.2 -0.2]

$b_k$  Transmit: [ 1 -1 -1 ]

$d_k$  Detect: [ 1 -1 -1 ]

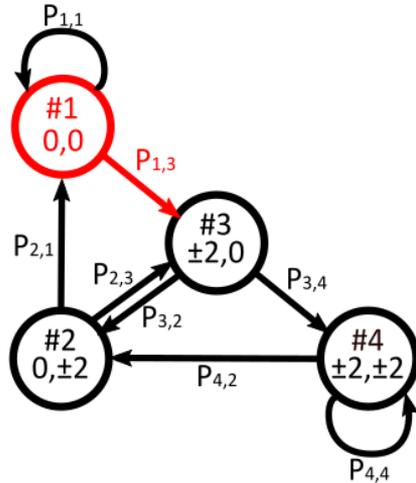
$n^{DFE}=0$

# Markov Model – State Transition Probability

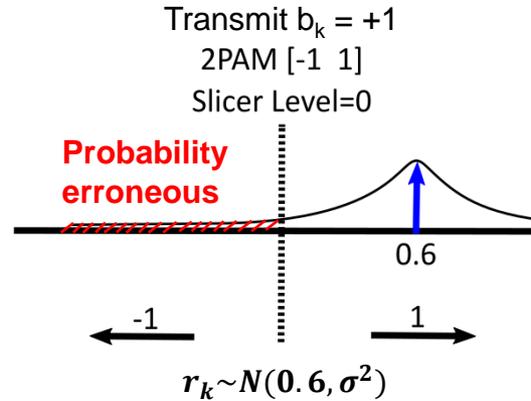
Use conventional statistical analysis to find the branch probabilities,  $p_{ij}$

Example: Previous decisions were all correct

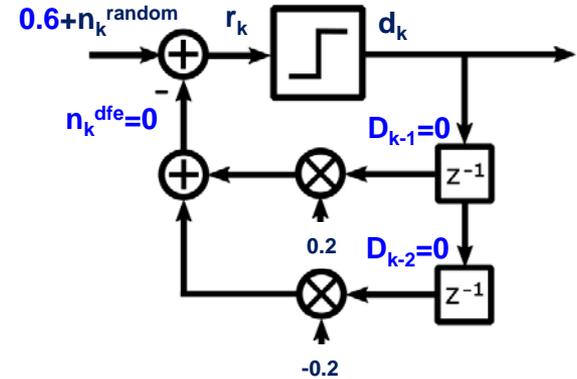
⇒ Current state #1: (0,0)



Markov chain state transitions  
(2-tap DFE)



⇒ Must also consider what happens when we transmit  $b_k = -1$  to calculate  $p_{13}$



Channel: [0.6 0.2 -0.2]

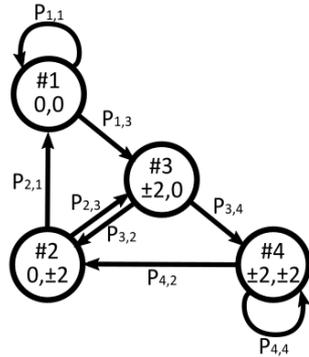
$b_k$  Transmit: [ 1 -1 -1 ]

$d_k$  Detect: [ -1 -1 -1 ]

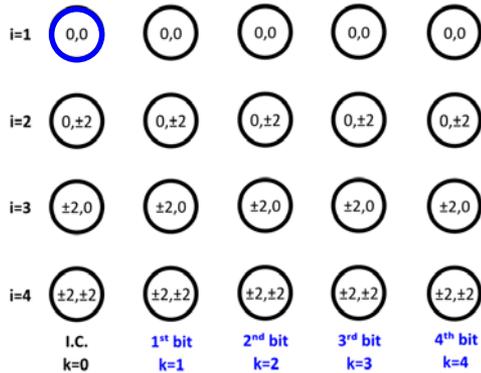
$n^{\text{DFE}}=0$

# Finding Error Pattern Probability in PAM Trellis

- Example: Finding the probability of a specified error pattern



Transmit	1	1	-1	1	-1
Detect	1	-1	1	1	-1
Error	0	1	1	0	0
Error State	1 → 3 → 4 → 2 → 1				



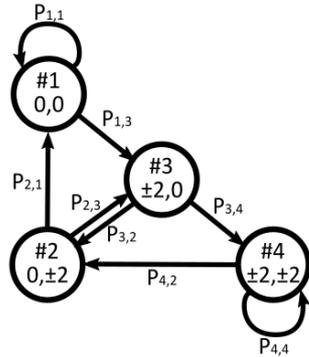
- Error Patter Probability:  
 $P_{13421} = P(1) \cdot P_{1,3} \cdot P_{3,4} \cdot P_{4,2} \cdot P_{2,1}$

Probability we are initially in state #1

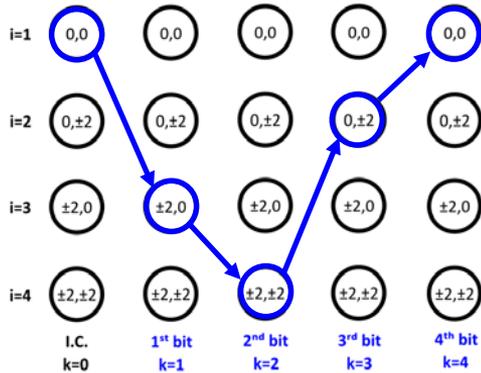


# Finding Error Pattern Probability in PAM Trellis

- Example: Finding the probability of a specified error pattern



Transmit	1	1	-1	1	-1
Detect	1	-1	1	1	-1
Error	0	1	1	0	0
Error State	$\boxed{1 \rightarrow 3} \rightarrow 4 \rightarrow 2 \rightarrow 1$				



- Error Patter Probability:  
 $P_{13421} = P(1) \cdot P_{1,3} \cdot P_{3,4} \cdot P_{4,2} \cdot P_{2,1}$

Probability we are initially in state #1



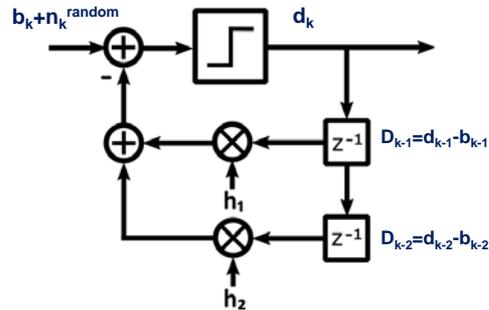
# Outline

1. Motivation
2. Statistical Model for BER Estimation
  - a. Modeling DFE Error Propagation in 2-PAM
  - b. 4-PAM Statistical Model**
  - c. Post-FEC BER Estimation for Non-Binary Linear Block Codes
3. Common Coding Techniques in Wireline Links
  - a. Interleaved FEC Code
  - b. MOD4 Precoding
4. Modeling Other Type of Noise Sources
  - a. Residual ISI
  - b. Jitter
5. Experimental Verification
6. Conclusion

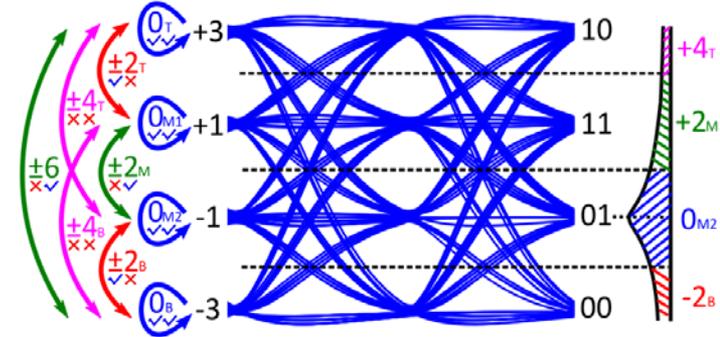


# 4-PAM Markov Model

- All states having the same error magnitude are aggregated together by applying weak lumpability,  $D_k \in \{0, \pm 2, \pm 4, \pm 6\}$
- More DFE error states are needed in the Markov Model

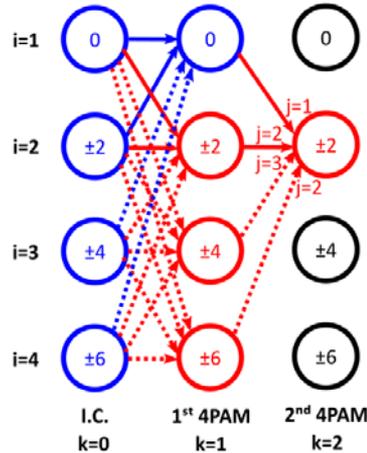


A receiver eye diagram indicating all possible symbol-detection outcomes for a link communicating Grey-coded 4-PAM symbols  $b_k \in \{\pm 3, \pm 1\}$

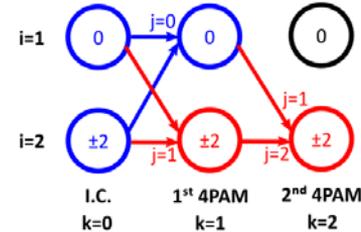


# 4-PAM Trellis Model

- $\pm 4$  and  $\pm 6$  events are unlikely at  $10^{-15}$  post-FEC BER



Trellis example of a 1-Tap DFE for a 4-bit codeword with all possible paths ending in state  $\pm 2$  ( $i=2$ )



Simplified trellis by ignoring all the dotted paths that have unlikely  $\pm 4$  and  $\pm 6$  error events

# Finding Pre-FEC BER

- **Over a sequence of  $n$  bits, the probability of:**

- 1 bit error is  $\Pr_n(1)$
- 2 bit errors is  $\Pr_n(2)$
- etc...

- **Then, we can calculate the BER over a  $n$ -bit codeword**

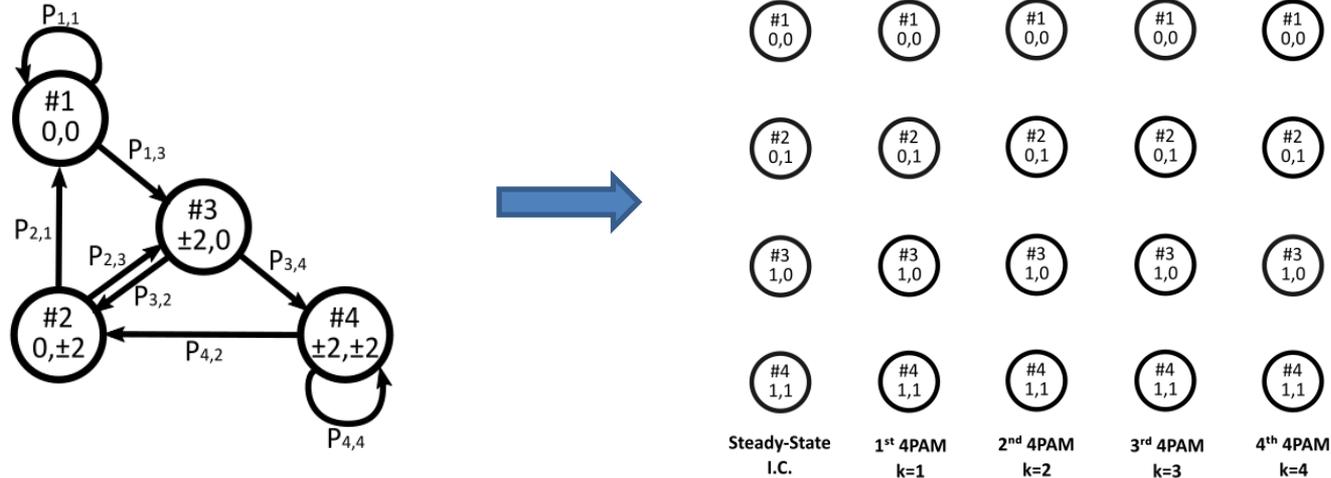
$$BER = \frac{1}{n} \sum_{j=1}^n j \cdot \Pr_n(j)$$

- **In general, for  $L$ -PAM and  $N$ -tap DFE, traversing a length- $n$  trellis exhaustively requires computations that are  $O(L^N L^n)$**



# Example of Traversing Trellis

- Example: 2-tap DFE, 8-bit codeword, 4PAM

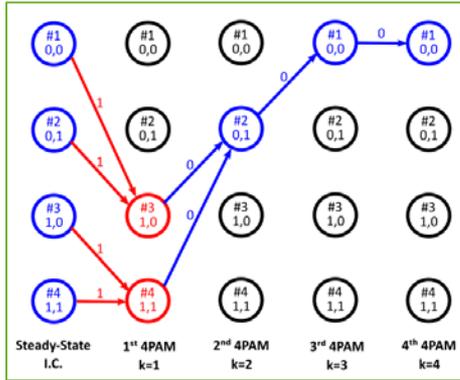


- Finding  $\Pr_n(1)$ , the probability of all trellis paths having exactly 1 bit error

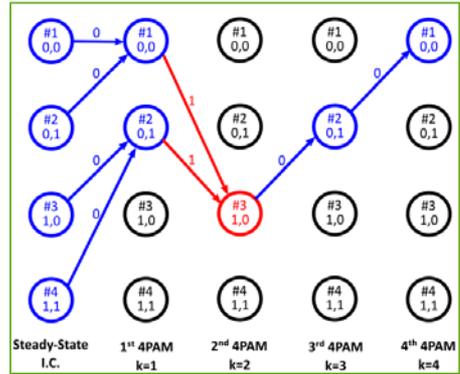


# Probability Model - Finding Pre-FEC BER

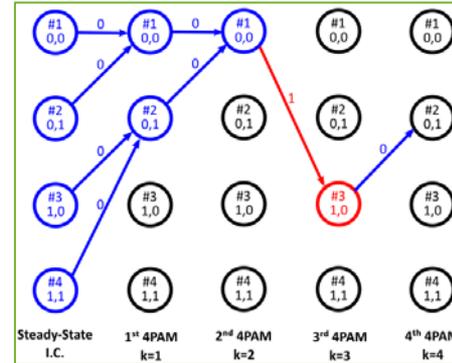
- Example: 2-tap DFE, 8-bit codeword, 4PAM



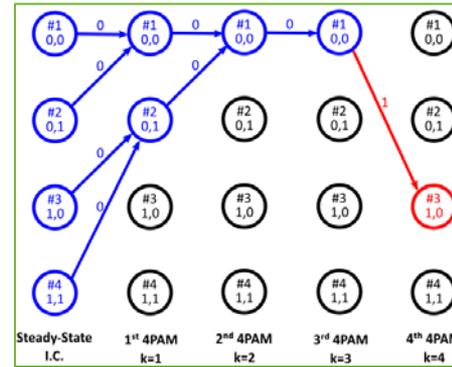
- Case 1: error at 1<sup>st</sup> stage
- $Pr_n(1) =$   
 $P_{13}P_{32}P_{21}P_{11} + P_{23}P_{32}P_{21}P_{11} +$   
 $P_{34}P_{42}P_{21}P_{11} + P_{44}P_{42}P_{21}P_{11}$



- Case 2: error at 2<sup>nd</sup> stage
- $Pr_n(1) =$   
 $P_{11}P_{13}P_{32}P_{21} + P_{21}P_{13}P_{32}P_{21} +$   
 $P_{32}P_{23}P_{32}P_{21} + P_{42}P_{23}P_{32}P_{21}$



- Case 3: error at 3<sup>rd</sup> stage
- $Pr_n(1) =$   
 $P_{11}P_{11}P_{13}P_{32} + P_{21}P_{11}P_{13}P_{32} +$   
 $P_{32}P_{21}P_{13}P_{32} + P_{42}P_{21}P_{13}P_{32}$



- Case 4: error at 4<sup>th</sup> stage
- $Pr_n(1) =$   
 $P_{11}P_{11}P_{11}P_{13} + P_{21}P_{11}P_{11}P_{13} +$   
 $P_{32}P_{21}P_{11}P_{13} + P_{42}P_{21}P_{11}P_{13}$



# Inefficiency of Exhaustive Computations

Case 1:  $Pr_n(1) = p_{13}p_{32}p_{21}p_{11} + p_{23}p_{32}p_{21}p_{11} + p_{34}p_{42}p_{21}p_{11} + p_{44}p_{42}p_{21}p_{11} +$   
Case 2:  $p_{11}p_{13}p_{32}p_{21} + p_{21}p_{13}p_{32}p_{21} + p_{32}p_{23}p_{32}p_{21} + p_{42}p_{23}p_{32}p_{21} +$   
Case 3:  $p_{11}p_{11}p_{13}p_{32} + p_{21}p_{11}p_{13}p_{32} + p_{32}p_{21}p_{13}p_{32} + p_{42}p_{21}p_{13}p_{32} +$   
Case 4:  $p_{11}p_{11}p_{11}p_{13} + p_{21}p_{11}p_{11}p_{13} + p_{32}p_{21}p_{11}p_{13} + p_{42}p_{21}p_{11}p_{13}$

- Computations required to repeat this for  $Pr_4(2)$ ,  $Pr_4(3)$ ,  $Pr_4(4)$  errors
- Pre-FEC BER =  $Pr_n(1) + 2 Pr_n(2) + 3 Pr_n(3) + 4 Pr_n(4)$
- Not practical to enumerate all error patterns for a long codeword
- Some multiplications are performed twice
- Trellis dynamic programming systematically stores these intermediate results so that the same multiplication is only performed once



# Outline

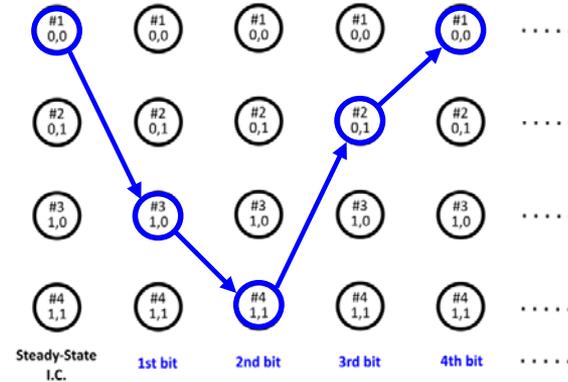
1. Motivation
2. Statistical Model for BER Estimation
  - a. Modeling DFE Error Propagation in 2-PAM
  - b. 4-PAM Statistical Model
  - c. **Post-FEC BER Estimation for Non-Binary Linear Block Codes**
3. Common Coding Techniques in Wireline Links
  - a. Interleaved FEC Code
  - b. MOD4 Precoding
4. Modeling Other Type of Noise Sources
  - a. Residual ISI
  - b. Jitter
5. Experimental Verification
6. Conclusion



# Finding Post-FEC BER of Long Block Codes

- **We wish to find the BER at the output of a FEC decoder operating on  $GF(2^m)$ ,  $m > 1$** 
  - e.g. many of the standard wireline codes are Reed Solomon codes of this type
- **Brute force approach would catalog all possible error patterns which are correctable**
- **Find the probability of these error patterns**

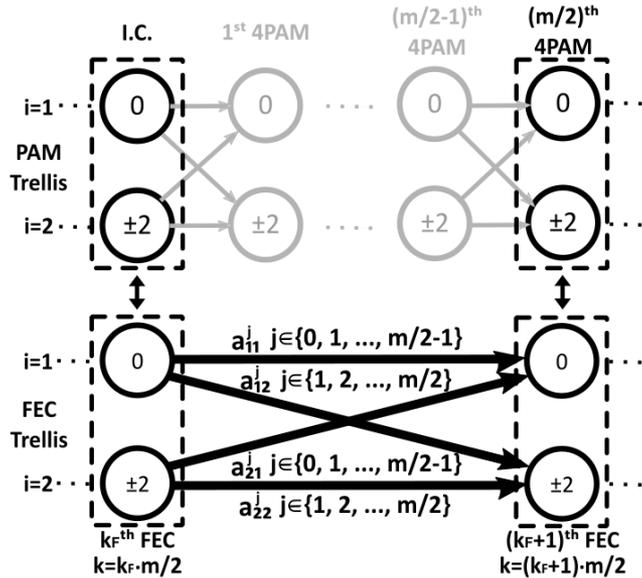
Example below corresponds to a 2-tap DFE;  
hence, 4-state PAM trellis



- **Example: RS(544, 514, 15) KP4 FEC on  $GF(2^{10})$** 
  - Each block is 5440 bits long
  - Can correct up to 15 FEC symbol errors
- **Number of trellis paths to compute is intractable**



# The “FEC Trellis”

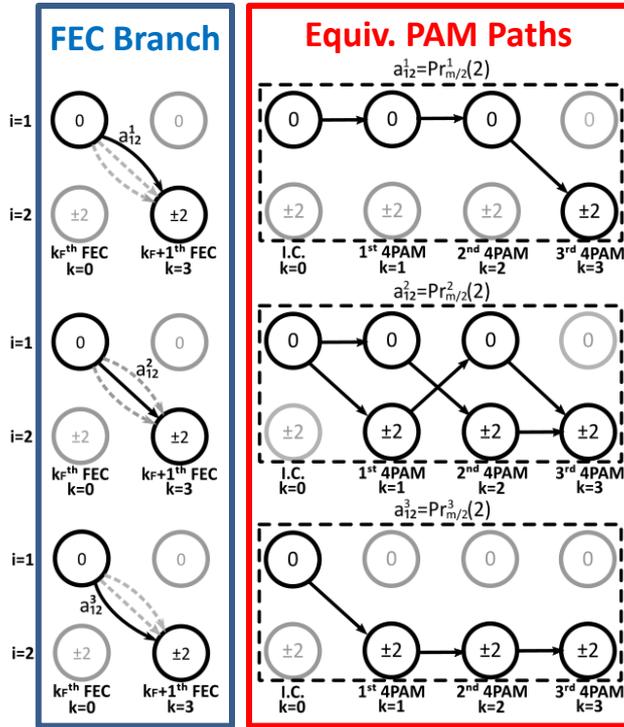


Example above: 1-tap DFE

- Construct a new trellis where each stage corresponds to an entire FEC symbol rather than a PAM symbol
  - “Time aggregation” of a Markov model
    - ✓ Much shorter “FEC Trellis”
- Branch probabilities in the FEC Trellis can be found by analysis of the short length- $m/2$  trellis above



# Finding Branch Probabilities in the FEC Trellis



Example above: 1-tap DFE,  $m = 6$

Thus, each FEC symbol is 3 4-PAM symbols

- The FEC trellis has a higher radix if we need to keep track of the number of pre-FEC bit errors

- Example:

$$a_{12}^1 = \Pr_{m/2}^1$$

≡ probability of going from state 1 (no error in DFE) to state 2 (error in DFE) traversing a FEC symbol (duration 3 PAM-4 symbols in this case) experiencing exactly one bit error

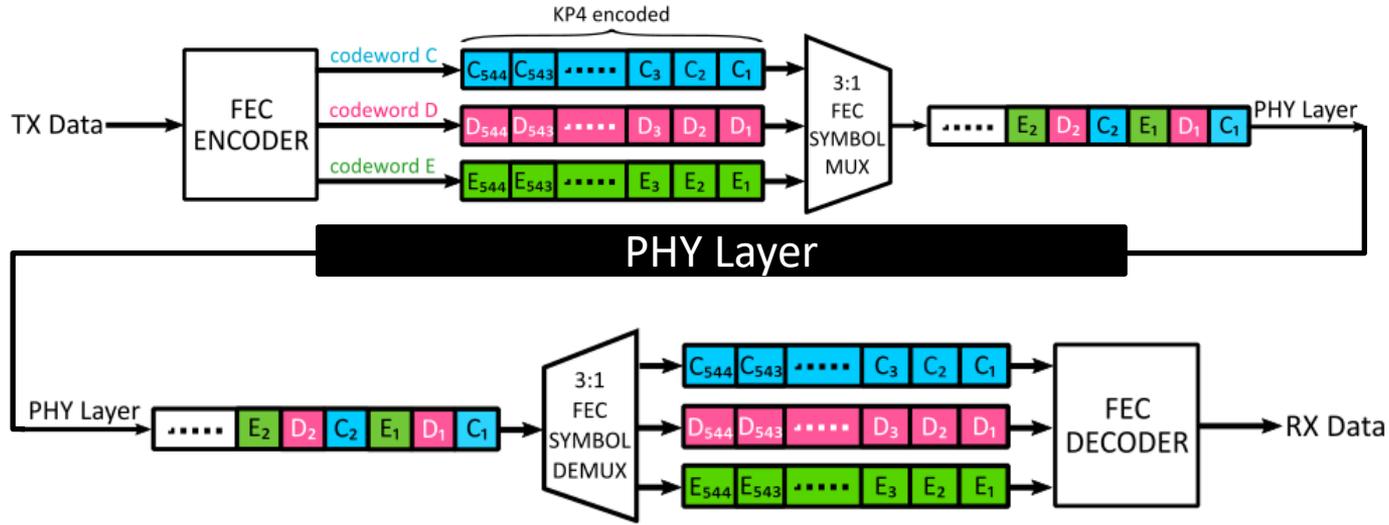


# Outline

1. Motivation
2. Statistical Model for BER Estimation
  - a. Modeling DFE Error Propagation in 2-PAM
  - b. 4-PAM Statistical Model
  - c. Post-FEC BER Estimation for Non-Binary Linear Block Codes
3. Common Coding Techniques in Wireline Links
  - a. Interleaved FEC Code
  - b. MOD4 Precoding
4. Modeling Other Type of Noise Sources
  - a. Residual ISI
  - b. Jitter
5. Experimental Verification
6. Conclusion



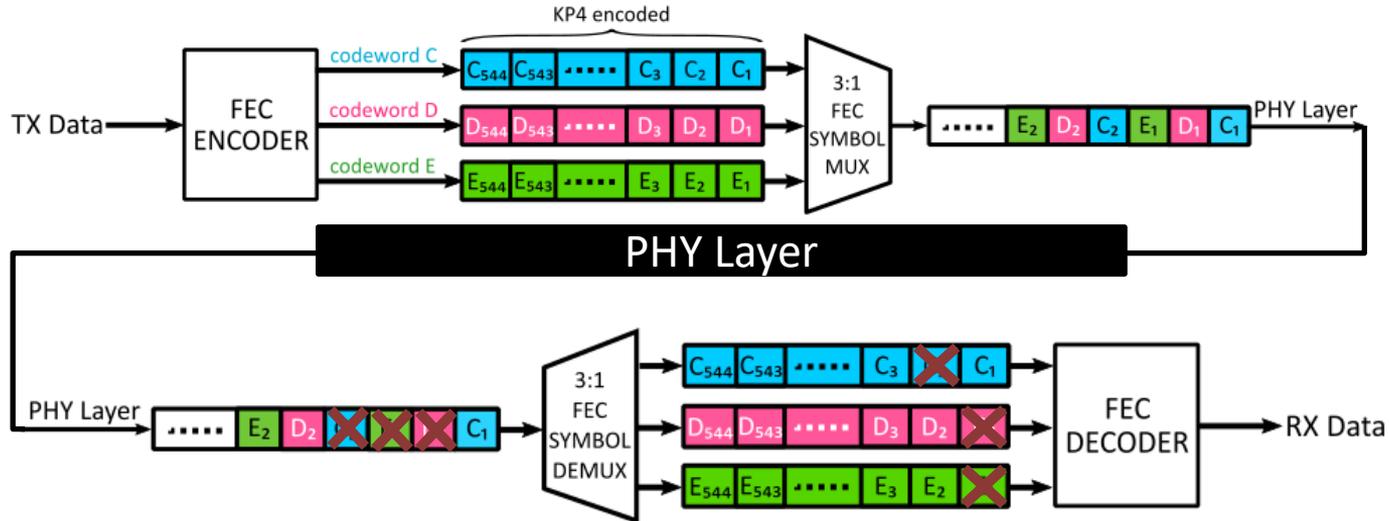
# Interleaved FEC Code



- Interleaving FEC code blocks is a simple way to spread bursts across multiple code blocks, and thereby improve burst-error-correction performance
- Cost is additional transceiver memory and latency



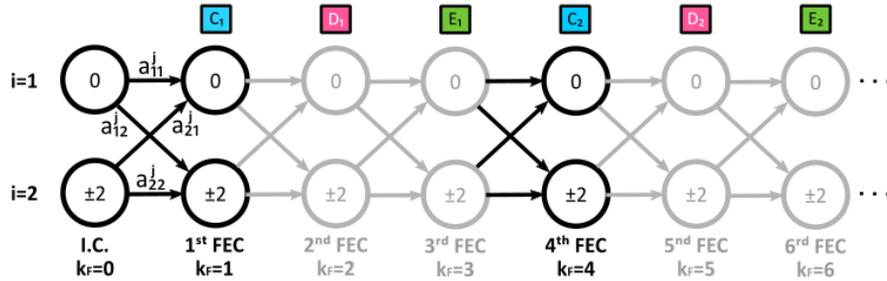
# Interleaved FEC Code



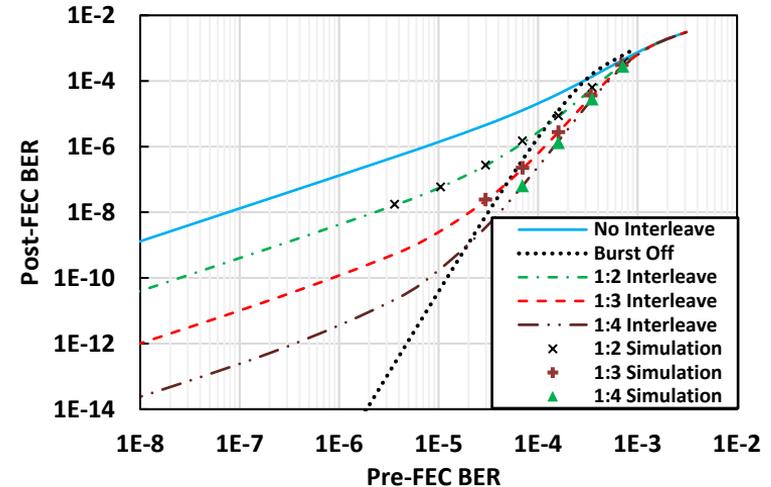
- Interleaving FEC code blocks is a simple way to spread bursts across multiple code blocks, and thereby improve burst-error-correction performance
- Cost is additional transceiver memory and latency



# Statistical Analysis of Time Interleaved Codes



- Analysis of a 3:1 interleaved code of length  $n$  requires analysis of a length  $3n$  trellis
- Results confirm the improved burst-error tolerance offered by interleaving



Pre-FEC vs post-FEC BER plot for interleaved RS(1000,992,4) codes with  $h = 0.5 + 0.25z^{-1} - 0.25z^{-2}$ .

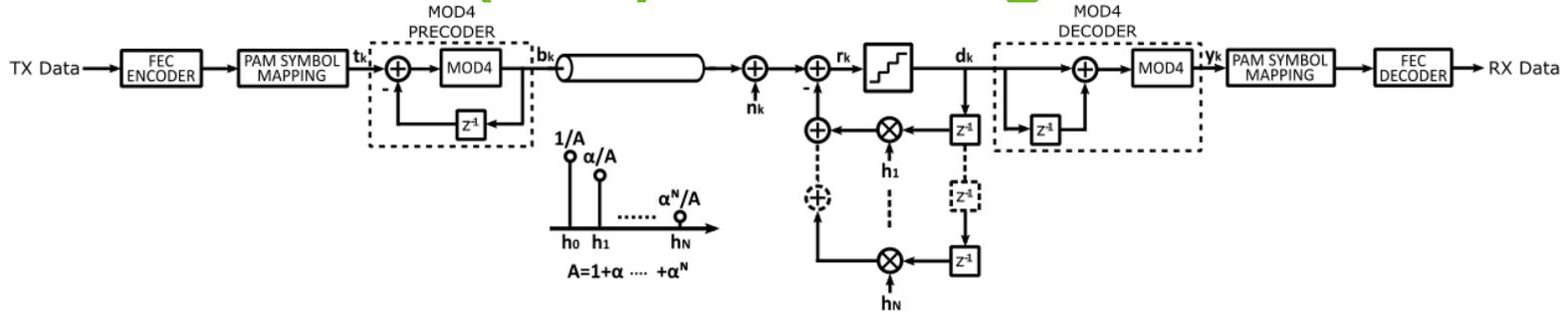


# Outline

1. Motivation
2. Statistical Model for BER Estimation
  - a. Modeling DFE Error Propagation in 2-PAM
  - b. 4-PAM Statistical Model
  - c. Post-FEC BER Estimation for Non-Binary Linear Block Codes
3. Common Coding Techniques in Wireline Links
  - a. Interleaved FEC Code
  - b. **MOD4 Precoding**
4. Modeling Other Type of Noise Sources
  - a. Residual ISI
  - b. Jitter
5. Experimental Verification
6. Conclusion



# Impact of MOD4 (1+D) Precoding



- **(1+D) precoding converts error bursts into only 2 errors: one at the start and one at the end of the burst**
- **Very beneficial for long bursts**
  - Bursts spanning 3 or more FEC symbols turn into only 2 FEC symbol errors

Precoder Input $t_k$	0	2	3	1	1	0	2
Precoder Output $b_k$	0	2	1	0	1	3	3
DFE Output $d_k$	0	3	0	1	0	3	3
Error Value $d_k - b_k$	0	1	-1	1	-1	0	0
Decoder Output $y_k$	0	3	3	1	1	3	2

- **Unfortunately, this also applies to very short bursts**
- **Bursts of length 1 become 2 bit errors**
  - Some isolated random errors (without DFE error propagation) may corrupt 2 FEC symbols

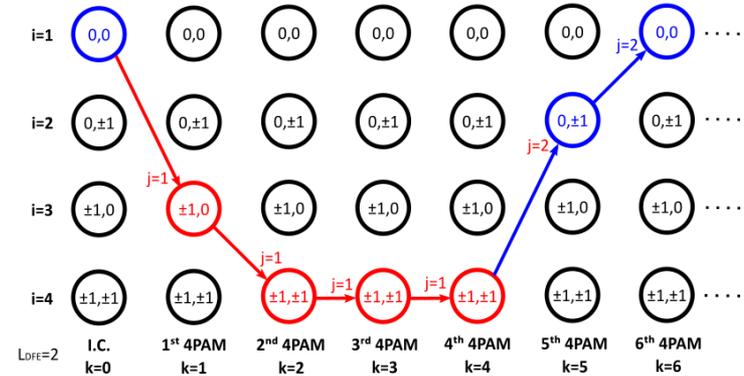
Precoder Input $t_k$	0	2	3	1	1	0	2
Precoder Output $b_k$	0	2	1	0	1	3	3
DFE Output $d_k$	0	3	1	0	1	3	3
Error Value $d_k - b_k$	0	1	0	0	0	0	0
Decoder Output $y_k$	0	3	0	1	1	0	2



# Statistical Analysis of (1+D) Precoding

- Statistical analysis method allows us to identify probability of all error patterns
- (1+D) precoding maps each error pattern to a different error patterns

Example below corresponds to a 2-tap DFE;  
hence, 4-state PAM trellis



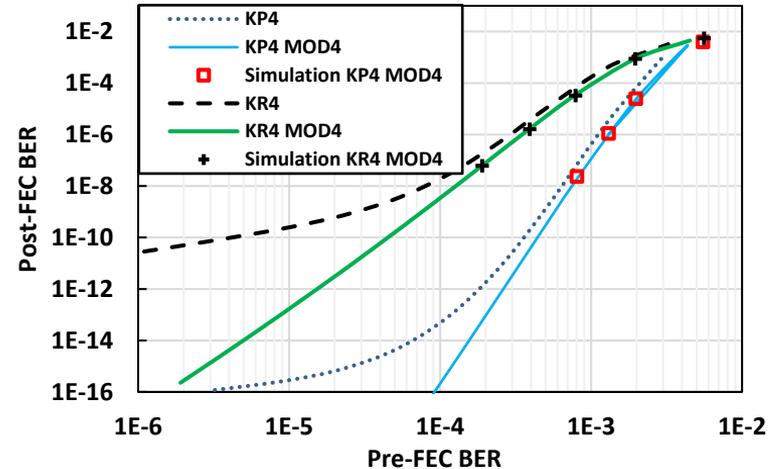
Precoder Input $\mathbf{t}_k$	0	2	3	1	1	0	2
Precoder Output $\mathbf{b}_k$	0	2	1	0	1	3	3
DFE Output $\mathbf{d}_k$	0	3	0	1	0	3	3
Error Value $\mathbf{d}_k - \mathbf{b}_k$	0	1	-1	1	-1	0	0
Decoder Output $\mathbf{y}_k$	0	3	3	1	1	3	2



# Example Analysis Including (1+D) Precoding

- Note that for the same SNR the pre-FEC BER is worse with precoding than without precoding
- However, precoding eliminates the error floor imposed by long burst errors

Pre-FEC vs post-FEC BER plot for the RS(544,514,15) KP4 and RS(528,514,7) KR4 code with  $h = 0.6 + 0.2z^{-1} - 0.2z^2$

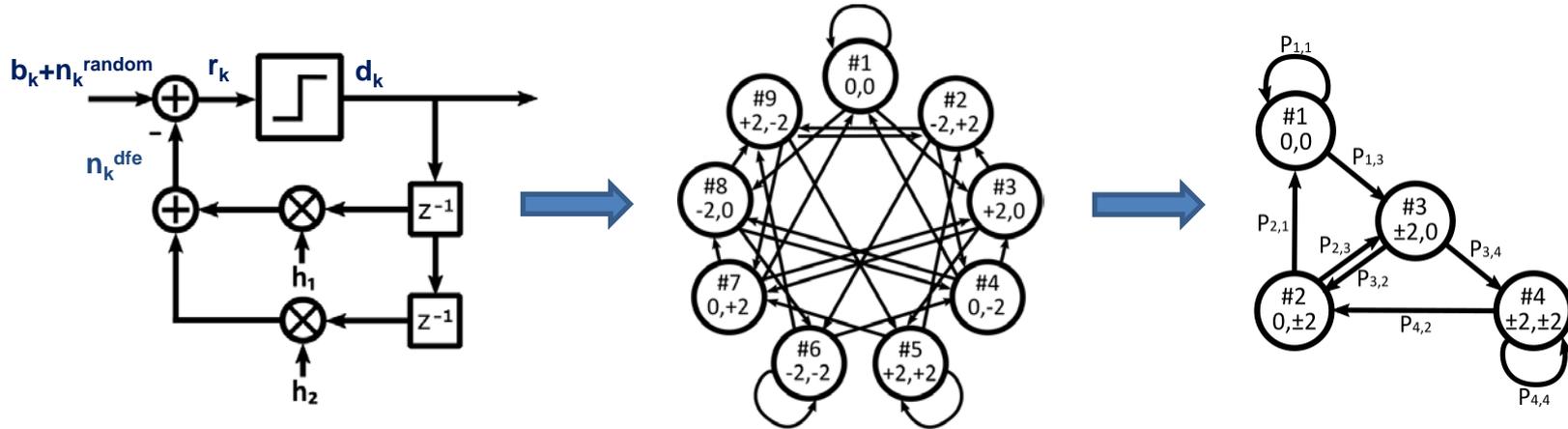


# Outline

1. Motivation
2. Statistical Model for BER Estimation
  - a. Modeling DFE Error Propagation in 2-PAM
  - b. 4-PAM Statistical Model
  - c. Post-FEC BER Estimation for Non-Binary Linear Block Codes
3. Common Coding Techniques in Wireline Links
  - a. Interleaved FEC Code
  - b. MOD4 Precoding
4. Modeling Other Type of Noise Sources
  - a. Residual ISI
  - b. Jitter
5. Experimental Verification
6. Conclusion



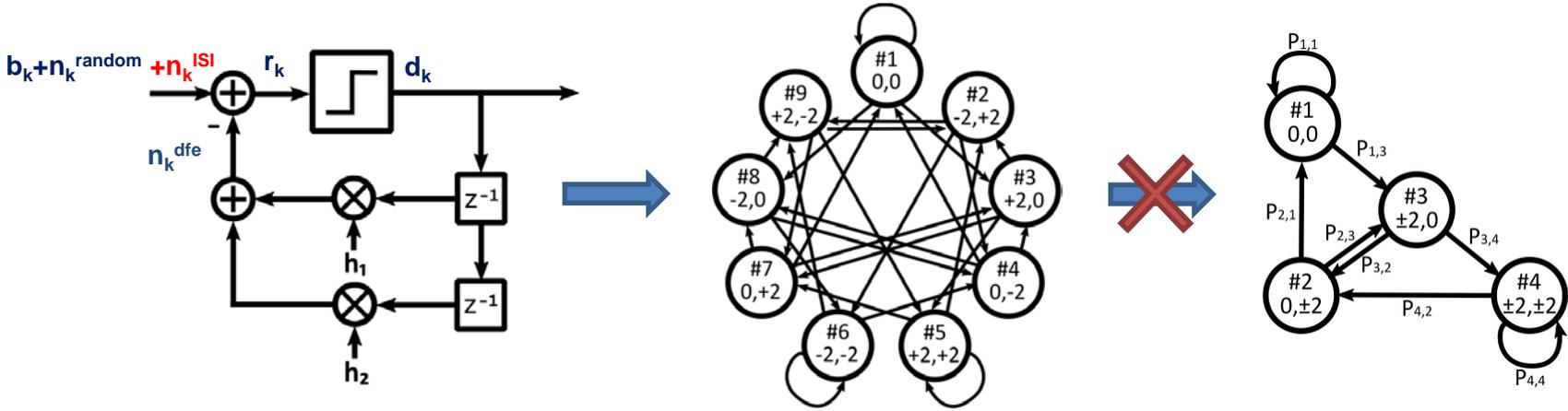
# Consider Residual ISI



- The statistical model discussed thus far assume perfect ISI equalization
  - Only AWGN noise and DFE feedback error are considered
- Allowing us to lump states having the same error values
- Certain conditions must be satisfied to perform state lumping [1], only true without residual ISI



# Consider Residual ISI



- Residual ISI can be treated as an additive noise
  - $r_k = b_k h_0 + n_k^{dfe} + n_k^{random} + n_k^{ISI}$
  
- State lumping is no longer possible in the presence of residual ISI
  - Can only work with the original Markov model

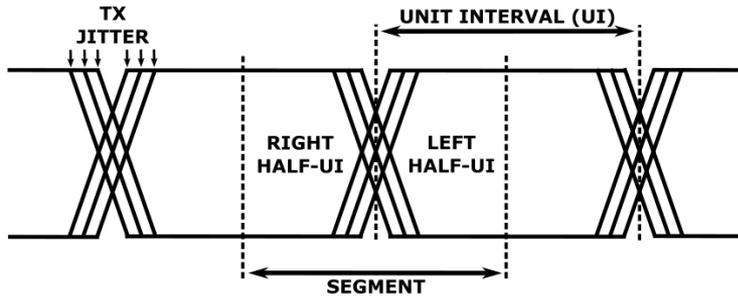


# Outline

1. Motivation
2. Statistical Model for BER Estimation
  - a. Modeling DFE Error Propagation in 2-PAM
  - b. 4-PAM Statistical Model
  - c. Post-FEC BER Estimation for Non-Binary Linear Block Codes
3. Common Coding Techniques in Wireline Links
  - a. Interleaved FEC Code
  - b. MOD4 Precoding
4. Modeling Other Type of Noise Sources
  - a. Residual ISI
  - b. Jitter
5. Experimental Verification
6. Conclusion



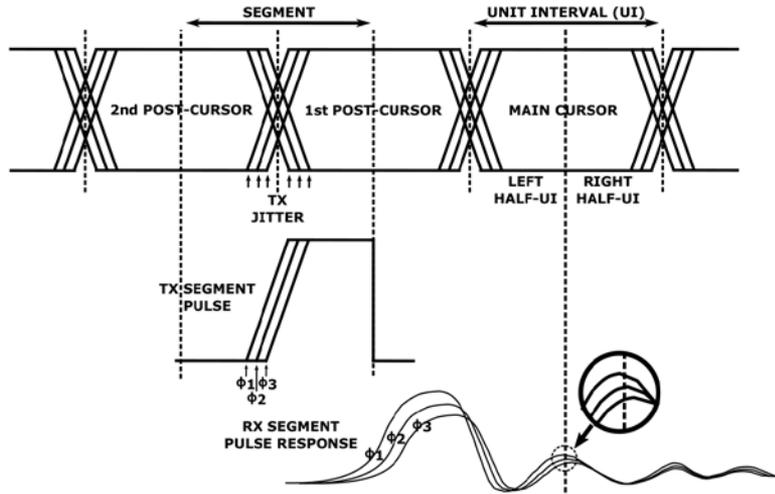
# Jitter



- **Without TX jitter, total ISI distribution can be obtained by convolving the ISI pdf of each UI**
  - ✓ ISI pdf of each UI is independent of others, convolution allowed
- **TX jitter modulates the rising/falling edge of each data transition**
  - ISI distribution of each UI is dependent with the neighboring UI
  - Cannot use convolution to obtain total ISI



# Jitter



- **Adapting segment-based analysis [3]**
  - Segments are defined as a jittery transition from the right half-UI of a symbol to the left half-UI of the subsequent symbol
- **Every data transition occurs in the middle of a segment**
  - ISI distribution of each segment now is independent with other segments
  - ✓ Convolution allowed



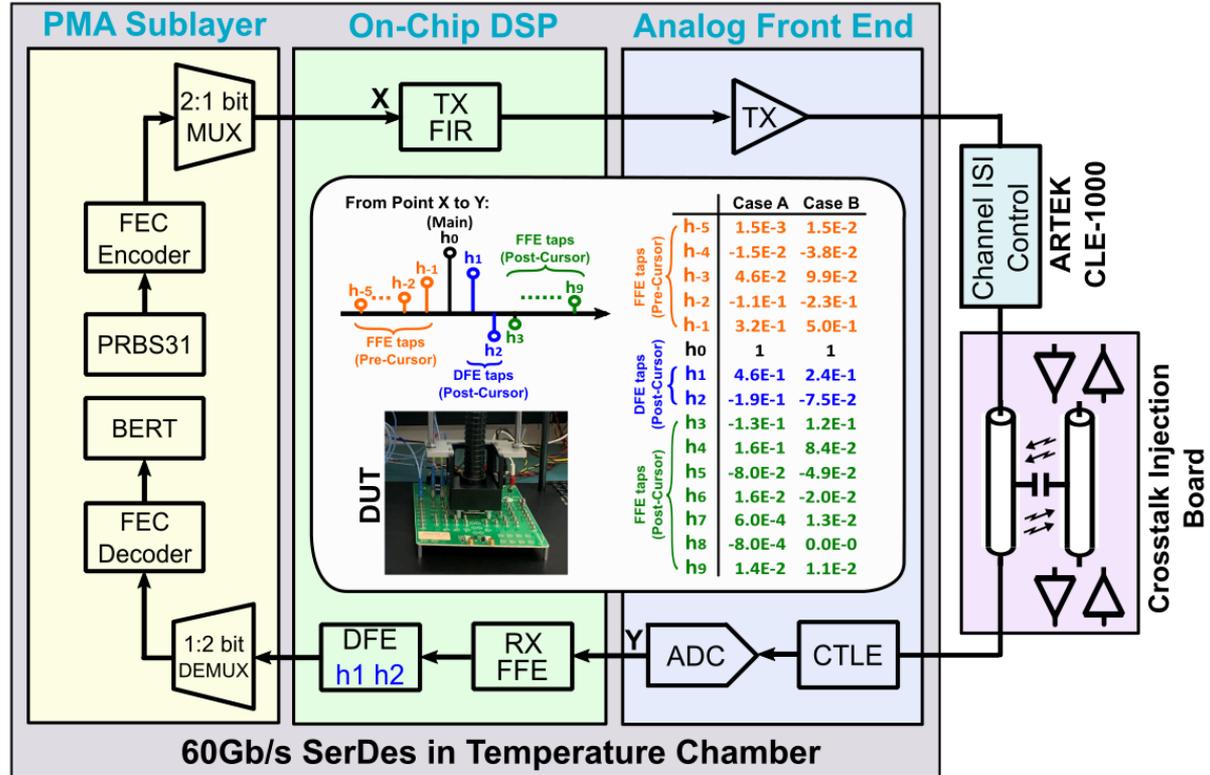
# Outline

1. Motivation
2. Statistical Model for BER Estimation
  - a. Modeling DFE Error Propagation in 2-PAM
  - b. 4-PAM Statistical Model
  - c. Post-FEC BER Estimation for Non-Binary Linear Block Codes
3. Common Coding Techniques in Wireline Links
  - a. Interleaved FEC Code
  - b. MOD4 Precoding
4. Modeling Other Type of Noise Sources
  - a. Residual ISI
  - b. Jitter
5. Experimental Verification
6. Conclusion



# Test Bench Setup

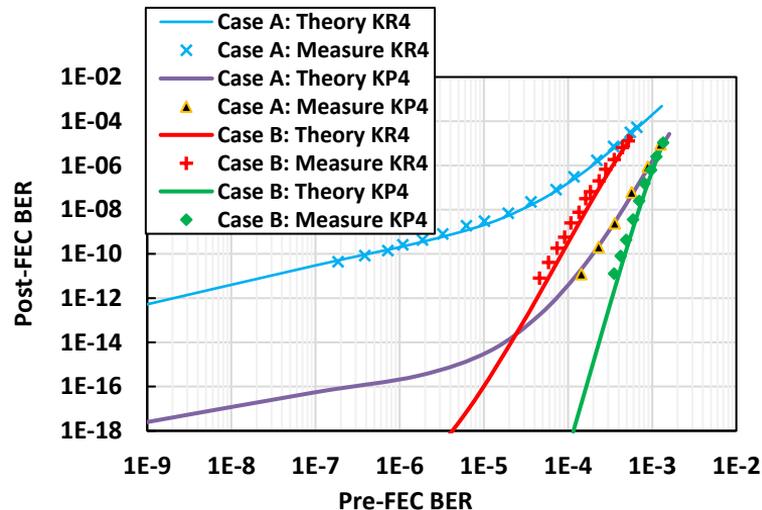
- A 4-PAM 60 Gb/s full transceiver fabricated in 7 nm FinFET [3]
- Two test cases:
  - Case A: 29 dB insertion loss
  - Case B: 24 dB
- Inject Gaussian-like crosstalk
- CDR phase locked after adaptive equalization to minimize random jitter



# Measured Results

- Measured results for both the RS(544, 514, 15) KP4 and RS(528, 514, 7) KR4 code are reported
- Different data points are generated by varying the amount of Gaussian-like crosstalk injected to the channel
- A measurable floor is expected in the post-FEC BER where burst errors due to error propagation in the DFE dominate

Measured and theoretical pre-FEC vs post-FEC BER plot for RS(528, 514, 7) and RS(544, 514, 15) code



# Outline

1. Motivation
2. Statistical Model for BER Estimation
  - a. Modeling DFE Error Propagation in 2-PAM
  - b. 4-PAM Statistical Model
  - c. Post-FEC BER Estimation for Non-Binary Linear Block Codes
3. Common Coding Techniques in Wireline Links
  - a. Interleaved FEC Code
  - b. MOD4 Precoding
4. Modeling Other Type of Noise Sources
  - a. Residual ISI
  - b. Jitter
5. Experimental Verification
6. Conclusion



# Conclusion

- **We presented a statistical approach that accurately estimates post-FEC BER for high speed wireline links subject to DFE burst errors and other important noise sources**
- **Using this approach we can accurately predict post-FEC BER and observe:**
  - The “error floor” imposed by burst errors
  - The positive impact of time interleaving and (1+D) precoding on the burst-error-performance of codes
- **The method was validated using a prototype 60 Gb/s 4-PAM link with KP4 and KR4 standard Reed-Solomon codes**



# References

1. M. Yang, S. Shahramian, H. Shakiba, H. Wong, P. Krotnev and A. Chan Carusone, "Statistical BER Analysis of Wireline Links With Non-Binary Linear Block Codes Subject to DFE Error Propagation," in *IEEE Transactions on Circuits and Systems I: Regular Papers*.
2. B. Casper *et al.*, "Future Microprocessor Interfaces: Analysis, Design and Optimization," *2007 IEEE Custom Integrated Circuits Conference*, San Jose, CA, 2007, pp. 479-486.
3. M-A. Lacroix *et al.*, "A 60Gb/s PAM-4 ADC-DSP transceiver in 7nm CMOS with SNR-based adaptive power scaling achieving 6.9pJ/b at 32dB loss," *2019 IEEE International Solid - State Circuits Conference - (ISSCC)*, San Francisco, CA, 2019.
4. A. Leon-Garcia, *Probability, Statistics, and Random Processes for Electrical Engineering*. Prentice Hall, 2007.
5. R. Kennedy and B. Anderson, "Recovery Times of Decision Feedback Equalizers on Noiseless Channels," in *IEEE Transactions on Communications*, vol. 35, no. 10, pp. 1012-1021, October 1987.
6. C. D. Meyer, "Stochastic complementation, uncoupling Markov chains, and the theory of nearly reducible systems," *SIAM Rev.*, vol. 31, no. 2, pp. 240–272, 1989.
7. X.-R. Cao, Z. Y. Ren, S. Bhatnagar, M. Fu, and S. Marcus, "A time aggregation approach to Markov decision processes," *Automatica*, vol. 38, pp. 929–943, 2002.



# Thank you!

---

## QUESTIONS?

