A 1-Tap 40-Gbps Look-ahead Decision Feedback Equalizer in 0.18-μm SiGe BiCMOS Technology

by

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Abstract

Design of a 1-tap decision feedback equalizer (DFE) at 40-Gbps is investigated for polarization-mode dispersion (PMD) compensation of single-mode fibre. The DFE is fabricated in 0.18μm SiGe BiCMOS technology with a 160-GHz f_t. In order to meet the high speed requirements, a look-ahead architecture is employed to decrease the propagation delay within the feedback path, while maintaining full functionality. Modifications to the architecture were made to ease the requirements on the clock distribution. Measurements show the DFE able to equalize a PMD emulating channel as well as a 20-ft SMA cable up to 10 Gbps with bit error checking. At 40 Gbps, the DFE compensated for a 9-ft SMA cable and functional verification was conducted by hand. The IC occupies an area of 1.5 mm^2 and operates from a 3.3 V supply with 230 mA of current. To the author's knowledge, this is the first fully functional 40-Gbps DFE in any technology.

Acknowledgments

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To my family who continues to support and love me.

To my love, Anjly, I owe everything.

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List of Acronyms

ADC Analog-to-digital converter

AGC Automatic Gain Control

BER Bit error rate

BERT Bit error rate tester

BiCMOS Bipolar complementary metal-oxide semiconductor

CDR Clock and data recovery

CML Current-mode logic

DFE Decision feedback equalizer

DGD Differential group delay

DSF Decision selective feedback

ECL Emitter-coupled logic

EF Emitter follower

FBE Feedback equalizer

FFE Feedforward equalizer

HBT Hetrojunction Bipolar Transistor

IC Integrated circuit

ISI Inter-symbol interference

MOS Metal-oxide semiconductor

OC-768 Optical carrier level 768

PMD Polarization-mode dispersion

SNR Signal-to-noise ratio

TIA Transimpedance Amplifier

UI Unit interval

VNA Vector Network Analyzer

1 Introduction

1.1 Motivation

As the demand for bandwidth continues to grow, it is only a matter of time before OC-768 systems will be a common place. The prolonged slow down of the fibre optical market has allowed researchers to evaluate possible impairments limiting these high data rate systems. One such impairment identified by [BB04] shows that the long haul transmission range of single mode fibre systems is limited by polarization-mode dispersion (PMD). Dispersion compensation of such systems to extend the range of communication is necessary for industrial adoption of OC-768.

PMD results from the impairments along a fibre optical channel which cause an input pulse to be split into two pulses with different polarizations. To a first order approximation, equation 1.1 represents the impulse response of a PMD limited channel and equation 1.2 presents the corresponding frequency response, where $\Delta\tau$ is the differential group delay (DGD) between the two modal pulses and γ is the proportional power split. The nonlinearity that occurs when converting between the electrical and optical domain play an insignificant role in the overall channel response and are therefore ignored. Depending on the DGD and the proportional power split, the frequency response of the channel changes as seen in Fig. 1.1 for various values of γ. Deep nulls occur in the frequency response when the proportional power is split evenly between the two pulses making equalization considerably more difficult.

$$h_{pmd}(t) = \gamma\delta(t) + (1-\gamma)\delta(t-\Delta\tau) \tag{1.1}$$

$$H_{pmd}(f) = \gamma + (1-\gamma)e^{-j2\pi f\Delta\tau} \tag{1.2}$$

Even though PMD compensation can be provided through a variety of means, both optical and electrical, compelling arguments in [BB04] and [Sew04] push towards an electrical solution involving an analog adaptive equalizer. Adaptive equalization is

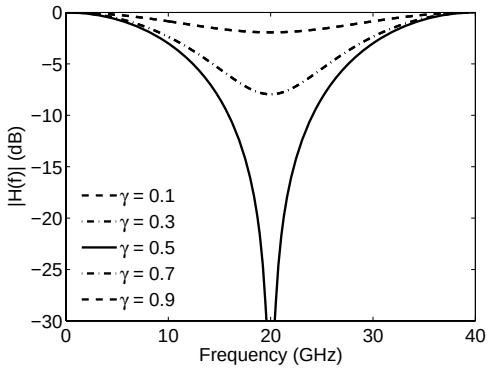


Figure 1.1: Frequency response of PMD with varying γ and $\Delta\tau = TB$. TB is a bit period (e.g. TB = 25 ps at 40 Gbps).[Plot provided by [Sew04]]

attractive since it allows for a higher order of system integration as well as the ability to adapt to the varying frequency response of a PMD limited system.

A linear adaptive equalizer, such as a feedforward equalizer (FFE), is effective at compensating for a variety of dispersive channels and allows for numerous taps to correct for a large number of precursor and post cursor inter-symbol interference (ISI) terms. The disadvantage of such a linear filter is that they also amplify the noise of the system, which degrades the overall signal-to-noise ratio (SNR). This limits the equalization ability of an FFE since it is unable to equalize large signal losses, such as the deep nulls in a PMD channel. Electrical equalization of the deep nulls can be achieved with a decision feedback equalizer (DFE) due to its non-linear nature. A DFE does not significantly amplify the system noise since it outputs a digital decision instead of an analog voltage. For most practical systems, a DFE is often paired with an FFE to correct for a variety of channels. A partial system level view of the equalizer is presented in Fig. 1.2.

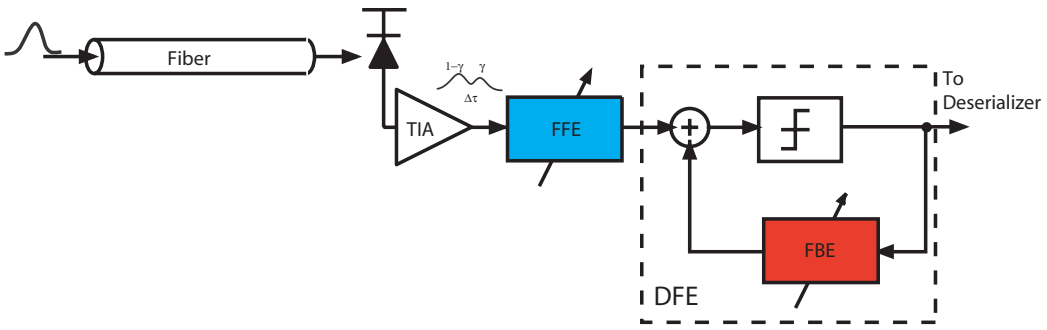


Figure 1.2: System level view of PMD equalization

Previous work in [Sew04] shows that a 3-tap FFE paired with a 1-tap feedback equalizer (FBE) is sufficient to mitigate practical PMD limited systems. This thesis is a continuation of [Sew04] and involves the design of some of the remaining equalizer building blocks. This work focuses on the design of a 1-tap 40-Gbps DFE. The scope of the project involves the implementation of the high speed path and does not address the adaptation or clock recovery issues.

1.2 DFE Architecture Background

The following sections are a quick overview of the possible architectures suitable for high speed implementation. Other architectures, such as a RAM-DFE [BSM95], were not examined since they are too slow for this application. The advantages and disadvantages of each will be examined for high speed design.

1.2.1 Direct Feedback Equalization

The direct feedback equalizer is the conventional approach to implementing the feedback equalizer (Fig. 1.3). The filter processing is computed in the feedback path and

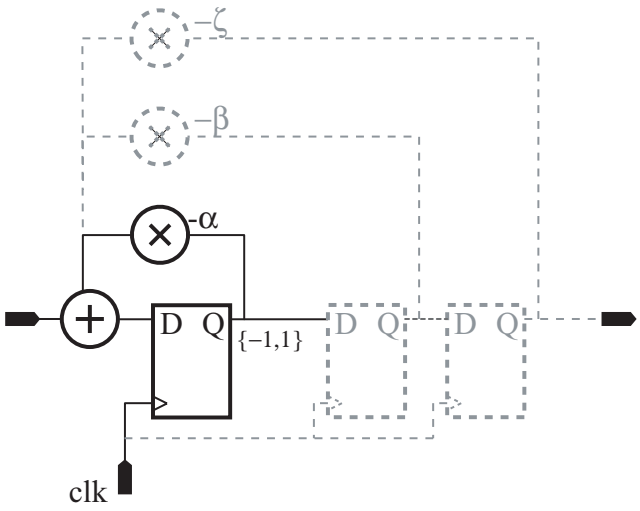


Figure 1.3: Direct feedback equalizer architecture for single tap (solid) and multiple taps (dashed)

added at the summing node. The implementation allows for multiple taps to be added as seen in Fig. 1.3 by the inclusion of the dotted components. From a system view point, direct feedback equalizers still allow for a well known proven clock and data

recovery (CDR) circuit to be used with little added overhead for clock distribution. The major draw back however involves the timing bottleneck of the feedback path which must be completed within a bit period, for a baud spaced equalizer. Additional taps also cause significant loading at the high speed node limiting the performance of the circuit. Implementation of a direct feedback equalizer at high data rates is limited. As the fabrication technology improves however, the speed at which the direct feedback equalizer is viable continues to increase. As will be presented in section 1.3, current technology has allowed for direct feedback equalizer implementations up to 10 Gbps.

1.2.2 Feed-forward Architecture

An alternate architecture to the direct feedback equalizer is a feed-forward system which eliminates the timing bottleneck. The architecture used in [NNI+04] removes the feedback path completely and uses the feed-forward structure seen in Fig. 1.4 to approximate a DFE. The T_{d1} and T_{d2} blocks are delay elements which have a delay difference of 1 unit interval (UI). This generates a non-linear filter without the feedback propagation delay; however, it is functionally different than a DFE.

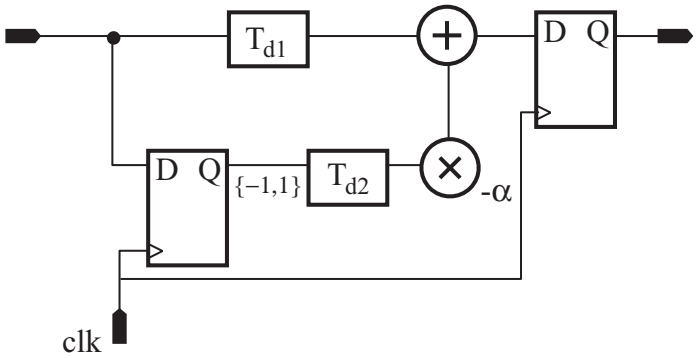


Figure 1.4: Feed-forward architecture of DFE [NNI+04]

The conventional DFE is considered effective on the assumption that the previous decision made was correct. If the previous decision is erroneous, the equalizer works to compensate the incoming signal incorrectly possibly resulting in error propagation. However, if the previous decision is correct, the system equalizes the input into the decision circuit so another correct design can be made, thus decreasing the bit error rate (BER) of the system. This is not the case for the feed-forward architecture since the input into the first decision circuit along the T_{d2} path is never equalized. Therefore

the input into the second decision circuit is equalized based on decisions made from the input raw BER, thus making error propagation a significant concern. The feed-forward DFE and the direct DFE are only equivalent if the input raw BER is low, a case where an equalizer is probably not required. The feed-forward architecture was not explored further since its functional use was not suitable for this application.

1.2.3 Look-ahead Feedback Equalization

Another method of decreasing the feedback propagation time is the use of a look-ahead architecture, originally proposed in [KW91] as a means for high speed implementation. As seen in Fig. 1.5, the architecture makes use of parallel processing [PH98], by removing the filter stages in the feedback path relaxing the timing constraints. The look-ahead architecture equalizes the input signal making multiple decisions. One path makes a tentative decision assuming the previous bit was a 1 and other path assumes the previous bit was a 0. The correct result is then selected and the other decision is discarded via the decision selective feedback (DSF) loop. This relaxes the timing constraint within the filter processing as well as removes the summing node for multiple tap designs (Fig. 1.6) allowing for high speed implementation. The addition of the look-ahead architecture however complicates the overall system by increasing the complexity of the CDR circuit as well as the clock distribution. This results in an overall increase in the area and power consumption.

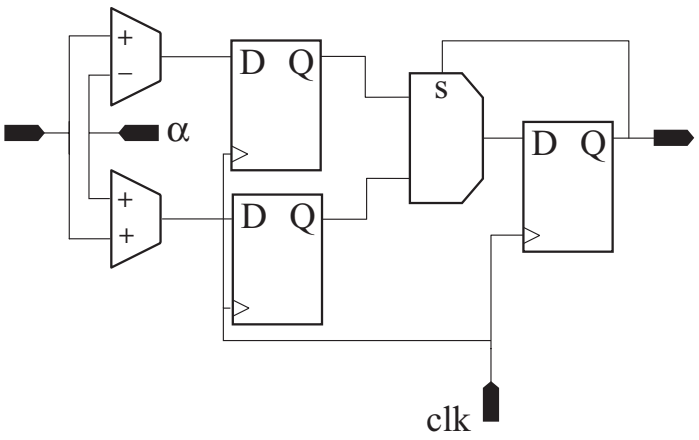


Figure 1.5: 1-tap look-ahead feedback equalizer architecture

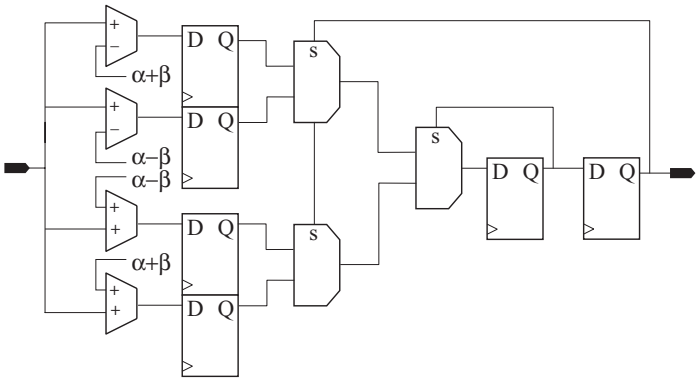


Figure 1.6: 2-tap look-ahead feedback equalizer architecture

1.2.4 Summary

The look-ahead architecture has the advantage of relaxed timing constraints in the feedback path while maintaining full functionality. Disadvantages of this architecture do pose system level issues, however solutions are available [SHG+04] [KHB97]. Multiple tap designs have been demonstrated which use a look-ahead approach for the first tap and the direct feedback for subsequent taps [BCC+05]. Since our channel only requires a single tap, a look-ahead architecture is employed. Further details of the circuit will be presented in section 2.1.

1.3 State of the Art

Since DFEs have been identified as a useful and necessary addition to adaptive equalizers for systems in the gigabit regime, considerable work has recently emerged. The following is a survey of the state of the art implemented adaptive equalizers circuits, which service a host of applications including chip-to-chip, backplane and multimode/single mode fibre.

Texas Instruments presented a 6.25-Gpbs adaptive 4-tap DFE for serial backplane communication [PBR+05]. The tap spacing is a half UI and allows direct first post-cursor cancellation using a direct feedback architecture. The IC was fabricated in a $0.13\mu m$ CMOS process occupying an area of 0.24 mm^2 and consumed 180mW from a 1.2 V supply.

Vitesse Semiconductor published a binary transceiver with adaptive equalizer for backplane transmission operating at 5-Gbps [KBPC+05]. It consisted of a 1-Tap FFE and a 3-tap feedback equalizer at the receiver. The entire transceiver occupied an

area of 12 mm^2 in 0.12μm CMOS technology. It consumed 2.1 W of power from 1.2 V supply. The DFE was implemented using a direct feedback architecture.

Synopsys, Stexar and UNC all presented a joint paper [KYMW+05] which introduced a 0.6 to 9.6-Gbps transceiver with both transmit and receive side equalization. Fabricated in 0.13μm CMOS technology occupying an area of 0.56 mm^2 and consumes 150 mW at 6.25-Gbps. The transmit equalizer has fixed 3-tap weights and the receive side equalizer has a 1-tap look-ahead DFE.

IBM published a 6.4-Gbps 0.13μm CMOS SerDes Core with a 4-tap feed-forward and 5-tap feedback equalizer [SBS+05]. The DFE used a look-ahead architecture for the first tap and a direct feedback for taps 2 through 5. The combination was able to compensate for loses over 30 dB. The transceiver consumed 290mW from 1.2V supply with an area of 0.79mm^2.

Bülow, et al. presented a 10-Gbps DFE [BBB+00], consisting of an 8-tap (55 ps tap spacing) FFE and a 1-tap FBE was implemented in a SiGe process. The feedback equalizer was implemented using a look-ahead architecture and could compensate for PMD up to 1-bit of DGD.

Quake Technologies Inc [MTP05] introduced a 10-Gbps equalizer for single mode fibre with clock and data recovery and on-chip adaptation. The equalizer is a 9-tap FFE with a 3-tap DFE. The system was implemented in a SiGe BiCMOS processes and occupies and area of 9 mm^2. The circuit consumes 900mW.

The fastest non-linear equalizer to the author's knowledge was presented in [NNI+04], by a group at NTT Photonics Laboratories. The IC uses a 1-tap feed-forward architecture to approximate a DFE operates at 40-Gbps. It was fabricated in a InP/InGaAs HBT technology with an f_t of 150 GHz occupying an area of 4 mm^2. It operated from a -4.5 V supply consuming 1.3 W of power. Measurements showed it was effective in mitigating PMD with $\Delta\tau$ of 25 ps and a γ of 0.3 at 40-Gbps.

Some researchers have proposed digital solutions for equalizing these high speed channels. The NTT Photonics Laboratories, who published the fastest DFE, also published a 10-Gbps digital equalizer solution for multimode fibre compensation [NNS+05]. A 24-Gsps, 3-bit analog-to-digital converter (ADC) was used to sample 10-Gbps data and equalize PMD within a fibre channel. The chip size for the ADC was 9 mm^2, with a power consumption of 3.84 W from a 4 V supply. These digital solution including other ADCs, are not practical for most systems due to the extremely high power consumption and chip size. Given current technology and speed limitations, ADC solutions are far from being viable at these speeds.

1.4 Outline

The rest of the thesis is outlined as follows. Chapter 2 contains a discussion of the various circuit blocks designed and the high speed implementation issues involved. Chapter 3 contains measurement results and the characterization of the DFE. Chapter 4 provides conclusions and a discussion of future research opportunities.

2 Design of 40-Gbps 1-Tap DFE Equalizer

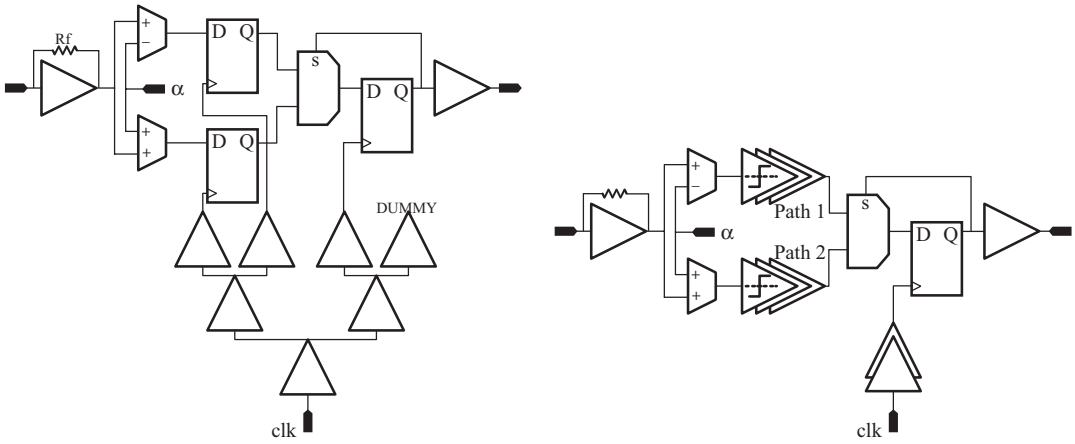
This chapter provides a description of a 40-Gbps decision feedback equalizer fabricated in Jazz Semiconductors' SBC18HX 0.18μm SiGe BiCMOS technology with a 160-GHz f_t. This DFE has been designed to serve as part of a larger PMD compensation system [Sew04]. The IC is a fully-differential 1-tap equalizer designed with a look-ahead topology. An analog differential control voltage adjusts the tap weight. On chip adaptation or clock recovery were beyond the scope of this thesis, but could be accommodated in future work.

Section 2.1 provides an overview of the look-ahead architecture, including implementation modifications for high speed integration. Section 2.2 introduces the DFE with a brief overview of the IC topology and key performance specifications. This section includes the device design methodology for each circuit building block including fabrication technology, transistor biasing and the inductor library. As well, this section also discusses in detail the design of each of the high speed blocks. Section 2.3 shows simulation results of the DFE while equalizing a PMD channel model.

2.1 Architecture Simulation

Of the DFE topologies presented in chapter 1, a look-ahead architecture is chosen in order to minimize the propagation delay in the feedback path. Slight modifications however have been explored to accommodate practical high speed implementation issues, such as 40 GHz clock distribution. One such change is the replacement of the flip flops/latches prior to the selector with 3 cascaded ECL buffers that act as slicers. The removal of the retiming blocks along the two paths greatly reduces the complexity of the clock path; however, it does cause a potential propagation mismatch that decreases the overall timing margin in the feedback path. The propagation mismatch has a similar effect as clock skew between the clocked flip flops/latches. The following analysis examines the potential propagation mismatch between the two paths caused by the clock skew (Fig. 2.1(a)) and the difference in propagation delay between the

slicers (Fig. 2.1(b)).



(a) (b)

Figure 2.1: Look-ahead implementation (a) with retimers at the selector input and (b) with slicers at the selector input

A Monte Carlo simulation for the propagation variation of a single buffer under mismatch conditions is presented in Fig 2.2(a). Process variation was not included since it would affect each path equally. For a population size of 100, the standard deviation of the propagation delay of a single buffer is 345 fs.

The variation of 3 cascaded buffers is determined by

$$\sigma^2 = var[\tau_{p1} + \tau_{p2} + \tau_{p3}] \tag{2.1}$$

$$\sigma^2 = E[(\tau_{p1} + \tau_{p2} + \tau_{p3})^2] - E[\tau_{p1} + \tau_{p2} + \tau_{p3}]^2 \tag{2.2}$$

where τ_{p1}, τ_{p2} and τ_{p3} are the propagation delay of each buffer. The final goal is to estimate the variation between the two propagation paths, so the mean propagation time ($E[\tau_{p1} + \tau_{p2} + \tau_{p3}]^2$) is set to a reference time of zero.

$$\sigma^2 = E[(\tau_{p1} + \tau_{p2} + \tau_{p3})^2] \tag{2.3}$$

Given τ_{p1}, τ_{p2} and τ_{p3} are uncorrelated (i.e. mismatch only, no process variation), the cross-correlations are zero and the variance of each buffer add together.

$$\sigma^2 = E[\tau_{p1}^2] + E[\tau_{p2}^2] + E[\tau_{p3}^2] \tag{2.4}$$

Now assuming the variance on τ_{p1}, τ_{p2} and τ_{p3} are identical for the buffers, the final

relationship is

$$\sigma_3 = \sqrt{3}\sigma_1 \tag{2.5}$$

From Fig. 2.2(b)-(c), the simulation corresponds for a population size of 100 with a σ of 550fs for path 1 and 480fs for path 2. A similar derivation can be made for the propagation variation between the two asynchronous paths (Fig. 2.1(b)) and the variation in the clock distribution (Fig. 2.1(a)), found in equation 2.6 and 2.7 respectively.

$$\sigma_{t_p mismatch} = \sqrt{var[\tau_{p1} + \tau_{p2} + \tau_{p3} - \tau_{p4} - \tau_{p5} - \tau_{p6}]} = \sqrt{6}\sigma_1 \tag{2.6}$$

$$\sigma_{t_p clock} = \sqrt{var[\tau_{p1} + \tau_{p2} - \tau_{p3} - \tau_{p4}]} = \sqrt{4}\sigma_1 \tag{2.7}$$

This results in 22% less variation in the clock distribution than the asynchronous path, not including the physical routing of the clock which makes the mismatch on the clock path optimistic. The slicer implementation has a possible mismatch of approximately 845 fs for one standard deviation. To verify the theoretical value and the assumptions above, a Monte Carlo simulation (Fig. 2.2(d)) for the implemented slicers (Section 2.2.4) shows a variation of 680 fs.

With respect to power consumption, there is a significant difference between the two architectures. Estimating the power consumption, using a buffer power of 26.4 mW, a latch power of 68 mW, and a clock buffer power of 59 mW; the resulting power difference is 278 mW in favor of the slicer based look-ahead architecture (Table 2.1). The estimated power of the buffer, latch and clock buffer, including the emitter follower, is found from simulation at room temperature for nominal process parameters with a supply voltage of 3.3V.

Table 2.1: Power comparison between look-ahead architectures

Architecture	Data Power	Clock Power
Look-ahead with Slicers	158.4 mW	120 mW
Look-ahead with Flip Flops	136 mW	420 mW

Though it is shown that the retimed selector inputs would provide a more robust circuit implementation, the reduction in power and circuit complexity provides favorable trade-offs. The slicer bases look-ahead DFE was implemented.

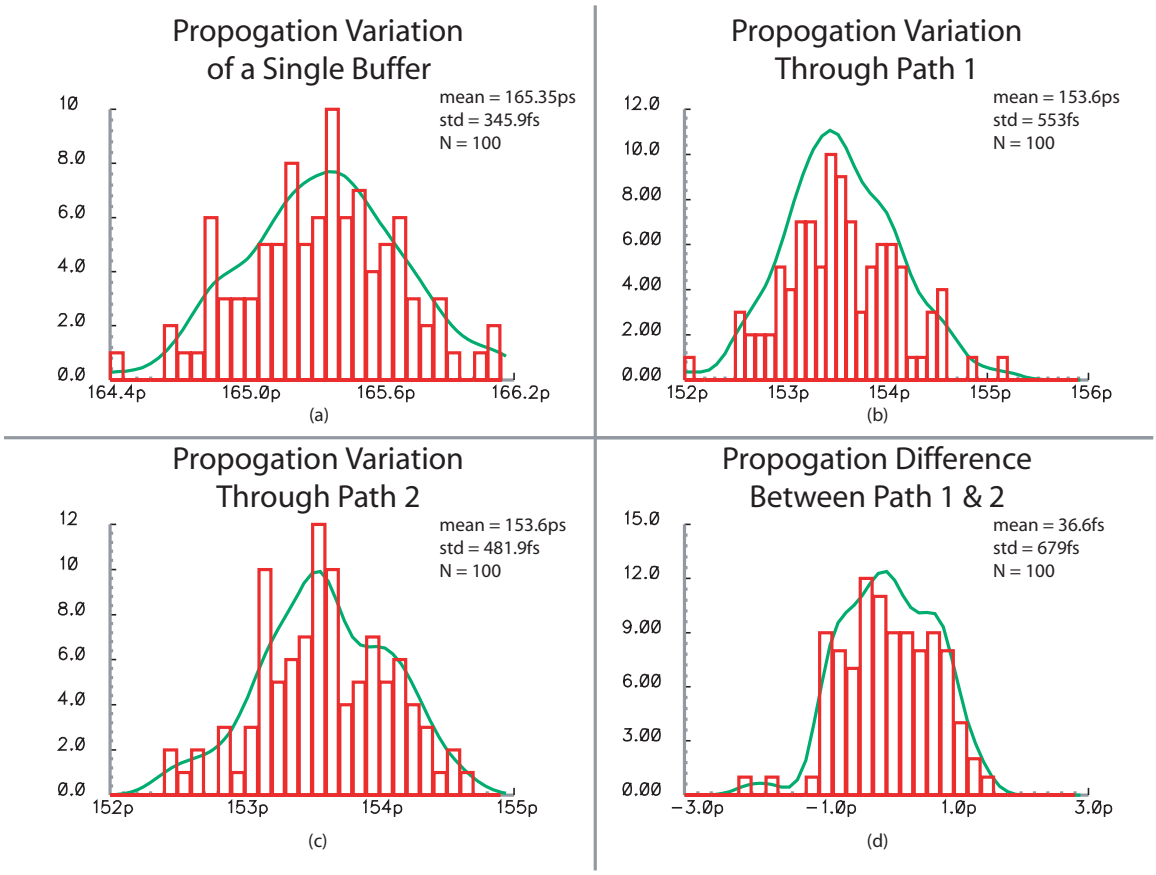


Figure 2.2: Monte-Carlo simulation of propagation delay variation through (a) a single buffer, (b) path 1 with 3 cascaded buffers, (c) path 2 with 3 cascaded buffers, and (d) the difference between path 1 and 2

2.2 Circuit Description

The block diagram of the implemented DFE, with key performance specifications from simulations, can be seen in Fig. 2.3 and is described from right to left below. The input is fed into the broadband front end which features two stages. The shunt-series feedback input amplifier is used as an input voltage preamplifier with low noise and large bandwidth. The output of the feedback amplifier is fed into a slicing threshold adjustment block which varies the differential DC offset of the output via the tap weight control voltage, α. This effectively changes the slicing threshold into the 3 cascaded emitter coupled logic (ECL) buffers that limit the signal. Each path acts as an equalizer to cancel 1 bit period of post cursor ISI. The slicer output feeds into the decision selective feedback, where the DSF selects one of the paths based on the previous decision of the flip flop. This feedback path from the clock input of the flip

flop to the data input of the flip flop must be within 1 bit period. An output driver with variable swing drives the output of the flip flop off-chip. The clock path features 2 stages of E^2CL buffers, and the clock signal is also made available externally for possible testing purposes.

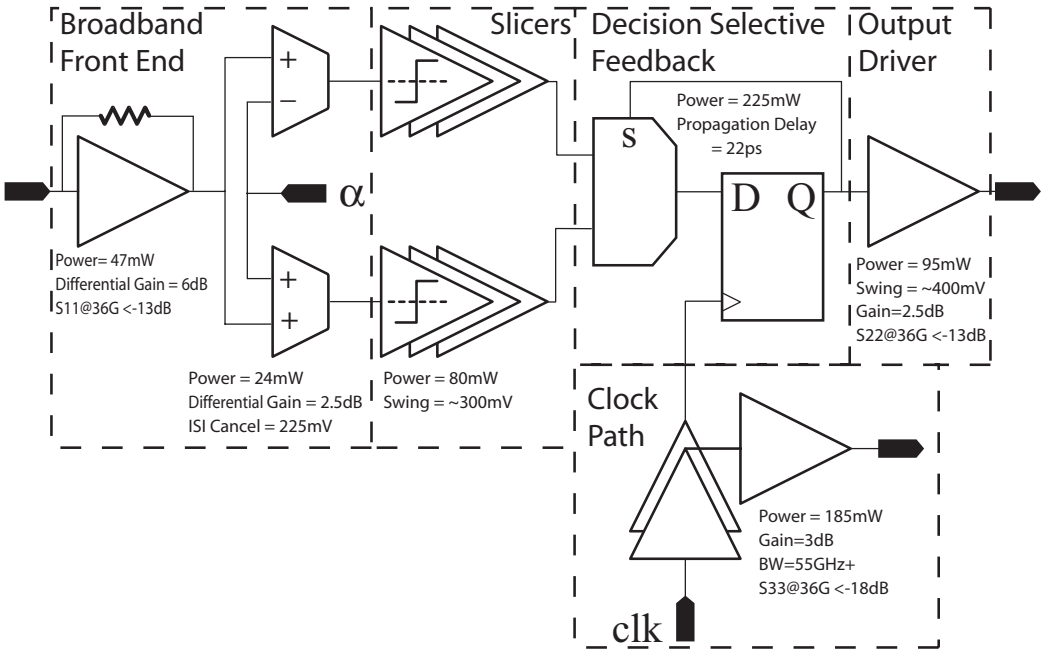


Figure 2.3: Chip block level representation

The following sections discuss the design of the overall building blocks as well as the design of the devices at 40-Gbps.

2.2.1 Building Block Device Design

The following sections provide background information used to design the various building blocks of the DFE. This includes the technology characteristics, transistor biasing, current source design and the inductor library.

Fabrication Technology

The design of the DFE is conducted in Jazz Semiconductors' commercially available SBC18HX 0.18μm SiGe BiCMOS technology. Even though the DFE implementation is not specific to this fabrication process, the use of a high speed technology is required. Careful technology selection is necessary in order to meet the performance requirements at 40 Gbps.

The technology has a maximum cutoff frequency (f_t) and maximum oscillation frequency (f_{max}) of 160-GHz and 150-GHz respectively from measurements. A collector current density (J_{peakf_t}) of 1.2mA/μm maximizes f_t and f_{max} simultaneously [RK03]. The minimum noise figure of the transistor at 40 GHz is 4dB from measurements. A collector current density (J_{minNF}) of 0.3mA/μm minimizes the noise figure of the transistor. The technology figures of merit are shown in Fig. 2.4. The fabrication processes has 6 metal layers, where the top metal is suitable for high speed applications.

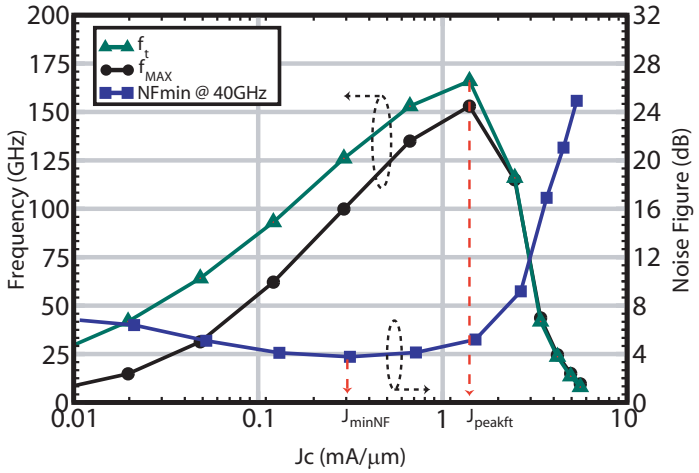


Figure 2.4: Technology figure of merits measurements of f_t and f_{max} and minimum noise figure at 40 GHz

Transistor Bias Conditions

As seen from Fig. 2.4, there is a collector current density that maximizes the performance of the transistor depending on its particular application. For low noise applications the transistor should be biased at J_{minNF} and for high bandwidth linear applications at J_{peakft} [VMS+97]. The biasing of the high speed digital blocks, however should be less than J_{peakf_t}.

The transistors of the high speed digital logic blocks are biased at $0.75J_{peakf_t}$ at common mode voltage levels. Biasing at J_{peakf_t} is undesirable since a total current of up to $2J_{peakf_t}$ would flow through the transistor as the current switches from one device to another [Rei96]. Such large current densities are avoided due to high current effects (Kirk-effect) and self heating which destroys the performance and reliability of the transistors [TN98]. The transistors are therefore biased slightly below J_{peakf_t} such

that it operates within the top portion of the f_t curves (Fig. 2.4) during switching [Voi05]. Lower current densities are not used due to the performance degradation of the blocks.

For an emitter follower (EF), the transistor is biased between 1/2 to 1/3 J_{peakf_t}. The devices are typically not biased at peak f_t due to the overshoot in the frequency response [Voi05]. It can be shown that the small signal voltage transfer function is a 2 pole system which can potentially be underdamped [JM97]. Biasing the EF at lower J_{peakf_t} still provides the required bandwidth while minimizing the potential peaking.

Current Sources

The current sources of the building blocks are all simple MOSFET current mirrors. More complicated current mirror topologies are not employed to increase the output impedance, and hence the common-mode rejection, since at high frequencies the capacitance dominates. Degenerated bipolar transistors typically are better suited for use as current sources due to their high output impedance and low collector-substrate capacitance; however, to allow for operation from a lower power supply voltage, MOSFET current sources were used throughout the design.

Inductor Design

Numerous single-metal spiral inductors were used throughout the design of the high-speed and broadband analog blocks to increase their bandwidth without increasing their power consumption. The inductors were characterized with ASITIC [Nik02] and approximated using a 2-π model seen in Fig. 2.5. Background information on inductors and modeling can be found in [DLB+05]. The following is a summary of the derivation and inductor design covered in [Lee98] for shunt peaking of a broadband amplifier.

The addition of an inductor at the load of a broadband amplifier (Fig 2.6), also known as shunt peaking, has been used to enhance the bandwidth of the amplifier. Consider the simple equivalent output impedance of an inductively peaked amplifier which contains a peaking inductance of L_p, load resistance of R_l and a load capacitance of C_l. The impedance of such a system is:

$$Z(s) = (sL_p + R_l)||\frac{1}{sC_l} = R_l\frac{s(L_p/R_l)+1}{s^2L_pC_l + sR_lC_l + 1} \tag{2.8}$$

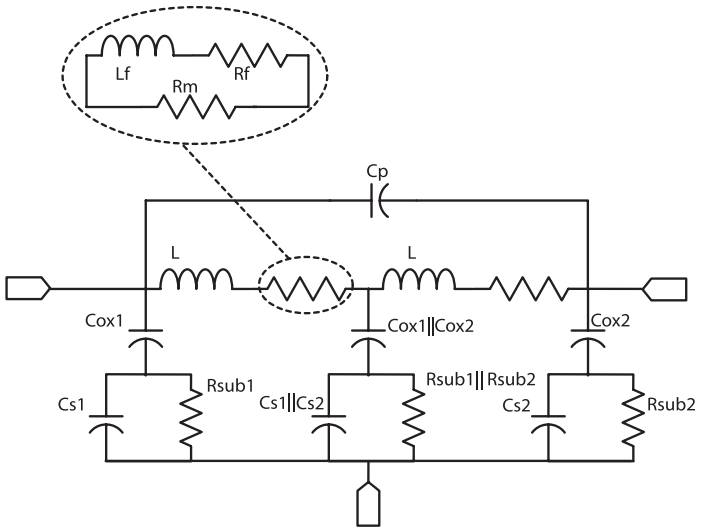


Figure 2.5: 2-π model of spiral inductor

The addition of the inductor increases the bandwidth by introducing a zero to the

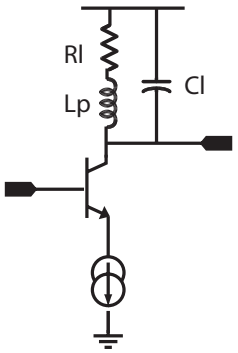


Figure 2.6: Inductively peaked amplifier

transfer function as well as increasing the frequency at which the pole has an effect. The bandwidth enhancement, where ω_2 is the "peaked" bandwidth and ω_1 is the previous bandwidth, is given in equation 2.9. The passive elements are collected such that $m = R^2C/L$.

$$\frac{\omega_2}{\omega_1} = \sqrt{(-\frac{m^2}{2} + m + 1) + \sqrt{(-\frac{m^2}{2} + m + 1)^2 + m^2}} \tag{2.9}$$

Using this equation, design guidelines are set to help choose the correct m ratio. From results in [Lee98], the following table is obtained. All inductors were designed to not exceed the group delay requirements so as to not add jitter to the broadband

data. Thus by employing inductive peaking, a 60% improvement in bandwidth can be obtained without increasing power consumption.

Table 2.2: Shunt peaking inductance design ratios

Condition	$m = R^2C/L$	Normalized Bandwidth	Normalized Peak Frequency Response
Max Bandwidth	1.41	1.85	1.19
Max Flat Response	2.41	1.72	1
Flat Group Delay	3.1	1.6	1

The inductor library used in the design of the high speed building blocks of the DFE were all single metal inductors and have a layout shown in Fig. 2.7. Their effective inductance values and their 2-π models are found in Table 2.3.

2.2.2 Broadband Front End

The broadband front end is extremely important and characterizes the overall system performance of the DFE. The input stage is a shunt-series feedback buffer followed by a high speed buffer with variable DC output offset. The following section discusses the design and characteristics of the blocks.

Shunt-Series Feedback Input Buffer

A shunt-series feedback input buffer is employed as an input voltage preamplifier. This circuit has the same topology as a transimpedance amplifier and will therefore be referred to as a TIA. The TIA has been shown to provide simultaneous input and noise matching without limiting the circuit bandwidth [VDC$^+$05]. Historically current mode logic (CML) inverter or ECL inverter stage are used as input preamplifiers with a 50 Ω on-chip resistor for input matching purposes (S_{11}). This however causes a degradation in the noise figure (sensitivity) of the system as well as it limits the system bandwidth since large devices are also required to provide the input noise matching. The use of the shunt feedback decreases the optimum source impedance (Z_{sopt}) and input impedance (Z_{in}), such that the matching can be achieved with a smaller bias current and device size.

The schematic of the implemented TIA is presented in Fig. 2.8. The design of the TIA is conducted using the methodology outlined in [VDC$^+$05]. Input transistors ($Q_{1,2}$) are sized for a current density of 0.4mA/μm, which is slightly higher than the

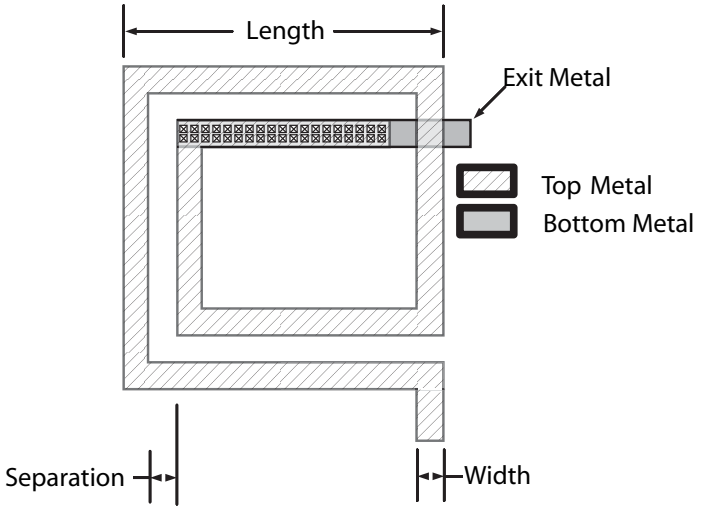


Figure 2.7: Single-metal inductor layout

Table 2.3: Table of inductor layout and modeling parameters.

Value	105 pH	135 pH	150 pH	175 pH
Top Metal	M6	M6	M6	M6
Exit Metal	M5	M5	M5	M5
Length (μm)	27	27	30	35
Turns	1.75	2.25	2.25	2
Width (μm)	2.5	2.5	2.5	2.5
Separation (μm)	2	2	2	2
L (pH)	38.5	52.5	62.5	74
R_m (Ω)	1.4	1.4	1.425	1.5
R_f (Ω)	.5	.7	1.575	1.63
L_f (pH)	5.4	8.05	29.7	33.3
C_{ox1} (fF)	2.46	1	1.79	1.89
C_{ox2} (fF)	2.1	2.24	0.52	0.76
C_{s1} (fF)	0.67	2	0.27	0.25
C_{s2} (fF)	1.9	3	0.17	0.16
R_{s1} ($K\Omega$)	12.6	11.8	37.2	41.2
R_{s2} ($K\Omega$)	1.9	5	59	63.1
C_p (fF)	0.5	0.6	1	0.6

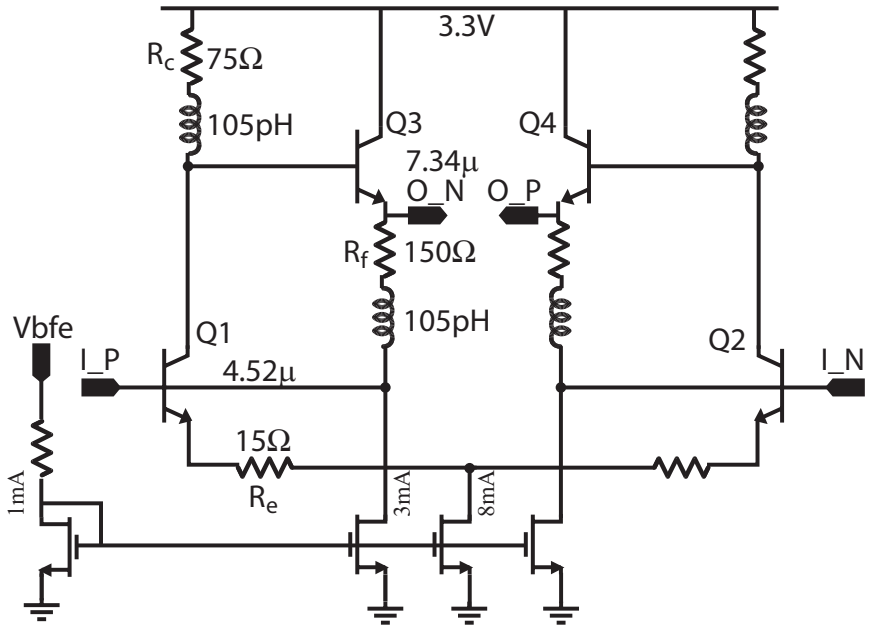


Figure 2.8: Shunt series feedback amplifier stage

transistor J_{minNF} since the low noise bias current changes due to the added emitter degeneration resistance (R_e) [Voi05]. The bias current, collector resistance (R_c), and the emitter degeneration resistance (R_e) are used to set the loop gain (equation 2.10) and output voltage swing of the TIA.

$$A_v = \frac{g_m R_c}{1 + g_m R_e} \tag{2.10}$$

The output voltage swing is a product of the bias current and R_c. It was set to 600 mV to maximize the input dynamic range. The loop gain approximately determines the feedback resistor (R_f) required for input impedance matching from equation 2.11, where R_{in} is 50Ω.

$$R_{in} = \frac{R_f}{1 + A_v} \tag{2.11}$$

R_f also provides a DC common-mode voltage drop to lower the base voltage of $Q_{1,2}$. This allows the output voltage to swing freely without decreasing the V_{CE} of $Q_{1,2}$ and dropping the transistor into saturation. $Q_{1,2}$ are scaled, with a constant J_{minNF} until the optimum source impedance (Z_{sopt}) is roughly 50 Ω. The peaking and feedback inductor are added to increase the bandwidth of the system and the feedback inductor also filters off the high frequency noise caused by R_f [HPM+03].

Slicing Threshold Adjustment Buffer

The slicing threshold adjustment buffer (Fig. 2.10) is composed of an emitter degenerated high-speed bipolar stage with DC offset control of the outputs ($O_{P/N}$) using a BiCMOS cascode ($Q_{3,4,5,6}$) via a control voltage, α. This circuit is the physical implementation of the filter coefficients of the equalizer. An introduction of a DC offset at the outputs causes a nonzero slicing threshold into the following slicers. This strengthens the transition equalizing for possible missed bits. A sample bit stream is presented in Fig. 2.9, which shows the unequalized input (top) during an erroneous transition. If the slicing threshold was zero the transition would be missed (Fig. 2.9(a)). However, if a nonzero threshold is used, the transition is detected and the slicer outputs the correct bit sequence (Fig. 2.9(b)).

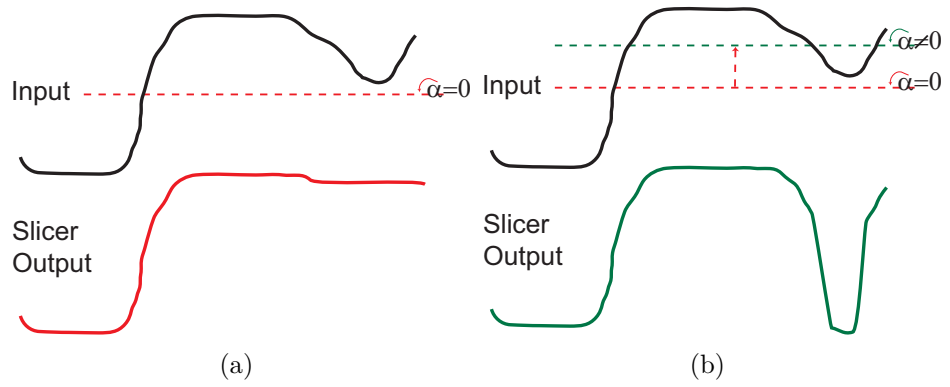


Figure 2.9: Sample bit stream showing an unequalized input (top) and slicer output (bottom) for variable slicing threshold (a) Erroneous slicer output for zero slicing threshold, $\alpha = 0$ (b) Error-free slicer output for nonzero slicing threshold, $\alpha \neq 0$

The high speed buffer is biased for maximum bandwidth and is degenerated to increase the linearity of the broadband front end. Shunt peaking inductors are used to further increase the bandwidth without increasing the power consumption of the block. The high speed outputs $O_{P/N}$ are connected to the BiCMOS cascode pair which vary the differential offset current into the load resistors. The MOSFETs are buffered from the high speed path with bipolar cascode transistors ($Q_{3,4}$) chosen because of their lower collector-bulk capacitances than the MOFSET drain-bulk capacitance. As well, the bipolar cascode devices provide a wider linear tuning range of the tap weight, due to the high output resistance and constant V_{DS} on $Q_{5/6}$, for large changes in the DC offset voltages. A large overdrive voltage of 0.6 V for the MOSFET differential

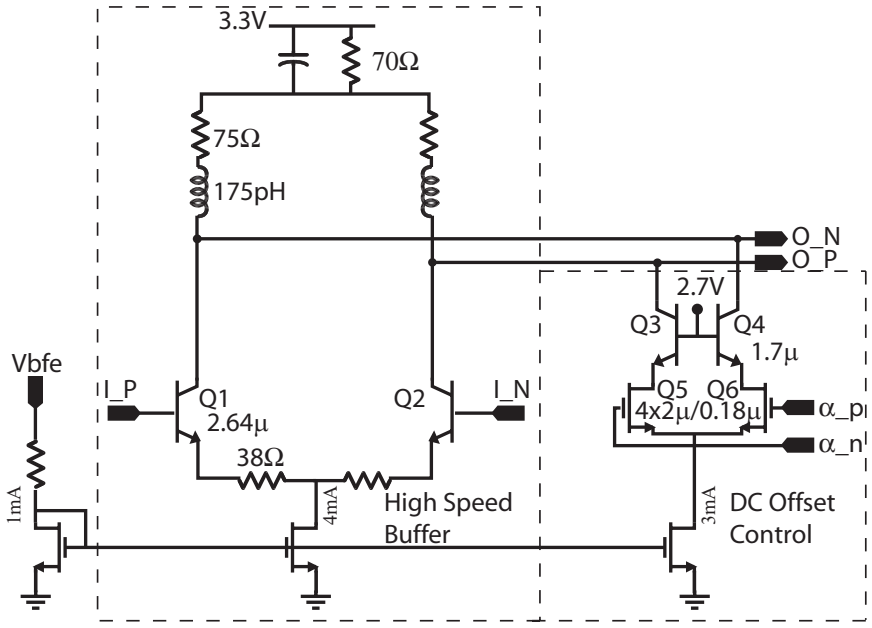


Figure 2.10: Slicing threshold adjustment buffer

pair ($Q_{5,6}$) increases the linear tuning range of α as well. This does however result in smaller devices sizes which have the potential to have a larger mismatch between the two threshold circuits in each path. A plot of the differential tap weight (α) versus DC output offset voltage is shown in Fig. 2.11.

Another method of generating a variable slicing threshold would have been to use mismatched differential pairs to provide a DC offset. As seen in Fig. 2.12, intentionally mismatching the differential pairs creates a high speed buffer with a positive DC offset and a high speed buffer with a negative DC offset. Varying the

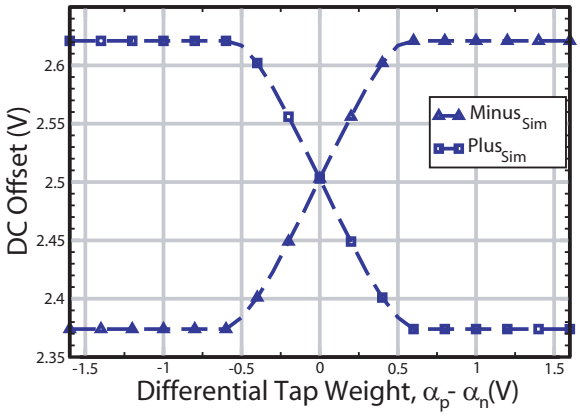


Figure 2.11: Simulated output offset voltage versus differential tap weight (α)

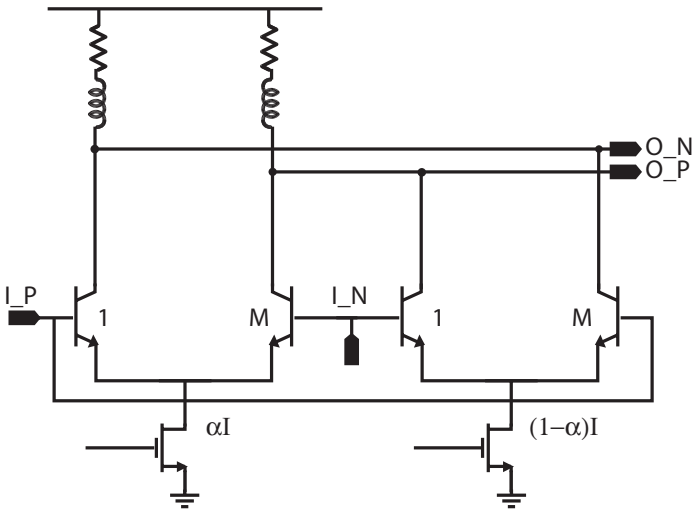


Figure 2.12: Alternative input referred threshold adjustment circuit [GHS+05]

tail current of the buffers, the output threshold level of the two mismatched pair is adjusted and can be zeroed. The circuit was used in [GHS+05] and designed to have little variation in gain and bandwidth over the tuning range.

The disadvantage of using the input referred threshold circuit (Fig. 2.12) is that it loads the high speed path more significantly than the other implementation. As well, it is considerably more difficult to design since the high speed performance and DC offset tuning are interdependent and subject to significant process variations. The implemented threshold circuit (Fig. 2.10) allows the high speed and DC performance to be optimized separately resulting in a robust circuit.

Broadband Front End Linearity

The input linearity is limited by the threshold adjustment circuit of the broadband front end. To determine the 1dB compression point (P_{1dB}) a single tone source is applied at one of the inputs, with the other input terminated to a 50 Ω resistor, and the resulting differential output power is measured. The input power was increased until the output power had compressed by 1dB. Single-ended P_{1dB} simulation results of the TIA and the variable threshold buffer are shown in Fig 2.13 for a frequency of 10, 20 and 30 GHz. A P_{1dB} of -4 dBm for the input feedback stage and -7 dBm for the variable threshold buffer has been achieved. This roughly corresponds to an input of 140 mV_{pp} for the entire broadband front end.

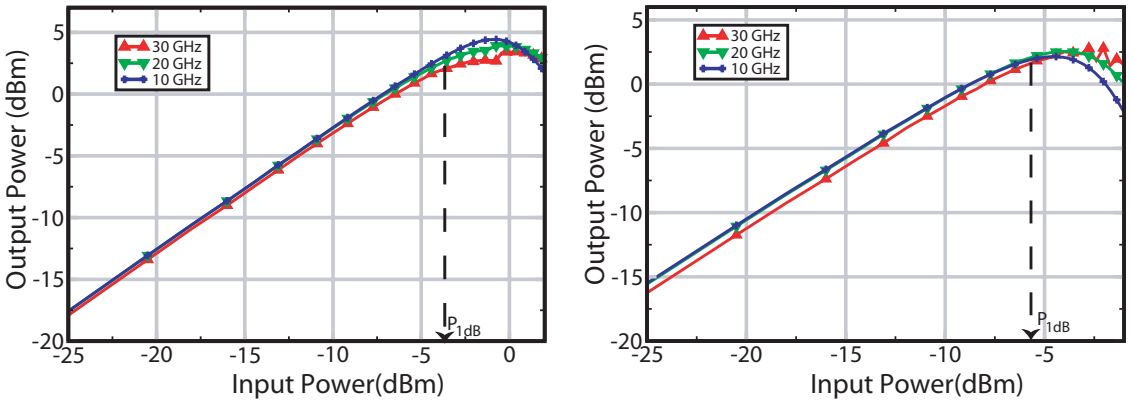


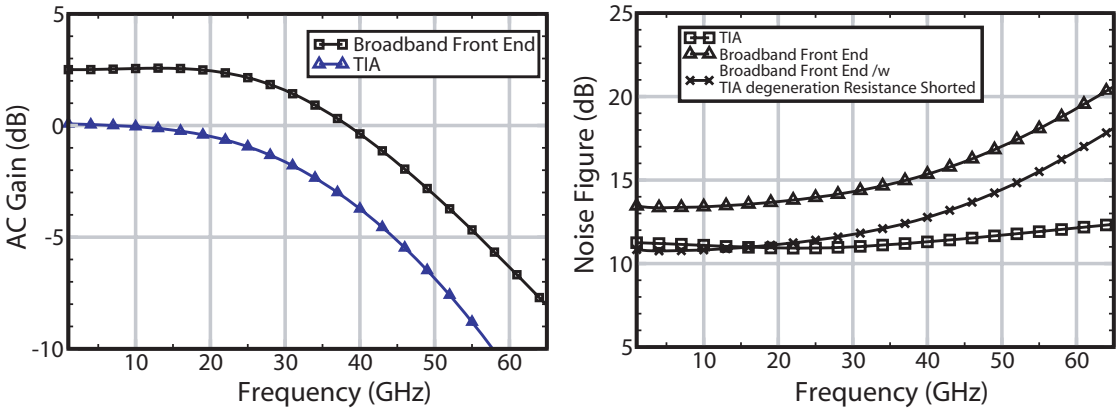
Figure 2.13: Broadband front end linearity (a) shunt series feedback amplifier (b) variable slicing threshold buffer

Broadband Gain and Noise Figure

The simulated single-ended input/output broadband gain of the circuit is shown in Fig. 2.14(a). The gain of the front end is relatively small, 2.5 dB, to maximize the input linearity. This however has an adverse affect on the noise performance (sensitivity) of the system. The lack of gain through the first stage allows for the preceding stages to degrade the noise figure of the system, as seen from Friis equation

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots \tag{2.12}$$

where F_i is the noise figure of the i^{th} block in a cascade of stages and G_i is the gain. The single-ended noise figure of the TIA and the entire broadband front end, with the other inputs terminated to 50 Ω, show a difference of 3.3 dB at 30 GHz (Fig. 2.14(b)). Running a noise simulation, the top noise contributors are found to be $Q_{1/2}$ of the threshold adjustment circuit (Fig. 2.10) due to the lack of gain in the TIA. Now if the degeneration resistance is shorted (decreased), the noise figure drops substantially (Fig. 2.14(b)) and moves towards the noise figure of the TIA as expected. Ideally an input stage, such as an automatic gain control (AGC), is utilized to maximize the input dynamic range while maintaining a high sensitivity.



(a) (b)

Figure 2.14: Simulated single-ended (a) Input/output frequency response for the TIA and broadband front end (b) noise figure for the TIA, broadband front end and the broadband front end with the TIA degeneration resistors shorted

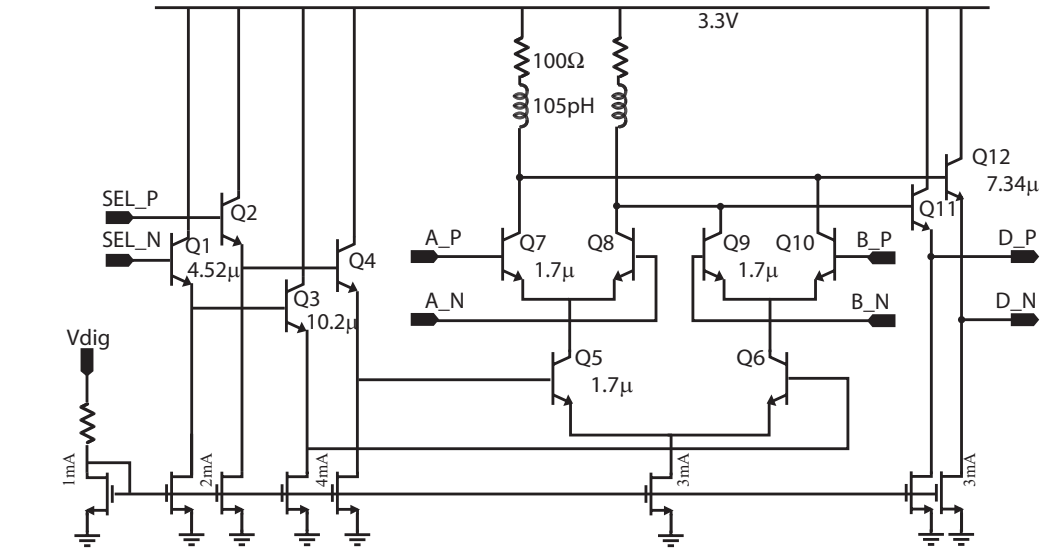
2.2.3 Decision Selective Feedback

The decision selective feedback (DSF) is comprised of a selector and a master slave flip flop (MS-FF). Schematics of the ECL implementation of these building blocks are presented in Fig 2.15. Device sizes and bias conditions are chosen based on the criteria set in section 2.2.1 for maximum high speed operations [Rei96]. The output nodes of the slave latch of the MS-FF, prior to the emitter followers, are routed in the feedback path and connected to the selector inputs ($Sel_{P/N}$). This lowers the fan-out of the slave latch and adds the interconnect capacitance at the internal node which can be compensated for with shunt peaking. Bias currents in the selector and latches, excluding the emitter followers, are set to the same value to have 1 to 1 loading (fanout of 1) along the feedback path.

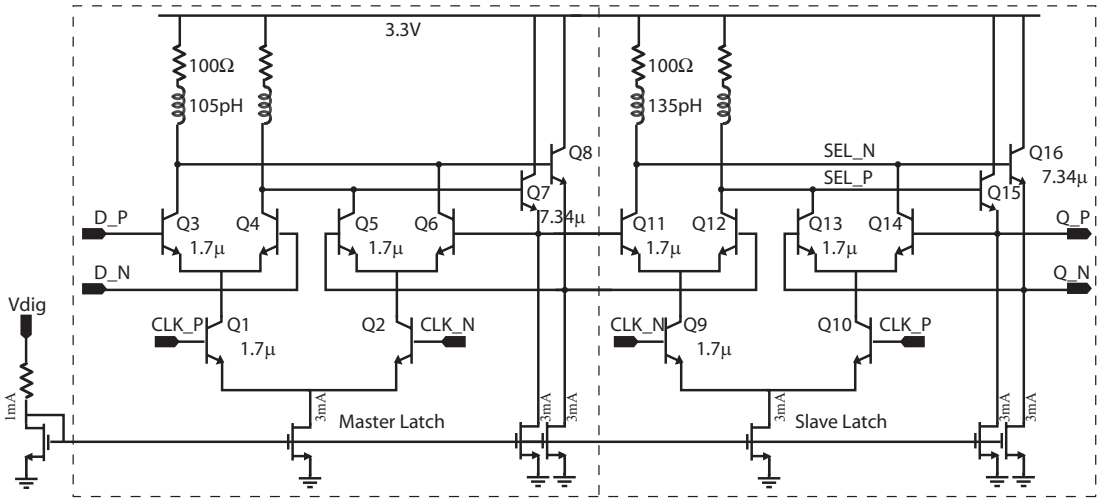
The critical path of the DSF is from the clock inputs to the inputs of the flip flop (Fig 2.16) including the setup time. The delay through this path must be less than 1 bit period (25ps at 40-Gbps). Much of the following discussion involved the analysis of the propagation delay and the resulting design choices.

Critical Path Design

The propagation delays of high speed CML/ECL cells are extensively covered in [Fan90] and most recently in [CML05]. In [CML05], a very lengthy equation is pre-



(a)



(b)

Figure 2.15: ECL schematic (a) selector and (b) MS-FF

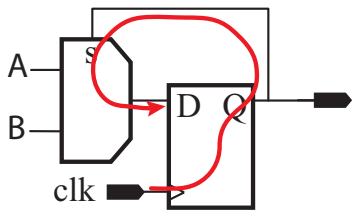


Figure 2.16: Critical propagation feedback path of DSF

sented to represent the propagation delay through a bipolar flip flop. The equation itself, however provides little intuition into the design of the feedback path of interest. In [DBV05] the propagation delay of an HBT cascode pair is simplified to the major contributors and is presented in equation 2.13. Even though the equation is not exact, it does provide design insight. From equation 2.13 there are three general contributors to the propagation delay of an HBT cascode: the transistor time constants, the parasitic interconnect capacitance, and the load resistance.

$$\tau_{pd} \approx \frac{\Delta V(C_\mu + C_{cs} + C_{int})}{I_t} + (k + \frac{R_b}{R_l})R_l(C_\pi + (1 - A_v)\, C_\mu) + \frac{C_\pi + C_{cs} + C_\mu}{g_m} \quad (2.13)$$

where

ΔV is the voltage swing of the ECL block
I_t is the tail current of the ECL block
R_l is the load resistance, $R_l = \frac{\Delta V}{I_c}$
R_b is the base resistance of the transistor
C_μ is the base-collector capacitance of the transistor
C_π is the base-emitter capacitance of the transistor
C_{cs} is the collector-substrate capacitance of the transistor
C_{int} is the interconnect capacitance
g_m is the transconductance of the transistor
k is the stage-to-stage size scaling factor (fanout), 1 for this feedback path
A_v is the gain of the input transistor of the cascode, approximately -1

The transistor time constants are determined by the transistor parasitic capacitance (C_μ, C_π, C_{cs}) and resistances (R_b, $1/g_m$). These terms also appear in the f_t and f_{max} equations and can be minimized by biasing at a collector current density of J_{peakft} [TN98].

Since the transistor time constants are strongly dependant on the collector current density, and weakly on the collector current, low bias currents could be used to minimize the power consumption. However, at low collector currents, the interconnect capacitance (C_{int}) dominates the propagation time. Therefore, in order to minimize this effect, the interconnect capacitance should be decreased and a collector current should be selected which is power efficient, yet minimizes the propagation dependence on C_{int}.

Lastly, the load resistance can be decreased for the same tail current (i.e. an ef-

fective decrease in the voltage swing, ΔV) to minimize the propagation time. There is a limit to how small the voltage swing can be made while still providing functionality. From [CML05], the minimum voltage swing required to switch the following differential pair is

$$\Delta V \geq 6V_t + I_c R_e \tag{2.14}$$

where $V_t = kT/q$ and R_e is the emitter resistance. For negligible emitter resistances, this is a swing of 150mV at room temperature. For noise immunity reasons the voltage swing is often kept larger than this minimum value.

Using the general design guidelines, the ECL is biased near J_{peakft}, with a tail current of 3 mA, the interconnect capacitance is minimized by routing the feedback path using the highest metal available and the output logic swing is set to approximately 300 mV to provide enough noise margin for the following ECL stages. The use of inductors also decreases the propagation delay [Lee98]. From simulations, a propagation delay through the critical path is 21 ps without including the feedback interconnect. Using ASITIC, the feedback interconnect is modeled and found to have a distributed total inductance of 150 pH and capacitance of 15 fF. The interconnect model increases the propagation delay to 22 ps. If the timing requirements had not been sufficient, the voltage swing could have been decreased further. Other enhancements, such as a keep-alive current [CML05], are also available, however they are considerably more complicated.

2.2.4 Slicers

The slicer is comprised of 3 cascaded ECL buffers shown in Fig 2.17. A single buffer could not be used since it would not provide the required gain while maintaining the system bandwidth. Emitter degeneration of the differential pair ($Q_{1/2,7/8,11/12}$) was used to reduce the small signal gain of each of the buffers and to distribute it between the 3 stages. A simulated gain of 5.5 dB per stage is achieved with an aggregated small signal bandwidth of 27 GHz, which is adequate for a 40-Gbps system.

Buffer 1 and 3 of the slicer use differential cascode amplifiers to lower the Miller effect on the input transistor ($Q_{1/2,7/8,11/12}$). A cascode amplifier was not employed for the second buffer since a lower common-mode voltage at the emitter of $Q_{5,6}$ would be required so that the cascode transistor would not saturate. In order to achieve the CM shift two methods were investigated and ultimately discarded. Cascaded emitter followers could have provided the correct CM level for the second buffer,

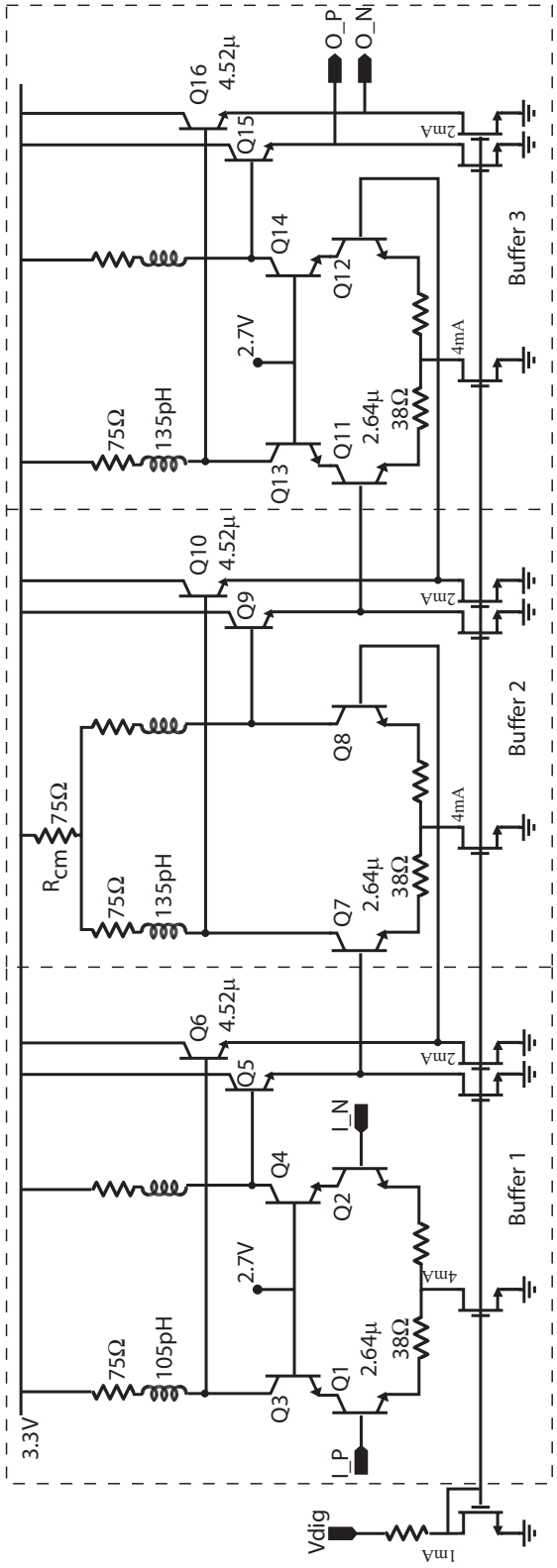


Figure 2.17: Slicer schematics (3 cascaded ECL buffers)

as well as increased the overall bandwidth of the slicers. The frequency response of multiple emitter followers however has the potential to be underdamped due to parasitic line inductance or the negative input impedance of the EF stages causing significant "ringing" in the large signal response [Rei96]. Another method would employ a diode connected transistor at the output of the emitter follower ($Q_{5,6}$) to provide the CM shift. The additional capacitance of the diode transistor decreases the bandwidth of the slicer more significantly than the advantages of the cascode amplifier. Since a bandwidth efficient CM level shift was not available a cascode amplifier was not used in the second stage. The common-mode resistor (R_{cm}) in the second buffer does however provide a DC shift to lower the common-mode voltage into the third buffer allowing a cascode amplifier to be used.

It is found from simulations (Fig. 2.18) that the second buffer is limiting the bandwidth of the overall system. To improve the bandwidth, the gain could be redistributed so that buffer 1 and 3 has less emitter degeneration (i.e. higher gain) than the second buffer. This could have improved the overall bandwidth of the system without decreasing the system-level gain.

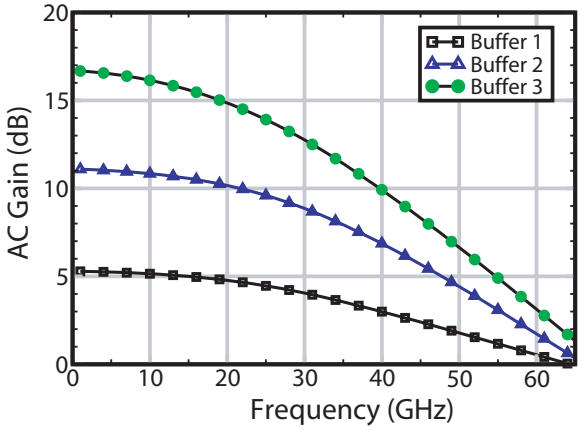


Figure 2.18: Slicer buffer AC frequency response

2.2.5 Output Driver

The output driver (Fig 2.19) consists of a pre-amplifier and output buffer with an emitter follower between the two stages. Emitter degeneration is employed for both the pre-amplifier and output buffer to decrease the small signal gain of the entire driver as well as increase the bandwidth. The output buffer has a 50 Ω load resistance

to achieve broadband matching. A bias current of 16 mA for the output buffer provides a 2x400 mV_{pp} voltage swing across an equivalent 25 Ω impedance (50 Ω load resistance in parallel with 50 Ω termination resistance). The pre-amplifier common-mode resistor, R_{cm}, lowers the common-mode voltage at $A_{P,N}$ to maximize the V_{CE} on the output buffer transistors, $Q_{5,6}$. This is used because the DC common-mode voltages at the outputs (O_P/N) are lower than previous ECL blocks. Independent tail current control of the output driver, includes the pre-amplifier, allows for variable voltage swing.

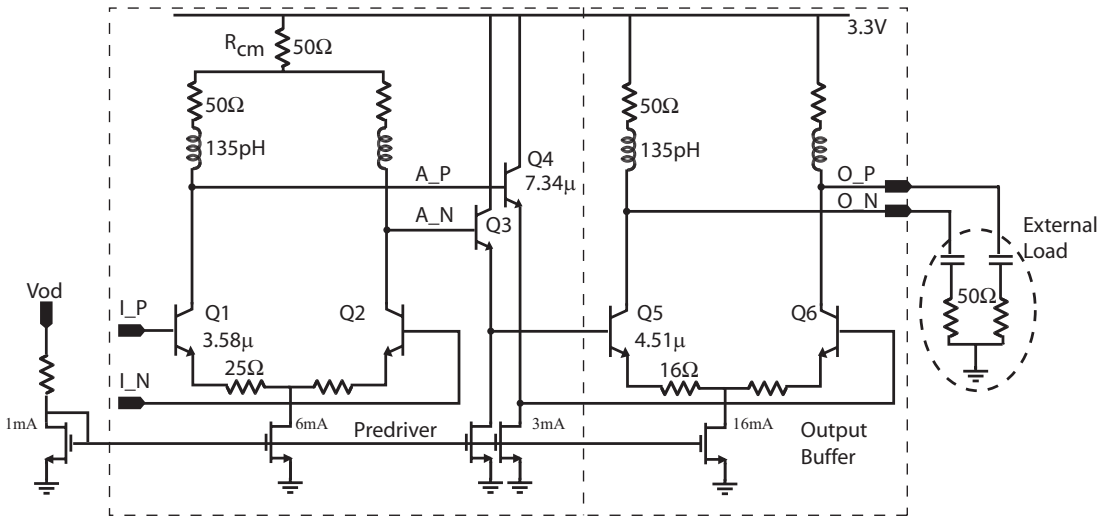


Figure 2.19: Output driver schematic including the pre-amplifier and output buffer

Fig. 2.20 shows the simulated small signal frequency response of the output driver. The plot includes the simulation results with the prefabrication design kit models as well as the recently updated design kit, post fabrication. An output driver with a gain of 3 dB and a bandwidth of 45 GHz was originally designed. The updated design kit shows the output driver also has a 3 dB gain at DC; however, the frequency response has 2 dB of peaking and a total bandwidth of over 60 GHz. Even though the output driver is still functional, the updated design kit simulations indicate that there will be more data dependent jitter and clock feed through at the output. It is not clear, without further investigation, what specific models were updated that has lead to the simulation mismatch.

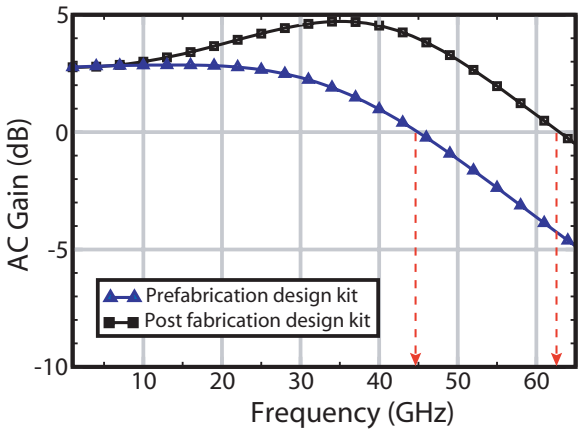


Figure 2.20: Simulated output driver AC frequency response using the prefabrication and post fabrication design kit

2.2.6 Clock Path

The clock distribution network can be seen in Fig. 2.21. The inputs into the emitter followers ($Q_{1,2}$) are matched with on-chip 50 Ω resistors to the power supply voltage. Unlike the data path, which uses a TIA stage, a high sensitivity input amplifier is not required. Cascaded emitter followers were used to increase the bandwidth of the system since a bandwidth of at least 50 GHz was desired for the 40 GHz clock path. The potential "ringing" caused by the double emitter follower is less of a concern, as long as it is stable, given the clock signal is narrowband. The clock buffer has an internal output that feeds the flip flop and an external output which is driven off chip. It is intended that the external output could be used as a trigger signal for the oscilloscope if high frequency splitters are not available during testing. The external output has a voltage swing of 2x300mV.

Fig. 2.22 shows the simulated small signal frequency response of the clock buffer, to the internal and external outputs, for both the prefabrication and post fabrication design kit. A clock buffer with 3.5 dB gain and a bandwidth of 55 GHz to the external outputs was designed. Similar to the output driver, the frequency response of the clock path differ between the design kits.

2.3 Time-domain Simulations

Time-domain simulations were conducted to obtain the large signal performance of the DFE. The random input data stream is passed through a PMD channel with γ

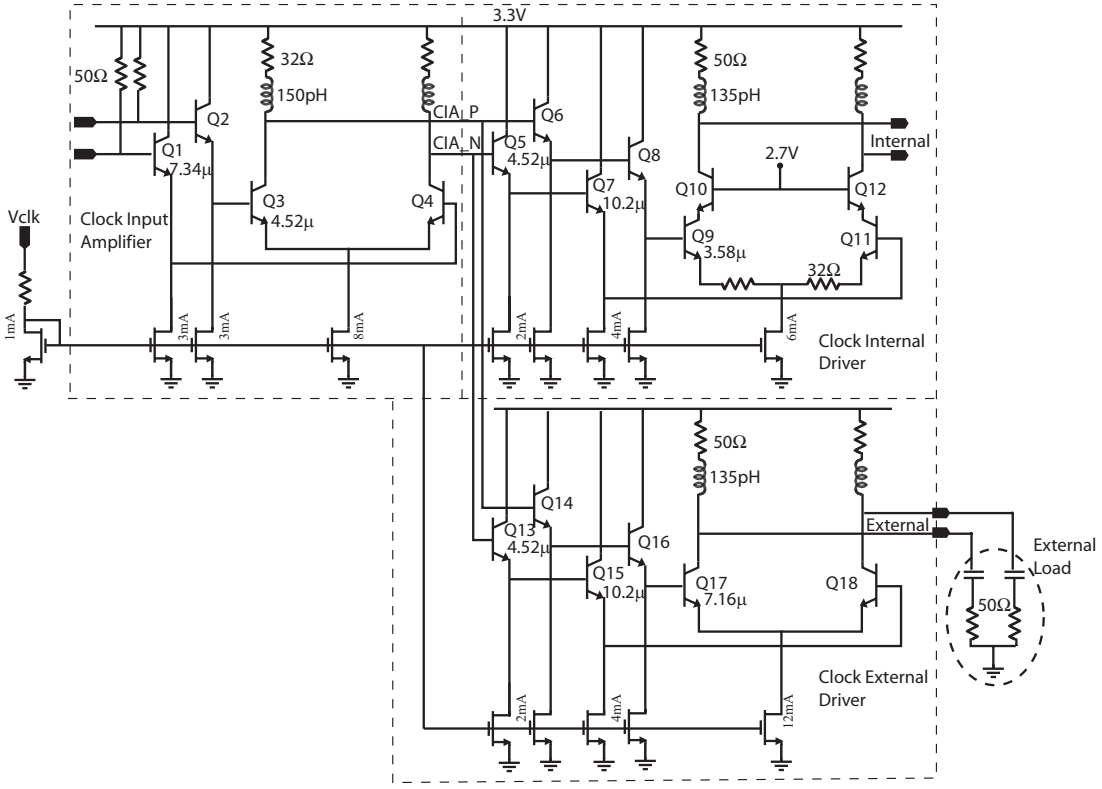


Figure 2.21: Two stage clock buffer schematics

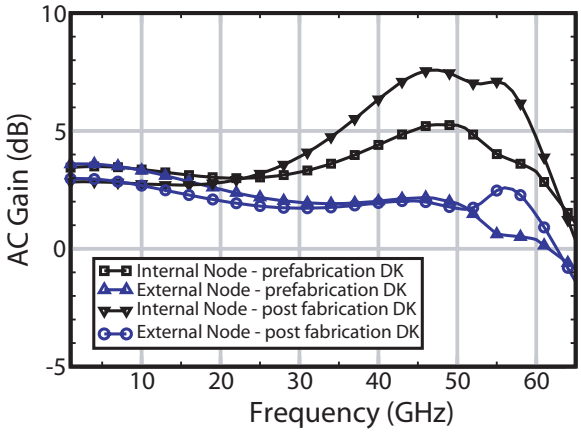
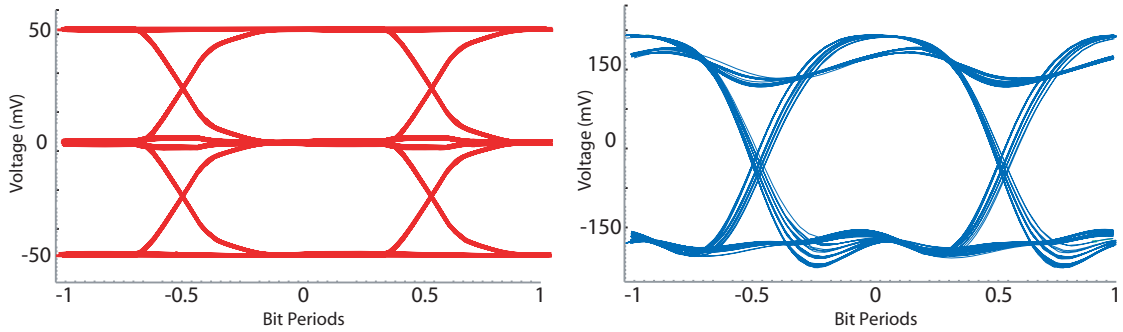


Figure 2.22: Simulated clock path AC frequency response using the old and updated design kit

of 0.5 and $\Delta\tau$ of 25 ps and is shown in Fig. 2.23(a). As mentioned previously in Chapter 1, this is the channel condition which cannot be handled by an FFE alone and specifically requires a DFE. The use of a random source is sufficient at stressing the functionality of the DFE given the impulse response of the channel is relatively short. The equalized output eye diagram is shown in Fig. 2.23(b). The output shows a superimposed clock ripple on the output eye due to the clock feed through from the flip flop to the output. The data dependant peak-to-peak jitter is 1.3 ps, with a rise and fall time of less than 6 ps. The differential tap voltage ($\alpha_P - \alpha_N$) was set to 100 mV. The bit sequence of 400-bits was manually verified for error free operation.



(a) (b)

Figure 2.23: Simulated single-ended eye diagrams (a) corrupted input eye diagram through a PMD channel with γ of 0.5 and $\Delta\tau$ of 25 ps (b) equalized output eye diagram

2.4 Conclusion

In this chapter, the complete design of the 40-Gbps DFE has been described. Each block has been presented with detailed discussion of the design choices and biasing conditions. Simulation results have been provided which demonstrate the expected performance of the equalizer. The following chapter presents the measured results.

3 Fabrication and Measurements

This chapter presents the measurements of the 40-Gbps DFE fabricated in Jazz Semiconductors' SBC18HX 0.18μm SiGe BiCMOS technology with a 160-GHz f_t [RK03]. Ideally, a 40-Gbps bit error tester (BERT) through a fiber optical channel, or PMD emulator, would have been used to verify the functionality of the test chip; however, in the absence of such system, a series of small signal and large signal tests were completed. The aim of the following chapter is to characterize the DFE.

Section 3.1 presents the test chips fabricated based on the design in Chapter 2. Section 3.2 summarizes the results of the S-parameter measurements including the breakout front end bandwidth and return loss of the high speed ports of the DFE. The P_{1dB} of the front end breakout and the variable tap weight tuning are presented in section 3.3. The bit error measurements at 5, 6 and 10 Gbps through a PMD emulating board and 20-ft SMA cable are demonstrated in section 3.4. Lastly, section 3.5 outlines the measurement results at 35Gbps to 39.5Gbps including verification of the correct bit sequence using an Agilent 86100C oscilloscope. All measurements were performed on wafer.

3.1 Circuit Layout

The die photo of the DFE test chip is seen in Fig. 3.1. It closely matches the block diagram in Fig. 2.3. The inputs on the left feed into the shunt-series feedback input stage. The clock input is applied from the bottom of the die with the DC control and supply voltages at the top. The DC voltages allow for multiple VDD pads to abide by electromigration rules as well as decrease the voltage supply's series resistance. The same is true for the ground pads. Individual functional blocks have tail current control which can be used to change, increase or decrease the bandwidth or the voltage swing. These blocks include the broadband front end (Vbfe), the digital core with the slicer and DSF (Vdig), the output driver (Vod), and the clock buffers (Vclk). Differential α control is also available to set the tap weight of the equalizer. The right side has

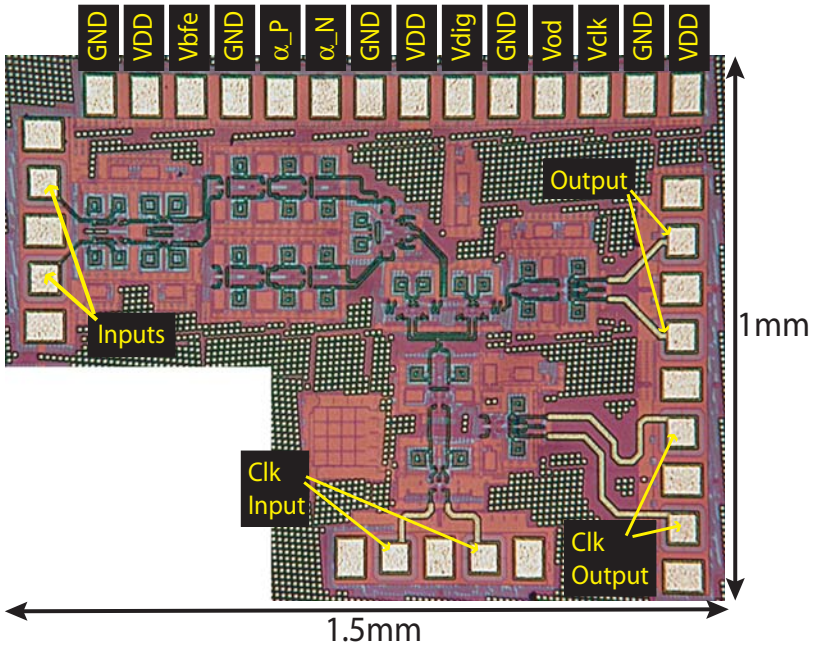


Figure 3.1: DFE fabricated in Jazz Semiconductors' SBC18HX 0.18μm SiGe BiCMOS technology with a 160-GHz f_t operating from a 3.3 V supply with 230 mA current.

two sets of differential outputs for the clock and data. The IC occupies an area of 1.5 mm^2 and operates from a 3.3 V power supply and draws 230 mA of current, of which 60 mA is for the clock path.

A die photo of the broadband front end breakout is presented in Fig. 3.2. The broadband breakout was fabricated to have access to the linear portion of the equalizer. It allows the characterization of the differential tap weight tuning, the broadband linearity and small-signal 3dB bandwidth. The inputs are on the left and the outputs of the threshold circuits are on the right and bottom. The DC input pads for the supply voltage, reference current voltage (Vbfe) and the differential threshold tuning voltage (α) are located at the top.

3.2 S-parameter Measurements

Single-ended S-parameter measurements, with the other differential input/output terminated with 50 Ω, were performed using a Wiltron 360B vector network analyzer

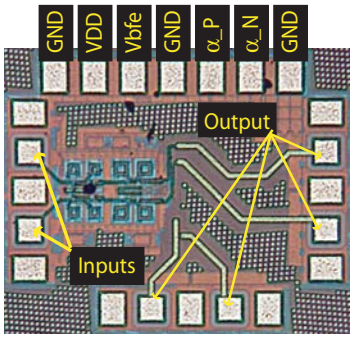


Figure 3.2: Broadband front end fabricated in Jazz Semiconductors' SBC18HX 0.18μm SiGe BiCMOS technology with a 160-GHz f_t operating from a 3.3 V supply with 30 mA current.

(VNA), seen in Fig. 3.3[1]. These small signal measurements are used to determine the high speed performance of the DFE. Measurements show the single-ended return loss (Fig 3.4(a)) of all the high speed ports for the DFE to be better than -10 dB up to 40 GHz. The bandwidth along the linear path from clock input to clock output (S_{43}) is shown in Fig. 3.4(c). A bandwidth greater than 50 GHz is achieved for the clock distribution; however, there is excessive peaking near 40 GHz. This is attributed to the use of cascaded emitter followers and the parasitic inductances within the layout. With proper layout and design, the peaking can be minimized, which is observed by lowering the bias current of the clock path, Fig. 3.4(d).

The VNA was also used to determine the 3dB bandwidth of the linear portions of the data path. Single-ended S-parameter measurements of the front end breakout, through the TIA and the top threshold adjustment circuit, with the other outputs terminated, demonstrate a bandwidth of 45-GHz up to the slicers. The left-to-right path is used to measure the bandwidth since calibration is considerably easier and valid to a higher frequency. Given that the measurements are single-ended, the differential gain is 6 dB higher than that presented in Fig. 3.4(b). The full data path bandwidth could not be measured due to the nonlinear decision circuit.

3.3 Broadband Front End Breakout Characterization

The broadband front end breakout was tested to determine the systems equalization performance. The following sections present the measured linearity and offset voltage

[1]It should be noted that the VNA does not perform 4-port measurements and Fig. 3.3 only provides reference port numbers for the data and clock inputs/outputs.

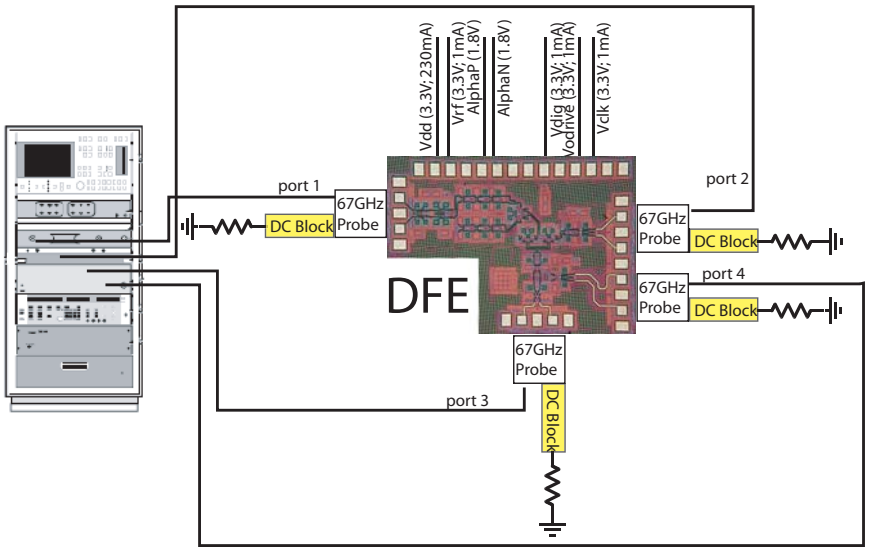


Figure 3.3: S-Parameter measurement setup

tuning characteristics.

3.3.1 Linearity

The P_{1dB} was measured to determine the linearity of the circuit over a wide range of frequencies. A single signal source is applied to the input and the corresponding power output is measured via a power meter (Fig. 3.5). To get accurate measurements, the input and output cable/probe losses were de-embedded. Measurements at 1, 5, 10, 15, 20, and 30 GHz are presented in Fig. 3.6(a). A P_{1dB} of -7.5dBm is achieved up to 20 GHz (Fig. 3.6(b)).

The single-ended spectra of the output at the 1dB compression point for 5, 10, and 20 GHz are seen in Fig. 3.7. Total harmonic distortion (THD) of the front end breakout can be calculated using equation 3.1, where P_i is the power (W) in the i^{th} harmonic.

$$THD = \frac{P_2 + P_3 + \cdots + P_i}{P_1} * 100\% \tag{3.1}$$

The THD at the 1dB compression point is 0.62%, 1.09%, and 2% at 5, 10 and 20 GHz respectively. If differential measurements were conducted, the actual THD would be slightly lower since the second order harmonic would be suppressed significantly. The third order harmonic of the 20 GHz signal was not seen since it was outside the spectrum analyzer bandwidth and most likely the bandwidth of the breakout.

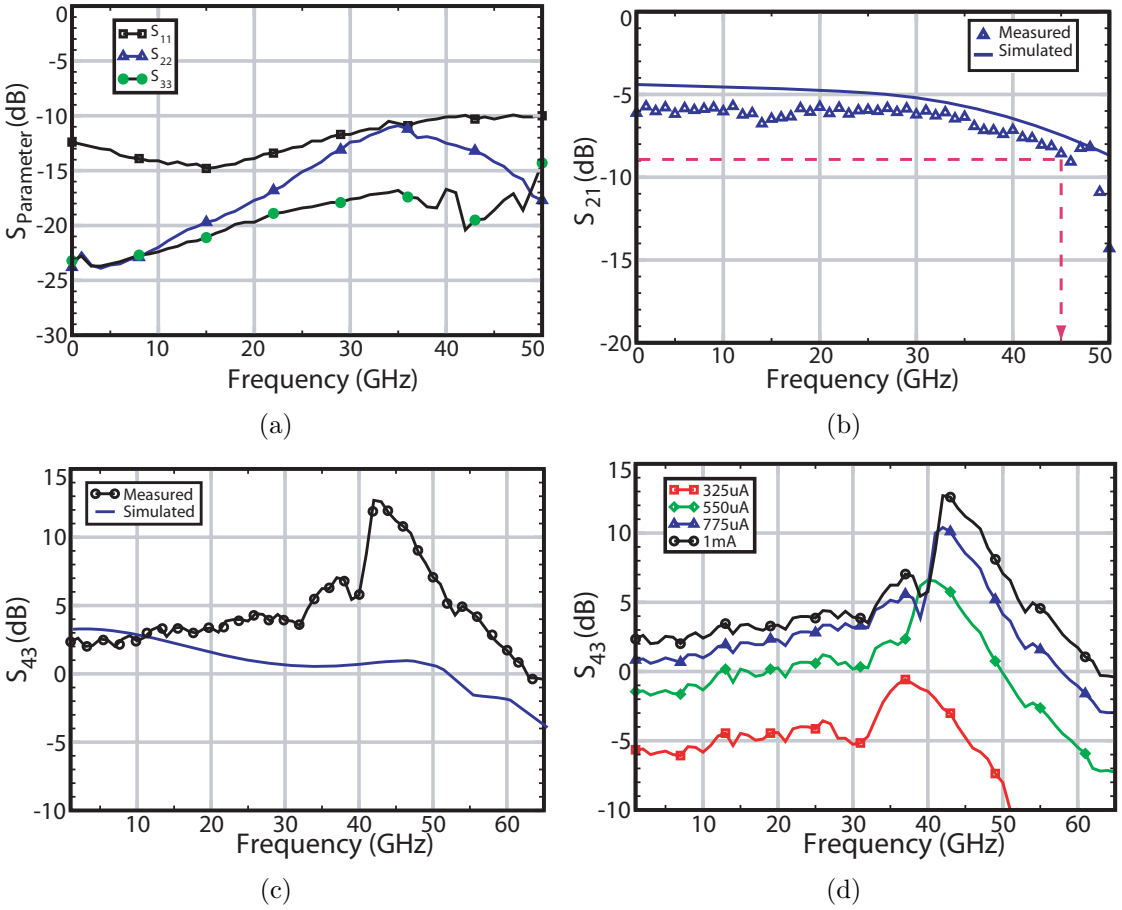


Figure 3.4: S-Parameter (a) measured return loss for input, output and clock path, (b) measured and simulated broadband front end bandwidth, (c) measured and simulated clock path frequency response and (d) measured clock path frequency response for various reference currents

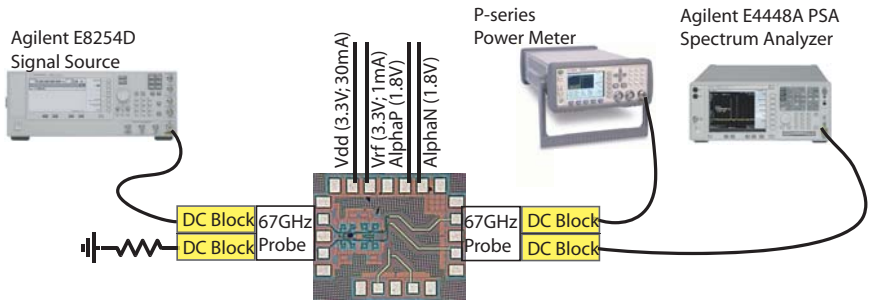
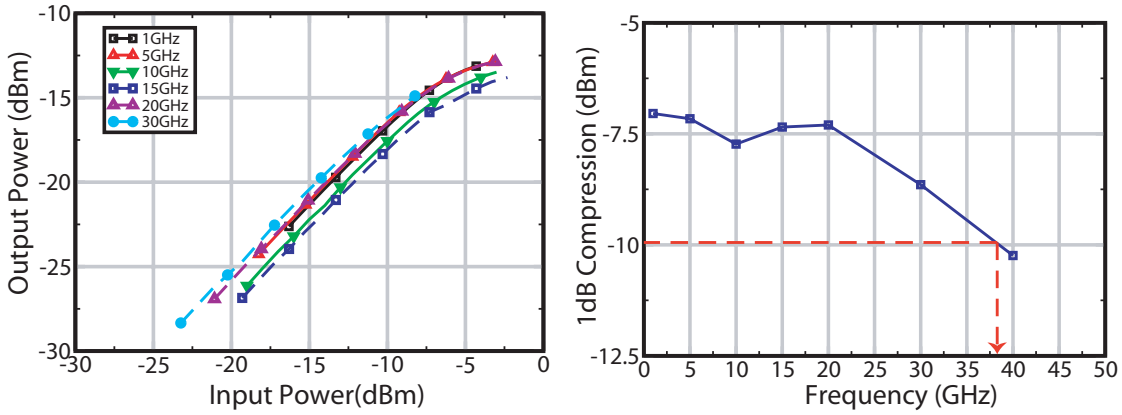


Figure 3.5: P_{1dB} measurement setup for the broadband front end breakout



(a) (b)

Figure 3.6: Linearity measurement of the broadband front end breakout (a) P_{1dB} at 1, 5, 10, 15, 20, and 30 GHz (b) 1_{dB} compression point as a function of frequency

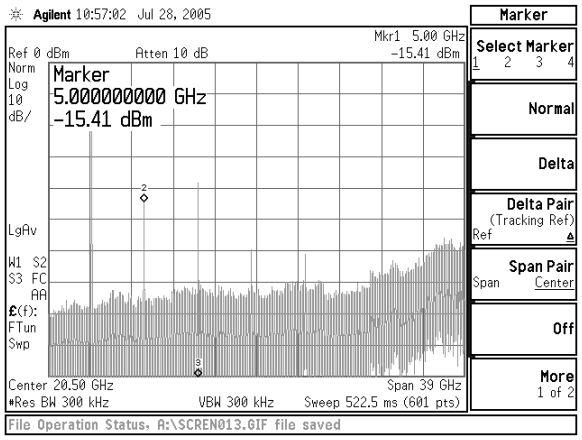
3.3.2 Threshold Adjustment

The differential tap weight $(\alpha_p - \alpha_n)$ was swept and the corresponding DC offset at the output of the threshold adjustment circuit was measured (Fig. 3.8). Measurements show a linear tuning characteristic between the output offset and differential tap weight. From Fig. 3.8, the measured output offset versus tap weight tuning slope is 0.15, compared to a simulated slope of 0.24. This indicates the g_m of the MOS differential pair is less than that seen in simulations. Also from measurements, there is an 11 mV_{pp} output referred offset voltage into the slicer. Given that the differential gain is 8 dB, the input referred offset voltage of the broadband front end is approximately 4 mV_{pp}.

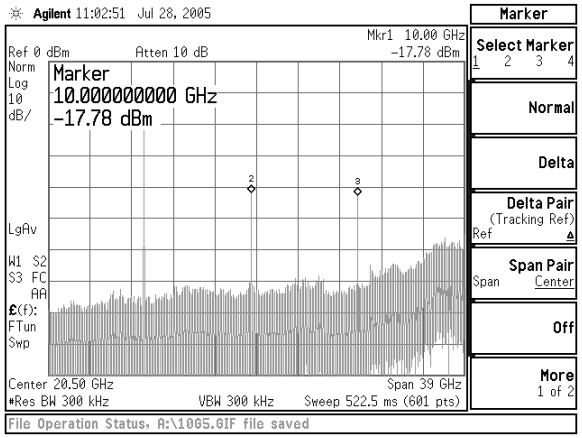
3.4 Bit Error Measurements

3.4.1 Measurement Setup

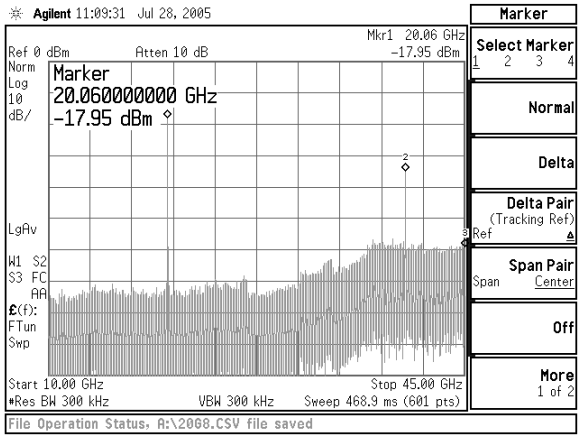
The measurement setup of the BERT is presented in Fig 3.9 and schematically represented in Fig. 3.10. This 10-Gbps BERT measurement runs off a single clock source, where one OTB3P1A Centellax 10-Gbps board is configured as a $2^{31} - 1$ PRBS generator and the other board is connected as a PRBS error checker. PRBS data is fed through a dispersive channel, PMD-emulating board and 20-ft SMA cable, into the equalizer. One of the equalizer outputs is displayed on the Agilent oscilloscope and



(a)



(b)



(c)

Figure 3.7: Spectrum of broadband front end at P_{1dB} compression point (a) 5 GHz, (b) 10 GHz and (c) 20 GHz

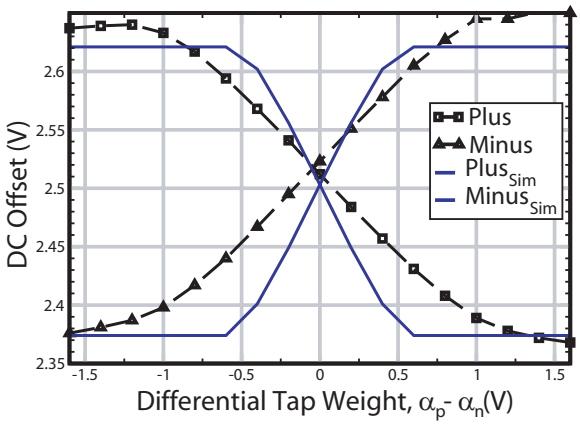


Figure 3.8: Measured and simulated output offset as a function of differential tuning voltage (α)

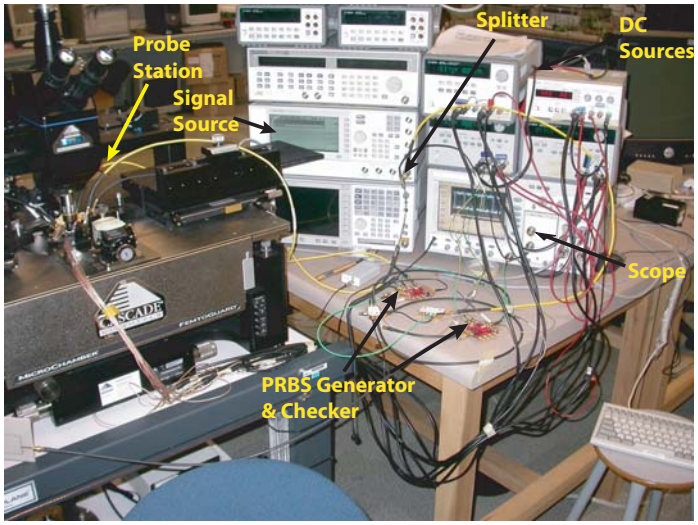


Figure 3.9: BERT measurement setup

the other is connected to the error checker. Channel 4 on the Agilent oscilloscope displays the error trigger. If a transition occurs, a bit error is detected. A jumper on the error checker is removed to allow the incoming and internal PRBS patterns to synchronize. Replacing the jumper starts the error checking. A sample measurement (Fig. 3.11) shows how an error free output (Fig. 3.11(a)) generates no transitions on the error trigger where as an erroneous output generates transitions on the trigger (Fig. 3.11(b)).

BERT measurements were conducted for two channels up to 10-Gbps. The two targeted channels were a PMD emulating board and a 20-ft SMA cable with 16 dB attenuation at 5 GHz.

3.4.2 PMD Emulating Channel Measurement Results

The PMD emulating board (Fig. 3.12) was designed by Jeremy Corbeil as part of his undergrad project at the University of Toronto. It emulates a PMD channel with a γ of 0.5 and $\Delta\tau$ of 200 ps. The frequency response of the channel (Fig. 3.13) shows a 30 dB null at 2.5 GHz. This results in the input eye diagrams in Fig. 3.14 for a $2^{31}-1$ PRBS pattern at 5 and 6 Gbps. The equalized single-ended output eye diagram, with an α of 0.2, is shown in Fig. 3.15. Fig. 3.15 has no transition on the trigger indicating error free operation for over 10K measurements. Assuming there are 3 measurements per second, this shows error free operation for over 50 minutes, which corresponds to a BER less than 10^{-12}. The 6-Gbps single-ended output eye has a low peak-to-peak jitter of 5.5 ps, an SNR[2] of 13.66 and a voltage swing of 2x320 mV_{pp}.

3.4.3 20-ft SMA Cable Measurement Results

The frequency response of the 20-ft multi-segment[3] SMA cable (Fig. 3.13) shows a linear (in dB) decrease versus frequency with 16 dB attenuation at 5 GHz. This results in the input eye diagram in Fig. 3.16(b) for a $2^{31}-1$ PRBS sequence at 10 Gbps. The resulting equalized single-ended output eye diagram, with an α of 0.3, is presented in Fig. 3.17. No transition on the error trigger is seen for over 4K measurements or 20 minutes, indicating a BER less than 10^{-12} at 10-Gbps. A low peak-to-peak jitter of 10.22 ps, an SNR of 13.13 and an amplitude of 2x290 mV_{pp} is seen at the output.

[2] $SNR = \frac{V_{pp}}{2V_n(rms)}$

[3] The 20-ft SMA cable was comprised of 9 shorter SMA cables connected in series.

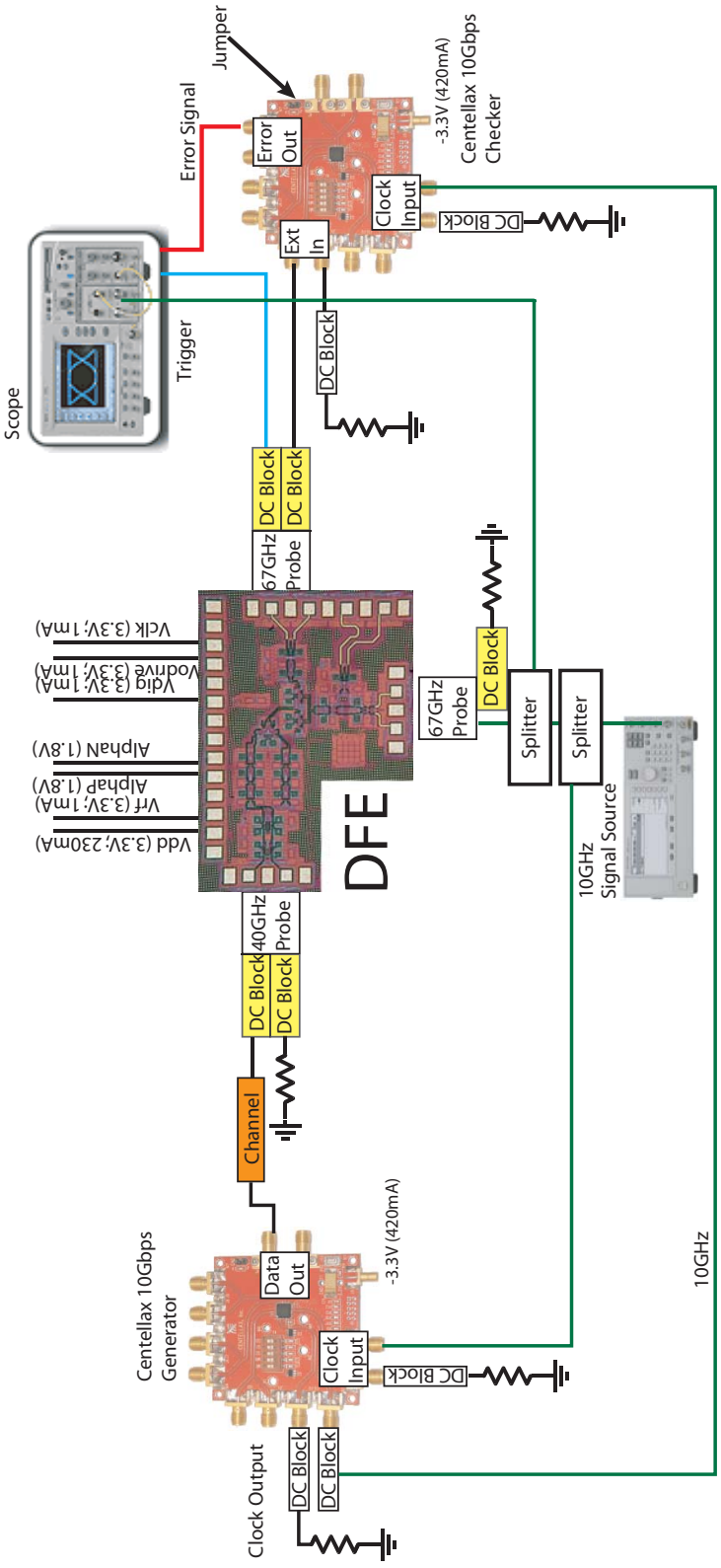
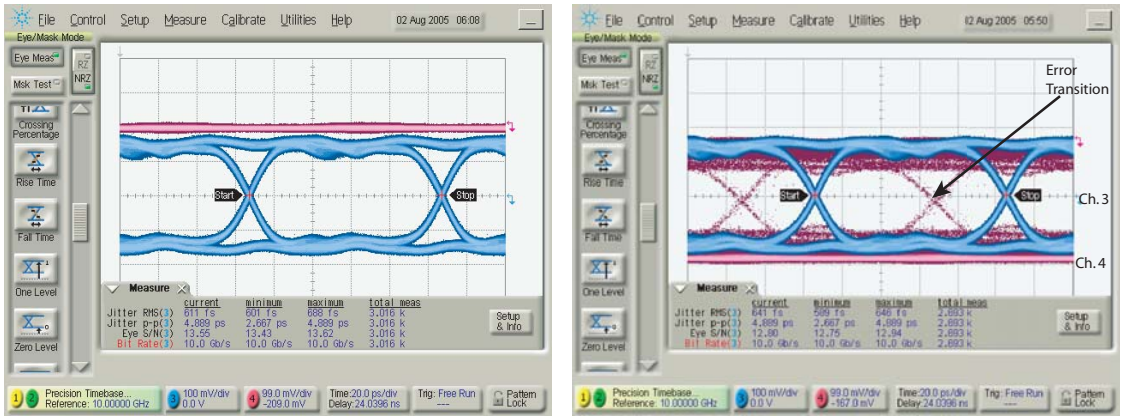


Figure 3.10: BERT measurement schematic setup



(a) (b)

Figure 3.11: Sample BERT measurement (a) error free and (b) erroneous output

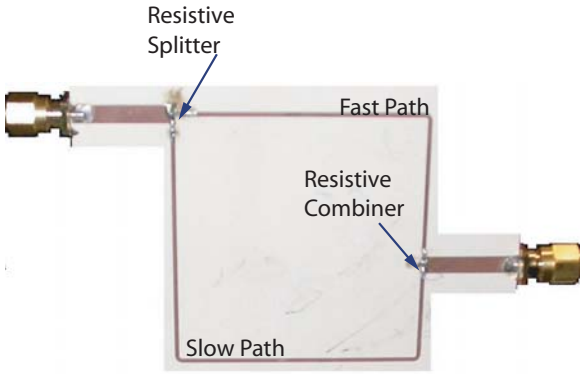


Figure 3.12: Picture of PMD emulating board

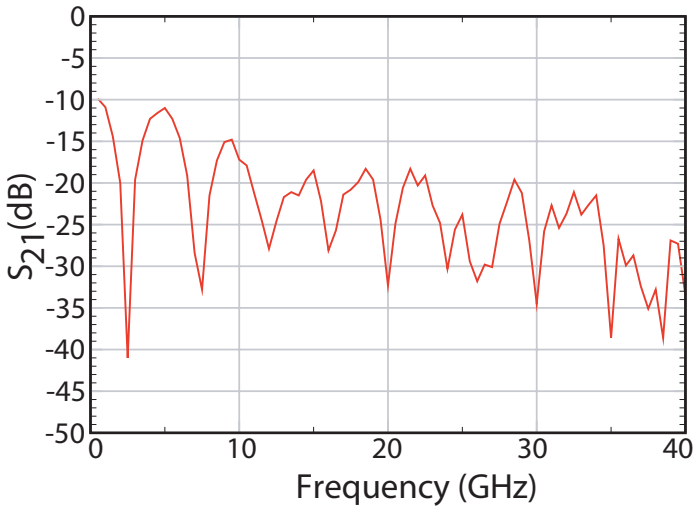
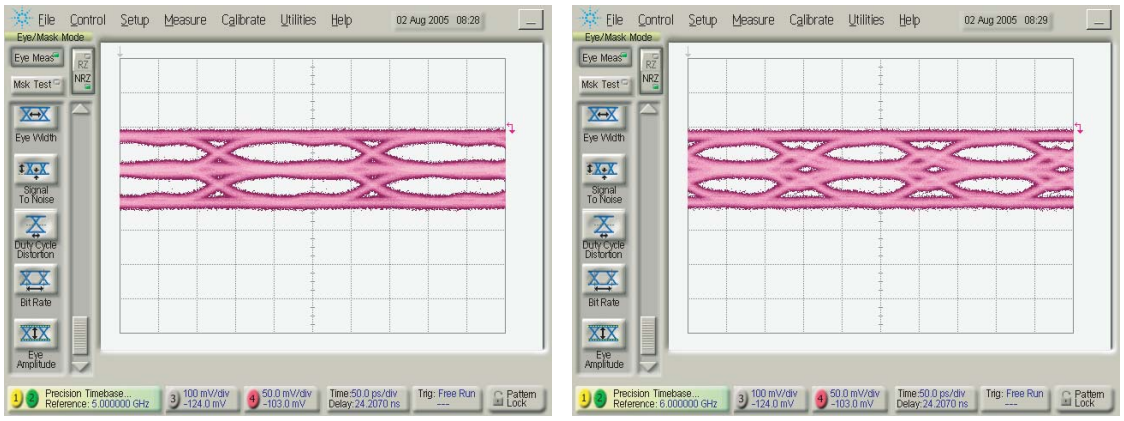
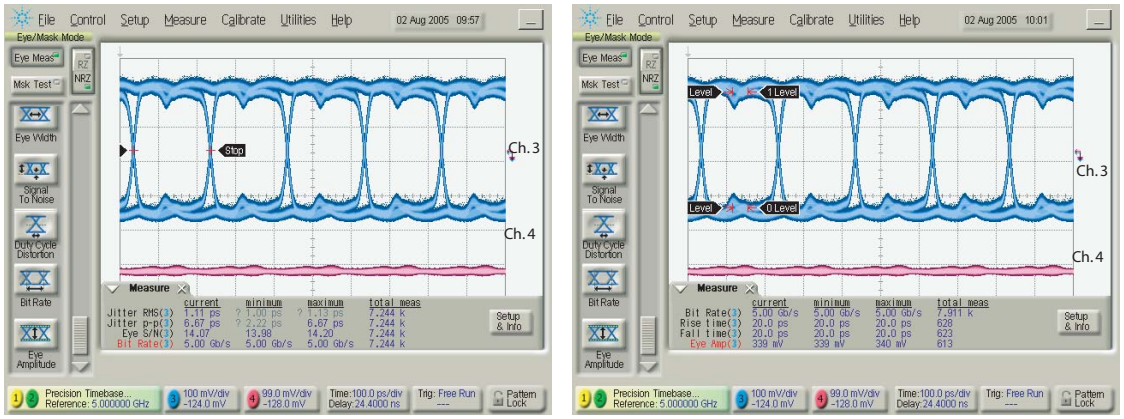


Figure 3.13: Board frequency response

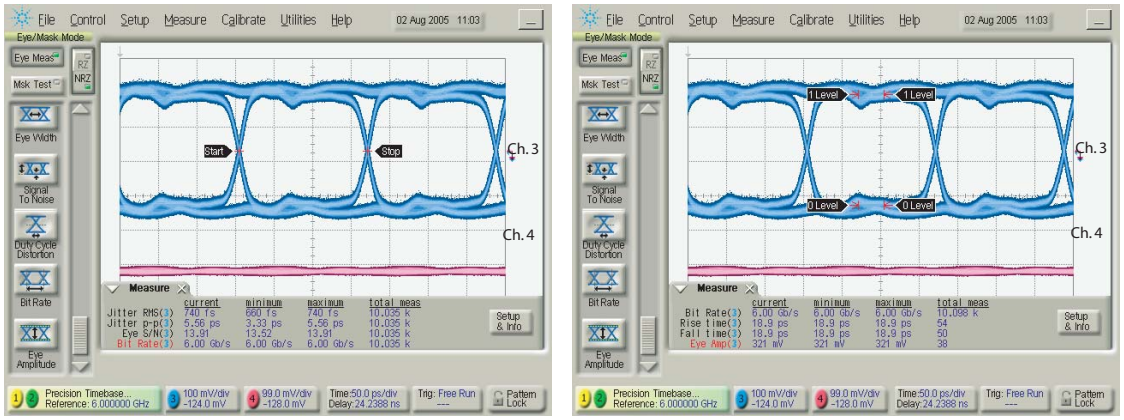


(a) (b)

Figure 3.14: Input eye diagram through the PMD board at (a) 5-Gbps and (b) 6-Gbps

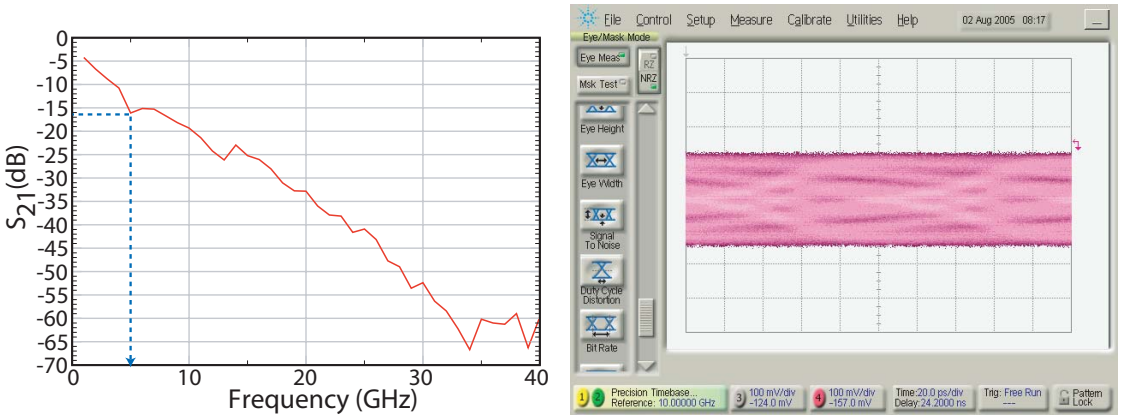


(a) (b)



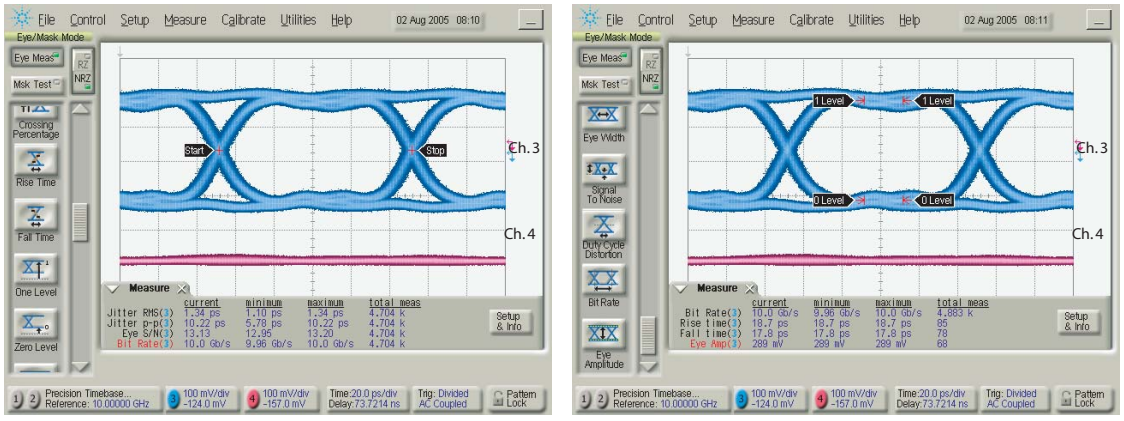
(c) (d)

Figure 3.15: Equalized output eye diagram through the PMD board at (a, b) 5-Gbps and (c, d) 6-Gbps



(a) (b)

Figure 3.16: Channel characteristics over 20-ft SMA cable (a) frequency response and (b) 10 Gbps $2^{31} - 1$ PRBS input eye diagram



(a) (b)

Figure 3.17: 10 Gbps equalized output eye diagram through 20-ft SMA cable

The jitter is significantly higher than the previous measurement since the precision time base of the oscilloscope was not used.

3.5 40-Gbps Equalization Measurements

3.5.1 Measurement Setup

The test setup for 40-Gbps measurements is described in Fig. 3.18. Two Centellax OTB3P1A boards produce 10-Gbps PRBS data which are fed into a multiplexer to generate a 40-Gbps data stream that is 4 times the bit length of the PRBS pattern of

the boards (i.e. a $2^7 - 1$ PRBS configuration results in a 508-bit repeating sequence). Positive and negative outputs of the boards are both used and uncorrelated via different lengths of cables. A single signal source clocks the entire test setup and is passed through a broadband frequency divider to generate the 20 GHz clock for the multiplexer and the 10 GHz clock for the PRBS generators. The oscilloscope displays the equalized single-ended output of the DFE as well as a non-distorted output from the multiplexer. Error checking was performed on the bit sequence manually using the waveform pattern lock feature of the oscilloscope.

3.5.2 Measurement Results

The 40-Gbps data is passed through a multi-segment 9-ft SMA[4] cable with a frequency response shown in Fig 3.19(a). The resulting input eye diagrams at 35 Gbps, 38 Gbps, and 39.5 Gbps are presented in Fig. 3.19(b), 3.19(c) and 3.19(d) for a PRBS board configuration of $2^{31} - 1$, $2^{10} - 1$, and $2^7 - 1$ respectively.

The resulting single-ended equalized output eye diagrams are seen in Fig 3.20. The 39.5 Gbps equalized output has an RMS jitter of 750 fs, a peak-to-peak jitter of 5.11 ps, an SNR of 9 and a voltage swing of 2x324 mV_{pp}. Significant clock feed through at the high data rates can be seen by the ripple on the top and bottom of the eye diagrams. The clock feed through is a common mode signal and would cancel off if the circuit was measured differentially.

Shown in Fig. 3.21 are the ideal (top), an unequalized DFE output (middle) and an equalized DFE output (bottom) waveforms, for a 508-bit sequence, captured by the Agilent 86100C oscilloscope. Errors in the unequalized output are indicated by an arrow on top of the bit pattern. The recovered sequence was compared against the ideal waveform by hand to verify error free operation. It provides a functional verification of the error free output bit sequence after equalization.

Using the Agilent oscilloscope, the jitter characteristics were obtained for the 39.5-Gbps, 508-bit sequence. The bathtub curve for the output eye diagram (Fig. 3.22(a)) indicates a timing margin of 0.75UI, with a total jitter of 6.13 ps. The total jitter has a significant data dependant jitter (DDJ) component (Fig. 3.22(b)) and is most likely caused by the peaking in the frequency response of the output driver seen in simulations using the updated design kit.

[4]The 9-ft SMA cable is comprised of 3 3-ft SMA cables connected in series.

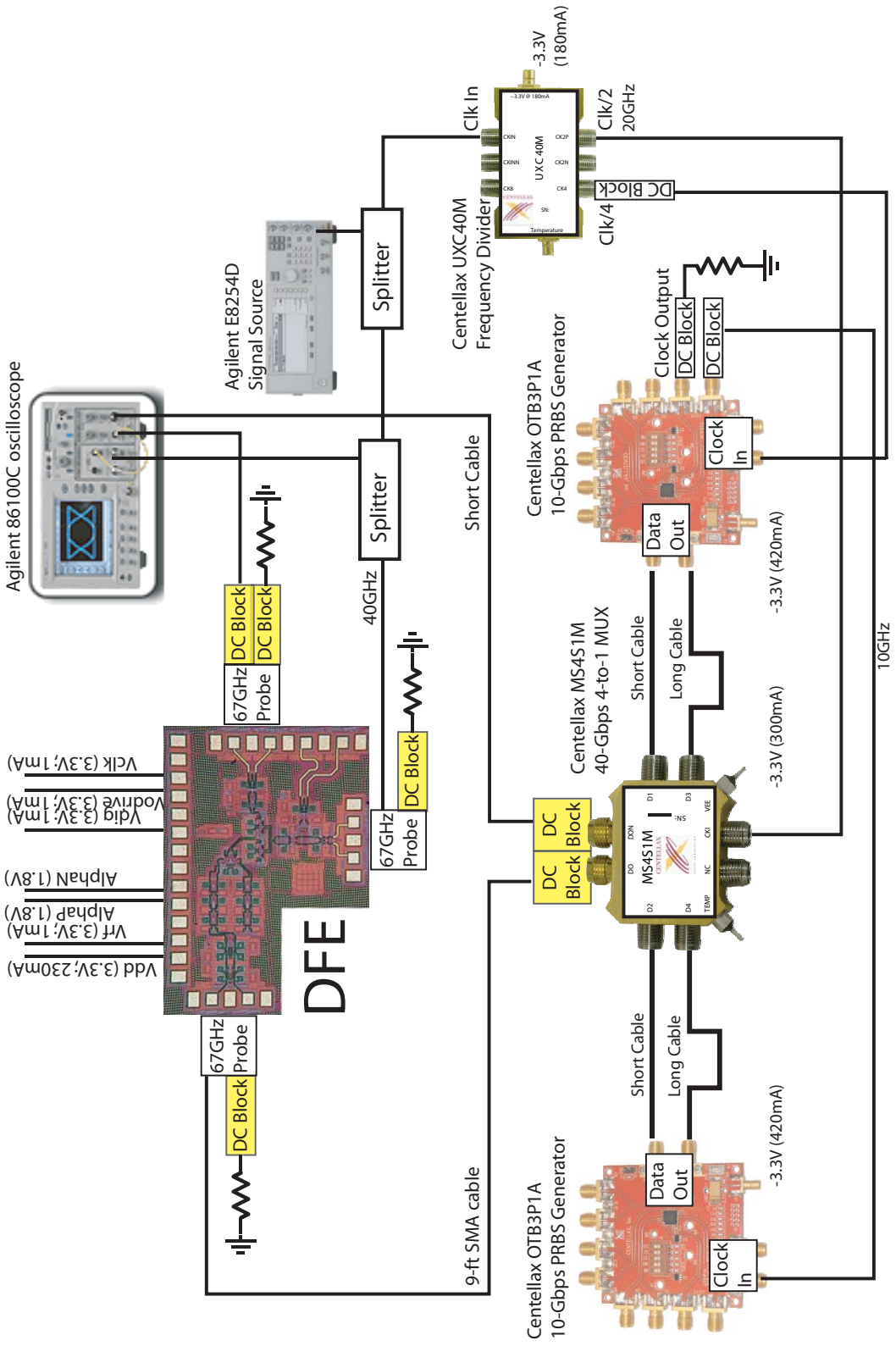


Figure 3.18: 35-40 Gbps measurement test setup

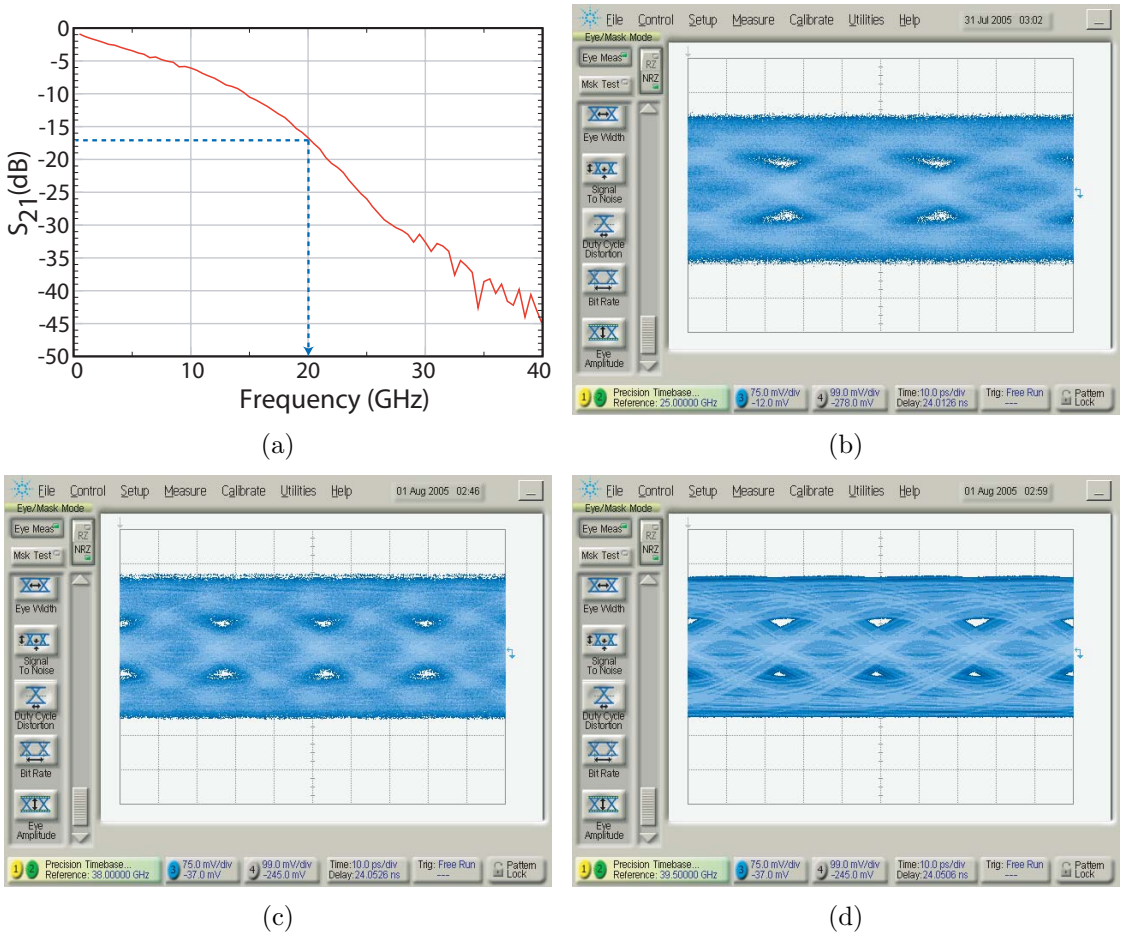


Figure 3.19: 9-ft SMA cable characteristics (a) frequency response, (b) $2^{31}-1$ PRBS input eye at 35 Gbps, (c) $2^{10}-1$ PRBS input eye at 38 Gbps, (d) $2^{7}-1$ PRBS input eye at 39.5 Gbps

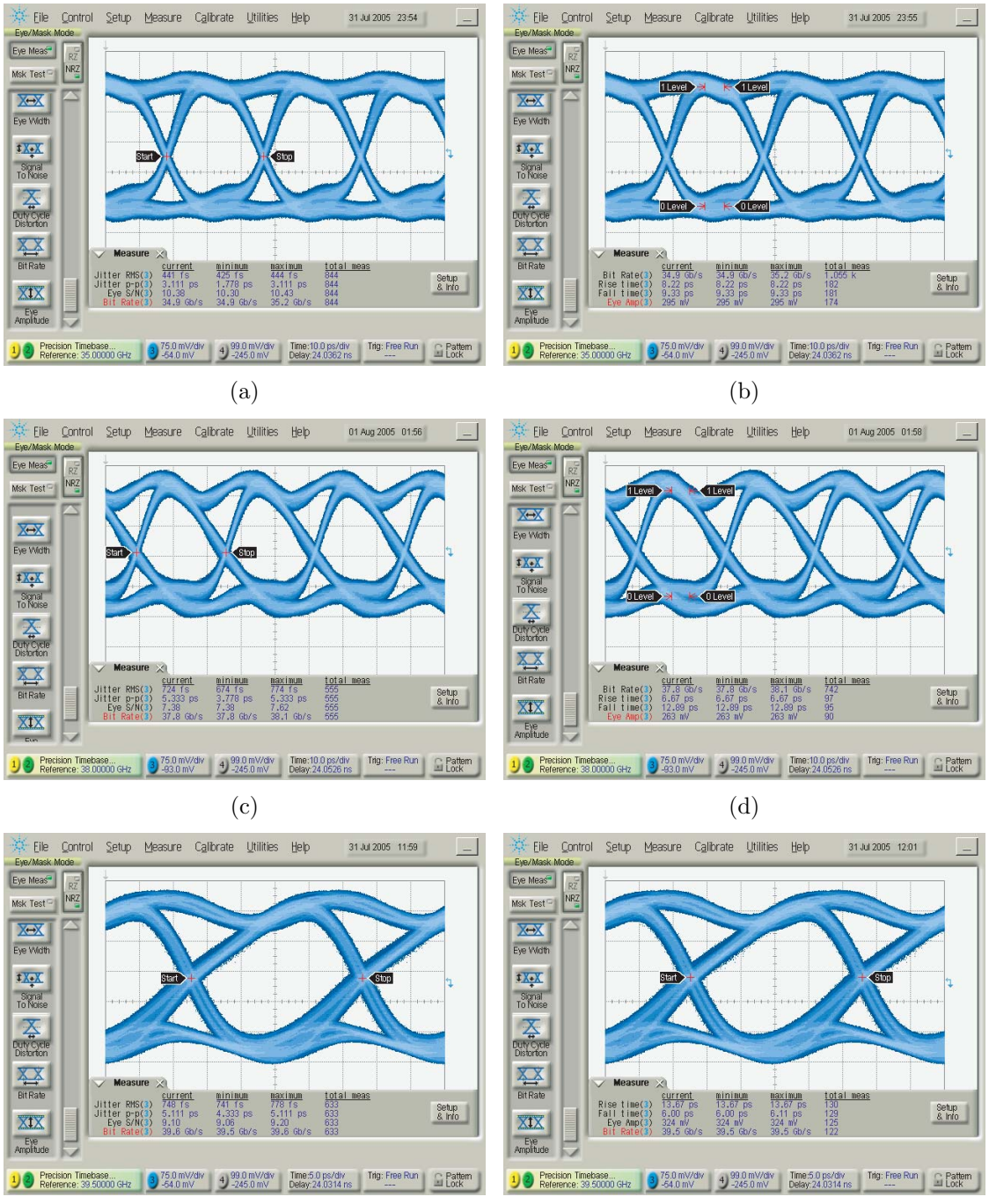


Figure 3.20: Single-ended equalized output eye diagram at (a, b) 35-Gbps, (c, d) 38-Gbps, (e, f) 39.5-Gbps

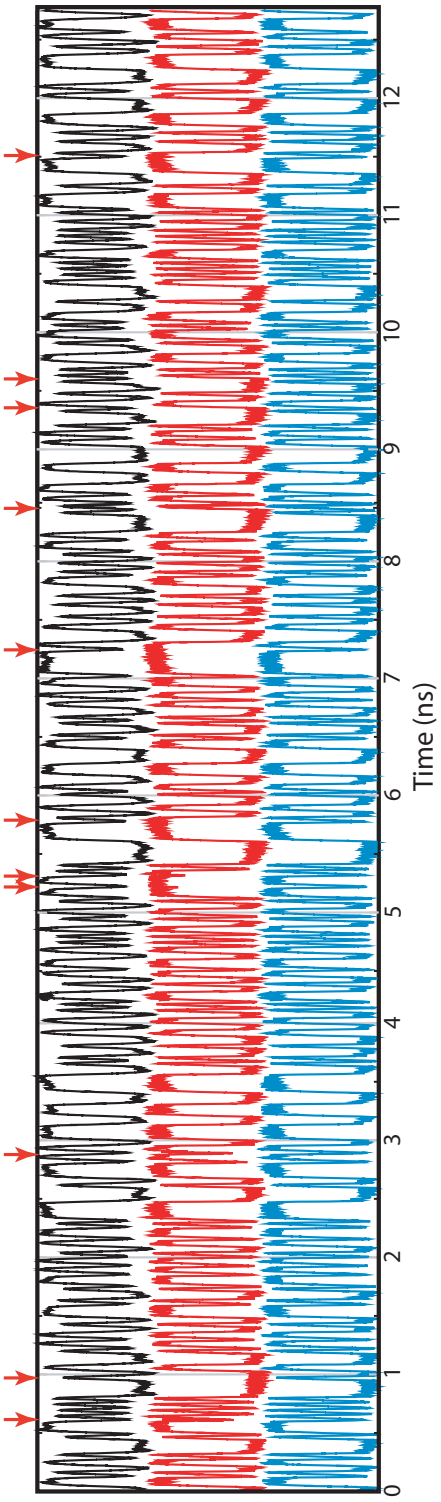
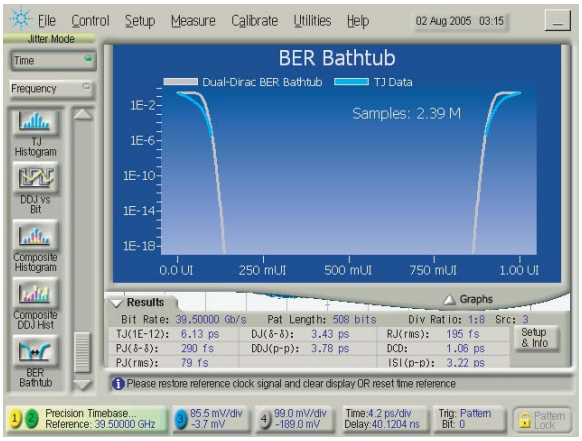
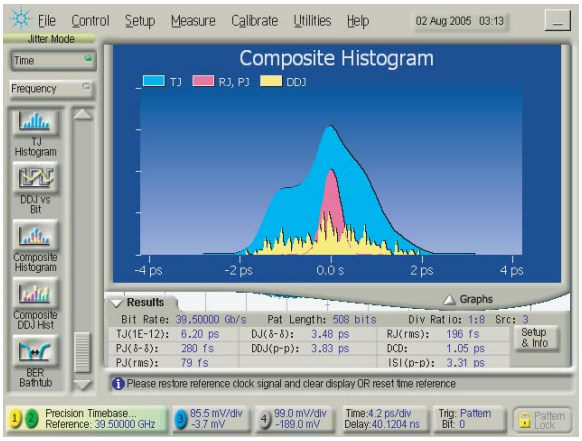


Figure 3.21: 508-bit sequence ($2^7 - 1$ PRBS on each board) for an ideal (top), unequalized (middle) and equalized (bottom) output. Errors indicated by arrows above bit sequence.



(a)



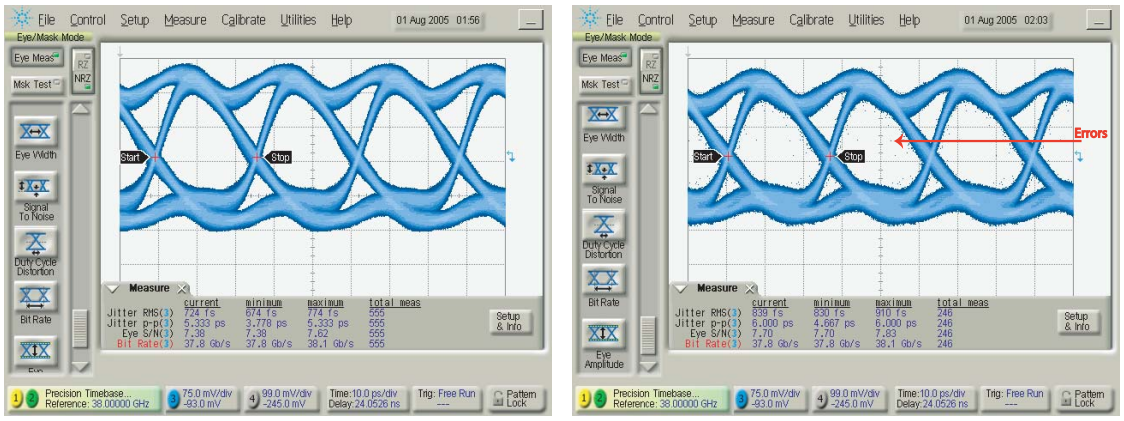
(b)

Figure 3.22: Jitter measurements for 508-bit sequence at 39.5 Gbps (a) bathtub curve and (b) jitter histogram

3.5.3 Measurement Limitation

The short comings of the measurement setup in Fig. 3.18 is the lack of information while adapting the tap weight. Unlike linear equalizers where adjusting the tap weight shows gradual improvement in the output eye diagram, a nonlinear equalizer almost always shows a clean output eye due to the decision circuit. Adaptation of the tap weight for the DFE is completed by capturing the bit pattern (508 for $2^7 - 1$, and 4092 for $2^{10} - 1$) with the oscilloscope and adjusting the tap weight until the output sequence is equal to the input bit sequence. Given that the verification process is completed by hand, the adaptation is cumbersome for long patterns. For long patterns, adaptation is first performed for shorter sequences and then with the

same tap weight, the PRBS order is increased. An example of this is presented in the eye diagram in Fig. 3.23(a), which shows an error free 38 Gbps equalized eye with a $2^{10} - 1$ PRBS sequence on the generator boards. When the PRBS generators are changed to a $2^{23} - 1$ bit sequence (Fig. 3.23(b)), errors in the output eye can be seen after 246 measurements. This indicates that the equalizer tap weight has not been optimized. Adjusting the equalization tap weight while manually verifying the bit sequence is not feasible since the erroneous pattern has a length of over 33 million bits. Moreover, due to the tuning sensitivity of the DC power supplies, the α control voltage can only be tuned coarsely in 10 mV differential steps. This further makes it cumbersome to reach the optimized tap weight and thus increasingly difficult to equalize the data through dispersive channels where significant ISI is found in the precursor and in the post cursor beyond 1 UI.



(a) (b)

Figure 3.23: Single-ended equalized output at 38 Gbps switching between higher order PRBS patterns (a) 2^{10}-1 (b) 2^{23}-1 with error

3.6 Summary

In this chapter, the characterization of the test chips was described. A series of small signal and large signal tests were performed to verify the functionality of the circuit. The analog front end is measured to show the linear characteristics of the full DFE. Equalization was performed through a PMD emulated channel at 5 and 6 Gbps, a 20-ft SMA cable at 10 Gbps and a 9-ft SMA cable at 40 Gbps. A BER of less than 10^{-12} for 5, 6 and 10 Gbps was verified. Error free operation at 40 Gbps with a

508-bit sequence was also completed. The key measured results are summarized in Table 3.1.

Table 3.1: Summary of measured results

Technology	Jazz Semiconductors' SBC18HX 0.18μm SiGe BiCMOS
Supply Voltage	3.3V
Power Dissipation	760mW
Broadband front end	95mW
Slicer	160mW
Decision Selective Feedback	225mW
Output Driver	95mW
Clock Path	185mW
S-parameter Measure	
S_{11} @ 40 GHz	-11 dB
S_{22} @ 40 GHz	-12 dB
S_{33} @ 40 GHz	-18 dB
S_{43} 3dB bandwidth	60 GHz+
Breakout 3dB bandwidth	45 GHz
P_{1dB} @ 20 GHz	-7.5 dBm
Eye Characteristics	6-Gbps
Peak-to-peak jitter	5.56 ps
SNR	13.91
Rise (Fall) time	18.9 (18.9) ps
Voltage Swing	2x321 mV
BER	$<10^{-12}$
Eye Characteristics	10-Gbps
Peak-to-peak jitter	10.22 ps
SNR	13.13
Rise (Fall) time	18.7 (17.8) ps
Voltage Swing	2x289 mV
BER	$<10^{-12}$
Eye Characteristics	40-Gbps
Peak-to-peak jitter	5.11 ps
SNR	9.1
Rise (Fall) time	13.67 (6) ps
Voltage Swing	2x324 mV

4 Conclusion and Future Work

The design of a 1-tap 40-Gbps decision feedback equalizer has been investigated for PMD compensation of single-mode fibre. In order to meet the high speed requirements, a look-ahead architecture is selected to decrease the propagation delay within the feedback path, while maintaining full functionality. Slight modifications to the architecture were made to ease the requirements on the clock distribution and reduce the overall power consumption of the DFE. A broadband front end provides a low noise, linear input stage with a bandwidth of 45 GHz. The differential tap weight was able to compensate for 225 mV of ISI using the threshold adjustment circuit. A propagation delay of 22ps from simulations is found through the critical path when interconnect parasitics are included. From measurements the DFE is shown to equalize a PMD emulating channel at 5 and 6 Gbps as well as a 20-ft SMA cable at 10 Gbps using a bit error checker. At 40 Gbps, the DFE compensated for a 9-ft SMA cable and the functional verification was conducted by hand. All the inputs/outputs of the DFE are suitable for high speed operation since they have a broadband matching of better than -10dB up to 40 GHz. The test chip occupies an area of 1.5 mm^2 and operates from a 3.3 V power supply and draws 230 mA of current.

To the author's knowledge, this is the first fully functional 40-Gbps DFE in any technology. It has been shown that using current commercially available technologies, equalizers at 40-Gbps are feasible [HV04] and previous assumptions on technology limitations are no longer valid. This work sets the stage for larger equalizer systems suitable for 40-Gbps fibre systems. With proper high speed design fully functional equalizers can be created.

Future work can involve the integration of an FFE with this DFE to create a complete PMD compensation system. As well, implementation of an AGC with a high dynamic range, bandwidth and sensitivity at 40 Gbps is still required. Moreover system level issues with the equalizer still exist. An adaptive algorithm for setting the tap weights has been accomplished at 10 Gbps and must be investigated for adoption at 40 Gbps. As well, low power clock recovery for the look-ahead architecture poses significant issues. The full implementation of a multiple tap FFE-DFE equalizer with

clock recovery and adaptive algorithms is a staggeringly vast task and area of research yet to be fully explored.

This work is a first step at solving current impairments of fibre optical systems. It is only a matter of time before OC-768 systems will be in place to meet the growing bandwidth needs.

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