A 30-GS/sec Track and Hold Amplifier in 0.13-μm CMOS Technology

Shahriar Shahramian, Sorin P. Voinigescu and Anthony Chan Carusone
University of Toronto, Toronto, Ontario, Canada, Email: sshahram@eecg.utoronto.ca

***Abstract*— A 30-GS/sec CMOS track and hold amplifier (THA) is designed and fabricated in a 0.13-μm technology. The chip operates from a 1.8-V supply and consumes 270 mW. The THA employs a low noise TIA input stage and a switched source follower (SSF) track and hold block. The SSF topology overcomes the shortcomings of switched series transistors by eliminating the use of a series switch all together. The measured single-ended S-parameters show an input and output return loss of better than -10 dB up to 35 GHz and 7 GHz of bandwidth when the circuit is operated in track mode. The measured total harmonic distortion of the THA is better than -29 dB.**

I. Introduction

This paper presents the design methodology and measurement results of a 30-GS/sec track and hold amplifier in CMOS. Decision feedback and feed forward equalizers have been demonstrated up to 40 Gb/s [1], [2]. However, if high-speed analog to digital converters (ADCs) can be realized, digital equalization is more robust, scalable and offers more flexibility. The design of a track and hold amplifier (THA) is a prerequisite to implementing high speed ADCs. An ADC design which omits the use of a THA has limited SNDR due to intolerable clock jitter [3].

With CMOS technologies scaling to nanometer dimensions and cutoff (f_T) and oscillation (f_{MAX}) frequencies of production CMOS technologies exceeding 200 GHz, MOSFETs can now be considered as serious contenders for implementing DSP-based equalizers above 10 Gb/s. All previously-reported THAs operating above 10 GHz have employed bipolar devices in the switched emitter follower topology, first proposed in [4]. The fastest THA reported to date is a switched-emitter follower, 40-GS/sec THA implemented in SiGe HBT technology and consuming 540 mW from a 3.6-V supply [5]. The fastest CMOS THA uses a switched series transistor topology in a 90-nm technology for a maximum clock frequency of 4 GHz while consuming 12.6 mW from a 0.9-V supply [6]. The switched series transistor architecture is inherently slow due to the large series resistance of the switch [6]. This work makes use of a switched source follower (SSF) to achieve a 30-GS/sec clock rate. By systematically biasing transistors in the signal and clock paths for maximum speed, the sampling frequency and bandwidth are increased by an order of magnitude compared with previously reported SSF THAs [7], [8].

Unlike all other CMOS THAs, this circuit employs a transimpedance amplifier (TIA) input to maximize bandwidth and minimize noise. The speed and performance of this CMOS THA are comparable to those of the fastest reported SiGe HBT and InP THAs [5], [9], [10] but are obtained with half the supply voltage and thus lower power due to the lower CMOS power supply voltage requirements.

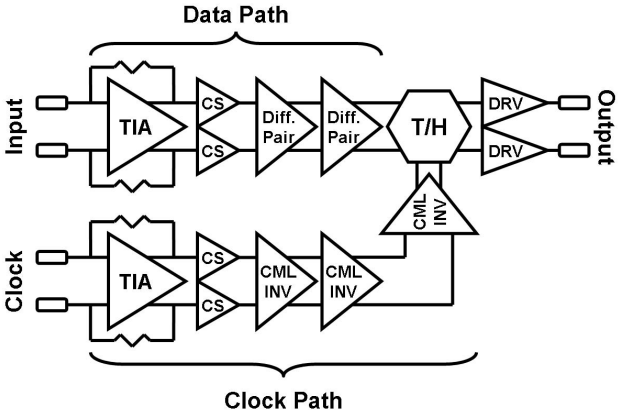

Fig. 1. Simplified block diagram of the fabricated THA.

II. Track and Hold Amplifier Design

Fig. 1 shows the block diagram of the track and hold amplifier. At the front-end is a TIA followed by a pair of common source (CS) amplifiers. The CS blocks drive two consecutive differential pair stages which in turn drive the track and hold (T/H) block differentially. The output drivers are single-ended common source amplifiers with 50Ω resistors. The data path of the THA is designed for maximum dynamic

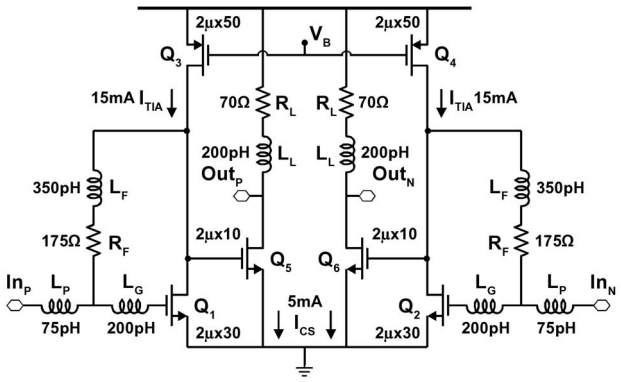

Fig. 2. Schematic of the TIA and CS stages. All MOSFETs have a drawn gate length of 0.13μm.

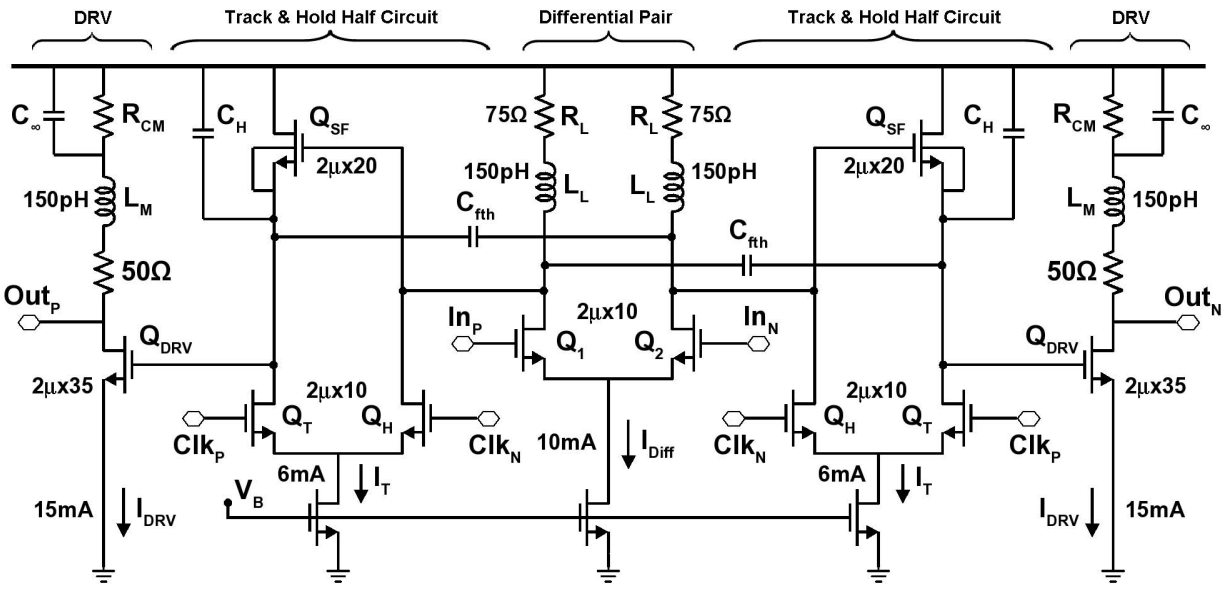

Fig. 3. Circuit diagram of the differential pair, T/H and output driver blocks. All MOSFETs have a drawn gate length of 0.13μm.

range. This is realized by choosing a low noise broadband input stage and biasing the transistors in the data path at 0.25 mA/μm for a good compromise between bandwidth, low-noise and high linearity.

A clock distribution network provides the differential clock signal to the T/H block. It consists of the same TIA-CS front-end as the data path, followed by three CML inverters. These stages operate in digital mode and are biased at 0.15 mA/μm for maximum switching speed. The circuit is powered from a 1.8-V supply and consumes 270 mW. The T/H block and the clock distribution network consume 12 mA and 70 mA respectively, while the remaining 68 mA of current is drawn by the input and output blocks.

A. Transimpedance Amplifier (TIA)

Instead of using 50Ω-terminated differential pairs, this design employs a low noise TIA input stage (Fig. 2). A TIA provides simultaneous noise and signal matching without the need for 50Ω matching resistors. Noise matching is achieved by sizing the input transistors (Q_{1-2}) to produce an optimum source impedance of 50Ω [11]. The input impedance is set by the feedback resistor R_F. Active PMOS loads (Q_{3-4}) are used to increase the open loop gain and maximize the linearity of the TIA. At DC, transistors Q_1 and Q_2 are diode connected and thus the output of the TIA biases the transistors Q_{5-6} [12]. The input-referred noise power spectral density of the cascade of the TIA and the differential pair stages obtained from simulation and integrated up to 30 GHz is 0.5 mV_{rms}.

B. Track and Hold Stage

Fig. 3 shows the schematic diagram of the T/H amplifier with a differential pair input and output driver. In track mode, Clk_P is high, Q_{SF} acts as a source follower and the output follows the input signal. In hold mode, Clk_N is high and the tail current I_T flows through the loads of the differential pair, R_L. The value of R_L is chosen such that the voltage drop $I_T R_L$ turns off transistor Q_{SF} and provides good isolation between the input and the output. The power supply voltage required by this design is dictated by $I_{Diff}R_L + V_{GS-QSF} + V_{GS-QDRV}$.

Taking advantage of the triple well option in this process, the bulk and source of Q_{SF} are shorted together to minimize V_{GS-QSF} and allow for a 600-mV_{P-P} signal swing at the output of the source follower. Even though a 1.8-V supply is required, the voltage drop across individual transistors does not exceed 1.2 V. The hold capacitance, $C_H = 250fF$, includes the parasitic capacitances at that node and a 50fF MIM capacitor. The value of C_{fth} is chosen to match C_{GS-QSF} and to cancel hold mode signal feedthrough.

C. Clock Distribution Network

The clock path converts a single-ended 30-GHz clock input to a differential signal with 750mV_{P-P} swing per side at the two switching pairs (Q_T and Q_H) in the T/H block. The blocks in the clock path operate at 30 GHz, the highest operating frequency of this circuit. It consists of a TIA stage (identical to Fig. 2) followed by three CML inverters. The schematic of the final three CML inverting stages is shown in Fig. 4. In order to ensure that every stage is fully switched, the gain of the inverters in the clock path is designed to exceed $\sqrt{2}$.

III. Fabrication and Testing

The chip was fabricated in a 0.13μm CMOS technology. The chip area is 1 mm^2 and the die photo is shown in Fig. 5. All measurements were conducted on-wafer with single-ended input and clock signal.

The simulated and measured S-parameters are shown in Fig. 7. The input and output return loss are better than -10 dB

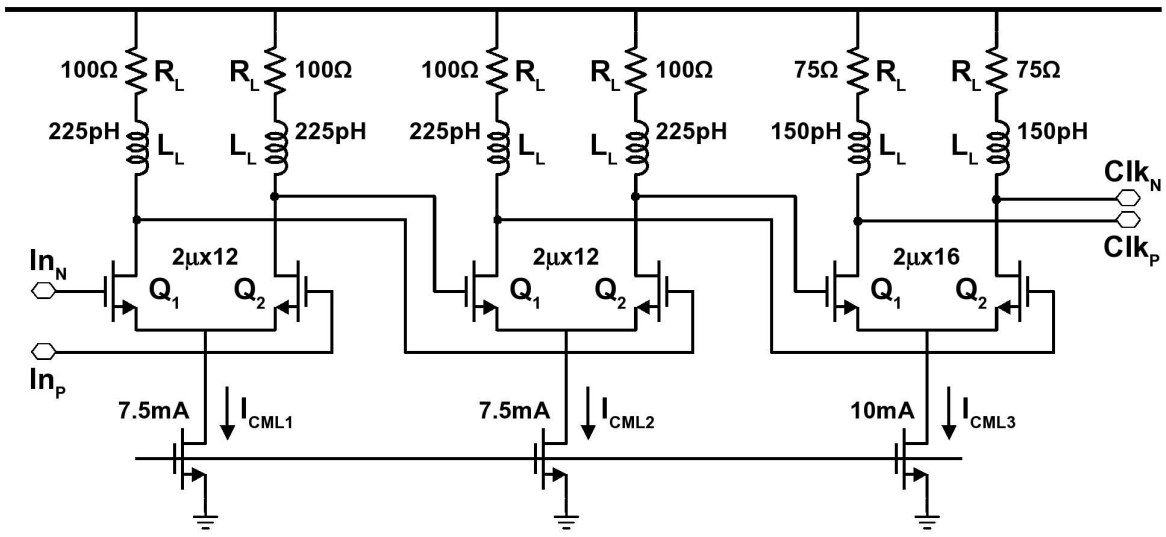

Fig. 4. Circuit diagram of the final three CML inverting stages of the clock path. All MOSFETs have a drawn gate length of 0.13μm.

up to 35 GHz. S_{21} has a bandwidth of 7 GHz when the circuit is operated in track mode. Since the front end of the data and clock paths are identical, the input return loss of the data path is also representative of the clock input return loss which is less than -15 dB from 22 GHz to 32 GHz.

Fig. 6 illustrates the two single ended outputs for a -12 dBm, 5-GHz input signal sampled at 30 GHz. Signal droop rate was measured at low clock frequencies to be less than 10 mV/ns. For a 30-GHz sampling frequency, this translates to a droop of only 0.2 mV per held value.

The input and output compression points of the circuit were measured from 1 GHz to 14 GHz in 1-GHz steps and are illustrated in Fig. 8. Fig. 9 shows the measured IIP3 and OIP3 as a function of frequency. The OIP3 plot indicates a circuit bandwidth of 7 GHz, in close agrement with the S_{21} measurement. Simulations show that the hold node is the bandwidth-limiting node of this circuit. The measured SFDR and THD are illustrated in Fig. 10. SFDR is calculated from the measured spectra and simulated noise floor integrated over a 30-GHz bandwidth, (evaluated to be -53 dBm). The THA has an SFDR of 40 dB at 1 GHz with 7 GHz of bandwidth.

IV. Conclusions

A 30-GS/sec CMOS THA was designed and fabricated in a 0.13-μm CMOS process. Following a systematic design procedure, and combining a low noise front-end with signal feedthrough cancelation and power supply voltage reduction techniques, has yielded the highest sampling frequency THA in CMOS. With a THD of better than -29 dB and 7 GHz of bandwidth, this THA is a potential contender for the front end of a 30 GS/sec flash ADC. Such an ADC can be used in over-sampling DSP based receivers for 10 Gbps applications.

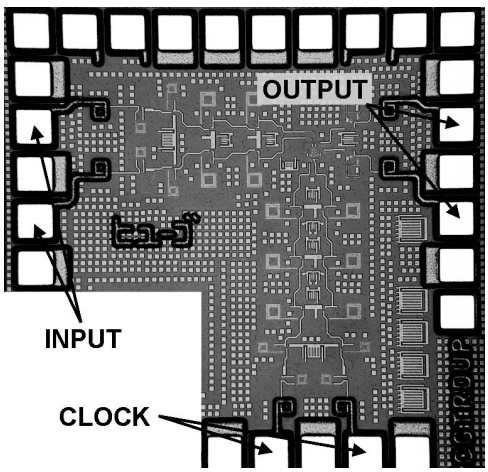

Fig. 5. Die photo of the fabricated THA

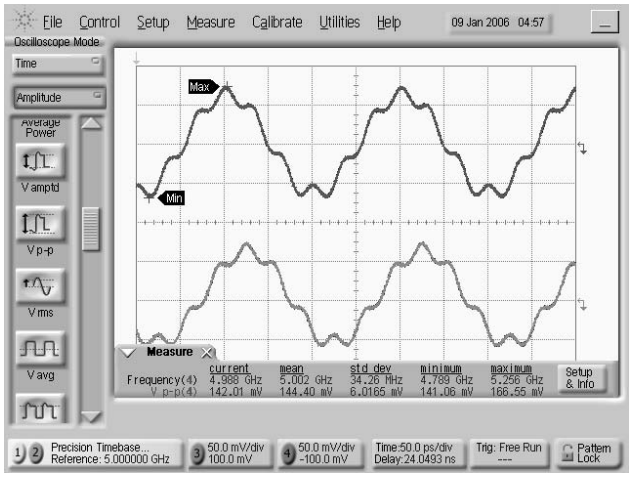

Fig. 6. Single ended outputs of a 5-GHz sinusoid sampled at 30 GHz.

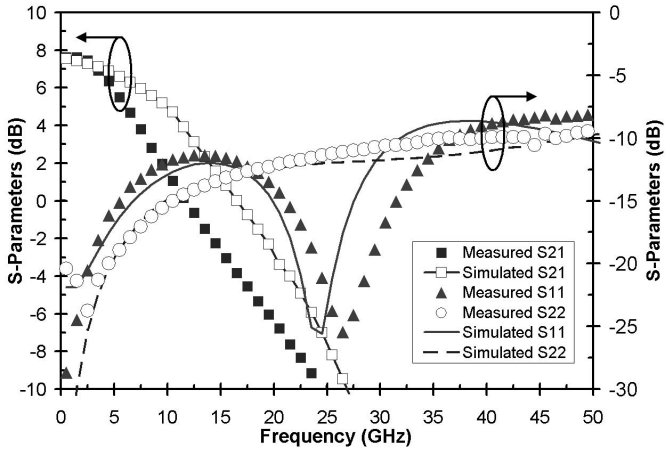

Fig. 7. Simulated and measured single-ended THA input return loss (S_{11}), output return loss (S_{22}) and transmission (S_{21}).

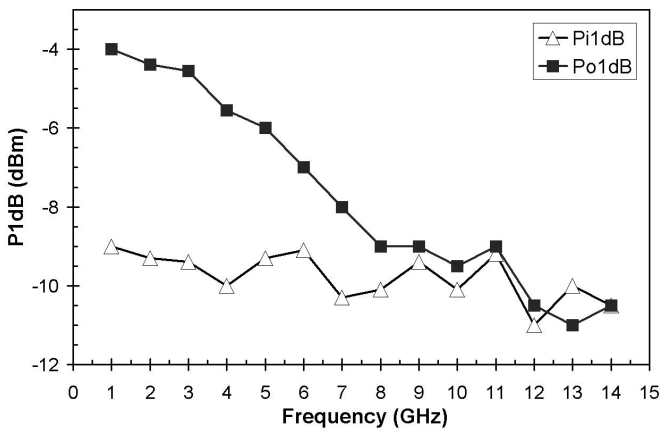

Fig. 8. Measured $\mathrm{Pi_{1dB}}$ and $\mathrm{Po_{1dB}}$ versus input frequency with 30-GHz clock frequency.

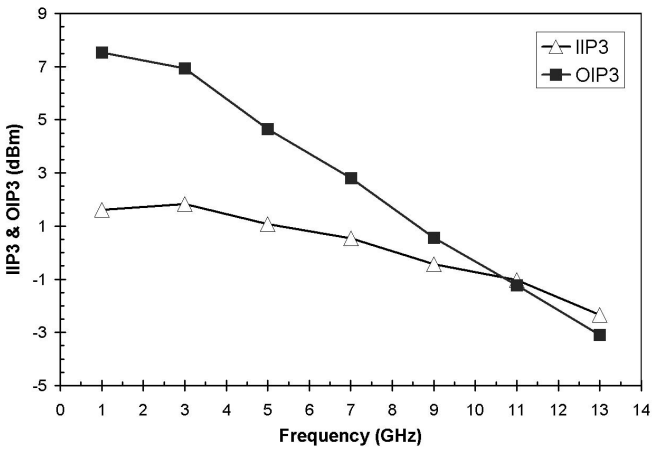

Fig. 9. Measured IIP3 and OIP3 versus input frequency with 30-GHz clock frequency.

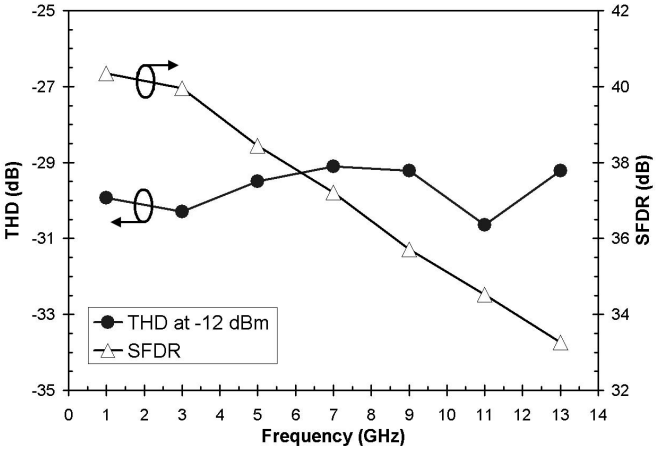

Fig. 10. Measured SFDR and THD versus frequency with 30-GHz clock frequency. The measured THD is shown for signals with -12 dBm input power.

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