A 2.3-4GHz Injection-Locked Clock Multiplier with 55.7% Lock Range and 10-ns Power-On

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***Abstract*—A frequency agile multiplying injection-locked oscillator (MILO) suitable for fast power cycling was designed in 65-nm GP CMOS. Edge detectors and multiple injection sites extend the lock range of the x4 multiplier to 36.3% of its free-running frequency. Lock range is further extended to 55.7% (2.3-4 GHz) by using 2 MILOs with adjacent lock ranges. Monitoring circuits identify the correct MILO and power-off the other MILO within 10 reference clock cycles.**

I. Introduction

Many wireline links require peak bandwidth operation for a small fraction of the time. Significant power savings have thus been realized by varying the interface baud rate as bandwidth requirements change, or powering down the link during idle periods [1], [2]. Greater link flexibility and further power savings can be achieved by combining both techniques in applications such as the source-synchronous memory link shown in Fig. 1. Combining these techniques, however, presents the significant challenge of designing clock multiplier that is both fast power cycling and frequency agile.

Multiplying injection locked oscillators (MILOs) can be powered on quickly but have narrow lock ranges, typically ≤ 5% [3] of the free-running frequency. PLLs [4], or MDLLs [5] can be tuned to accommodate a wide range of input frequencies, but their slow settling time makes them unsuitable for fast power-on architectures. While it is sometimes possible to adapt these loops for fast power-on applications by initializing their control voltages [1], this requires constant link speed between consecutive power-on cycles, limiting frequency agility. This paper presents the first clock generator that is both frequency-agile and has fast power-on. It has the ability to power-up in less than 10 cycles of the reference clock and to switch between operating frequencies on successive power-up cycles with no tuning of ILO operating frequency. This concept is illustrated by the waveforms in Fig. 1.

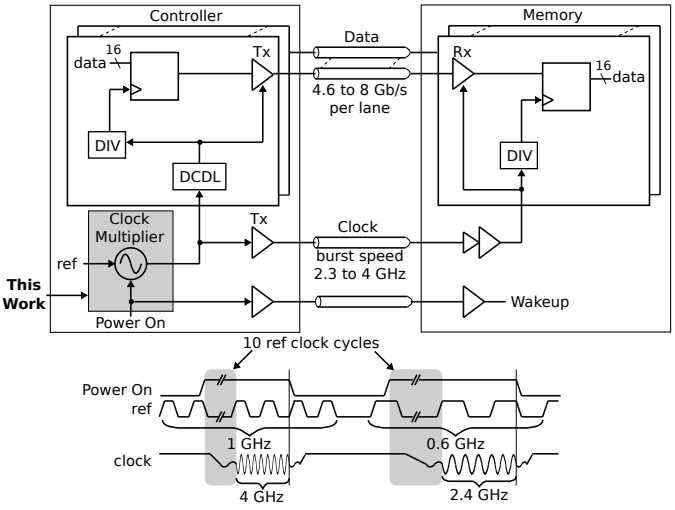


Fig. 1. A frequency agile clock multiplier that is suitable for fast power cycling can achieve link flexibility and power savings.

The proposed MILO, presented in section II, uses edge detectors and multiple injection points to achieve a wide lock range. The frequency agility is then increased further through the addition of a second MILO with an adjacent lock range. Although the addition of this MILO presents challenges to the fast power cycling of the multiplier, these challenges are addressed by the power-down circuitry detailed in section III. Measurement results are presented in section IV.

II. Wide Lock Range MILO Design

The core of the proposed MILO is shown in Fig. 2. It incorporates a ring oscillator structure made of differential CML delay stages, each having a secondary input differential pair for clock injection and an enable (EN) switch for fast power-on. The input clock passes through a delay line matched to the ring oscillator's delays. The resulting clock signals are the injected into each stage of ILO1. This technique was implemented in [2] to achieve a lock range of approximately 200 MHz, or 7.1% of the 2.8 GHz nominal frequency.

To increase the lock range further, the input clock passes through two edge detectors, Edge1 and Edge2, prior to injection. The pulse widths created by these detectors are fixed to multiples of the ILO's free-running frequency, f_0, and are respectively set to $\frac{1}{f_0}$ and $\frac{1}{2f_0}$ so that the signal at the output of Edge2 closely resembles a 50% duty-cycle clock at $4f_{in}$, as illustrated in Fig. 3(a). In order to ensure that these pulse widths are well-matched to f_0, the delay elements used in the edge detectors are replicas of those used in ILO1 with the unused injection pair grounded. In addition, the XOR gate used in the edge detectors is replicated in ILO1 as a fifth delay stage. These edge detectors achieve a significant increase in injection authority, which increases the lock range to 36.3% of f_0.

One disadvantage of using edge detectors with fixed pulse widths to perform frequency multiplication is that this can introduce deterministic jitter (DJ) into the injected signal when it is far from f_0, as shown in Fig. 3(b). To mitigate this effect, ILO2, which is identical to ILO1, is added at the output of the MILO core. By injecting the output of each stage of ILO1 into the corresponding stage of ILO2, the jitter filtering properties

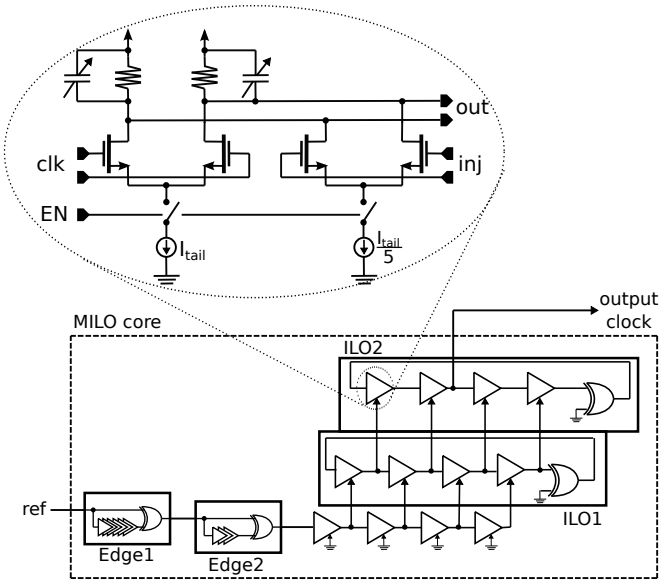


Fig. 2. Multiple injection points and edge detectors extend the lock range of the proposed MILO architecture.

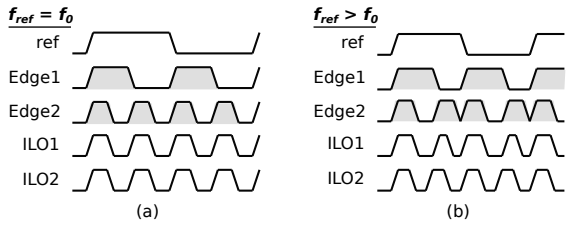


Fig. 3. Fixed edge detector pulse widths, highlighted in grey, introduce deterministic jitter when the injected signal frequency differs from f_0.

of ILO2 are exploited without limiting the overall lock range of the MILO.

III. Clock Multiplier Design

In the proposed clock multiplier two MILOs with separate but adjacent lock ranges are implemented as shown in Fig. 4. The adjacent lock ranges were implemented using different load capacitances in the delay elements used in each of the MILOs. These capacitances were implemented as varactors to allow adjustment of the lock range if necessary, however, no adjustment is performed during multiplier operation or between bursts.

Together, the two MILOs extend the lock range to 55.7% of f_0. In order to avoid a significant increase in power consumption, it is necessary to identify and power down the unlocked MILO. In order to maintain the desired fast power-on functionality, this identification and power-down must occur as quickly as possible.

In this design, selection is performed within 10 reference clock cycles of power-on by disabling either MILO if it fails to lock to the correct frequency multiple or, if both MILOs lock correctly, then selecting the one that is locked closest to its free-running frequency. This is achieved using the Edge Counter, Time to Digital Converter (TDC) and Frequency Offset Compare logic shown in Fig. 4. Since only one MILO

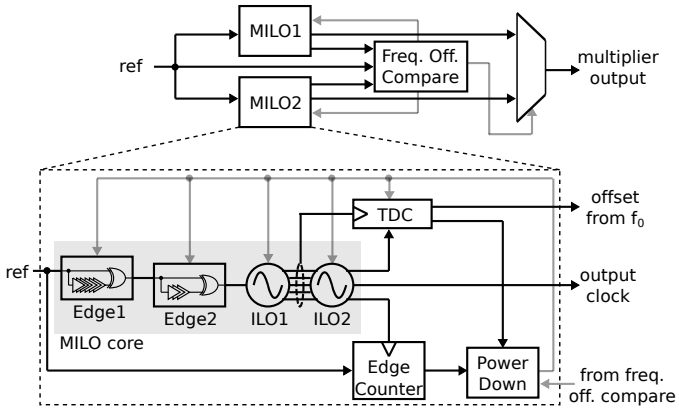


Fig. 4. The clock multiplier consists of 2 MILOs with logic used to deactivate the unused MILO within 10 ref clock cycles.

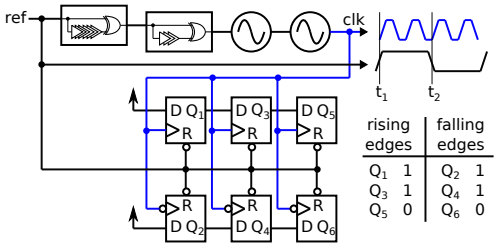


Fig. 5. Counting the number of rising and falling edges present in the output clock during one half-period of the reference enables quick identification of locking to an incorrect multiple of the reference frequency.

consumes power after selection is complete, additional MILOs could be used to achieve greater lock range without additional steady state power consumption.

A. Edge Counter

One significant challenge in the design of a frequency agile clock multiplier is the potential for false lock to an incorrect frequency multiple of the reference signal. Although designed to multiply the reference clock by a factor of 4, the multiplier may lock to other multiples (i.e. x3 or x6) if these should fall within the MILOs lock range. To check for this condition, the Edge Counter shown in Fig. 5 counts the number of rising and falling output clock edges present in one half-period of the reference clock.

If the multiplication factor is correct then there will be two rising and two falling edges present in each reference clock half-period, resulting in output bits Q_1 to Q_6 as shown in Fig. 5. Any change in these bits identifies an incorrect multiplication factor, resulting in immediate power-down of the corresponding MILO.

B. TDC Phase Analysis

The multiplier structure must also be able to identify and power down a MILO that is unlocked. This is accomplished using the TDC shown in Fig. 6, which is used to take a snapshot of the phase relationship between the clock output from ILO2 and its injected signals. The condition $Q_6 = \overline{Q_1}$ is only violated when the ILOs are not locked, in which case the TDC initiates a power-down of the unlocked MILO.

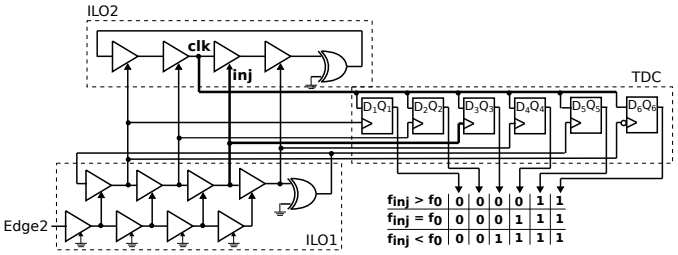


Fig. 6. A TDC takes its input from the two ILOs to determine if they are locked and, if so, how far they are operating from f_0.

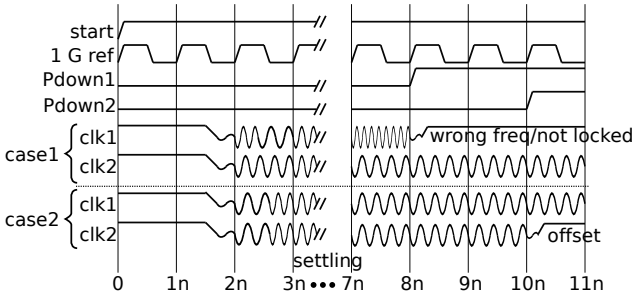


Fig. 7. Timing diagram shows behaviour of MILOs and their control logic during a startup sequence using a 1-GHz reference clock.

Furthermore, bits Q_2 to Q_5 can be used to indicate the amount of offset between the operating frequency of ILO2 and its free-running frequency. This information is used when the input frequency lies within the overlap of their lock ranges so that both MILOs are locked at $4f_{in}$. In this case bits Q_2 to Q_5 from each MILO are compared by the Frequency Offset Compare logic to determine which oscillator is operating closest to its free-running frequency. This MILO should be more tolerant to subsequent voltage and temperature variations and is therefore chosen as the clock output while the other MILO is powered down.

Operation of the multiplier and its power-down logic during the startup sequence is summarized by the timing diagram shown in Fig. 7. To allow for the MILOs to settle to their final frequencies, on-chip logic counts 8 cycles of the reference clock before enabling "Pdown1", which allows power-down decisions to be made by the Edge Counter or TDC. If no decision has been made then "Pdown2" is enabled 2 cycles later to allow power-down to be decided by the Frequency Offset Compare logic.

IV. Measurement Results

A prototype of the multiplier was fabricated in a 65-nm GP CMOS process and a die photo is shown in Fig. 8. Both MILOs, along with the frequency compare logic and 50 Ω driver occupy 0.149 mm^2 and consume (a) 0 mW while idle, (b) approximately 165 mW during a power-up cycle and (c) 96 mW during steady-state frequency multiplication.

A. Lock Range

Fig. 9 shows the measured lock range of the multiplier from 2.28 to 4.04 GHz, or 55.7% of the 3.16 GHz center frequency. This includes an overlap region of 320 MHz with

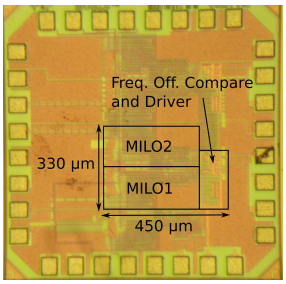


Fig. 8. Die photo of the multiplier in 65-nm GP CMOS.

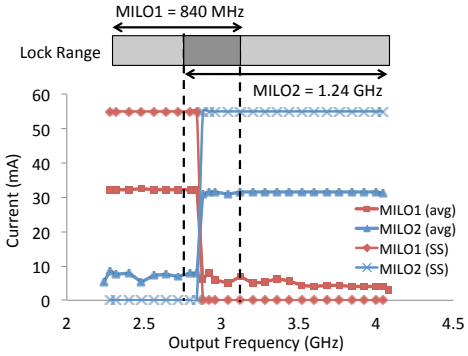


Fig. 9. Measured results show an overall lock range of 55.7% and that the Frequency Offset Compare logic switches between MILOs at an appropriate point. Average (avg) current consumed during 50-ns bursts with a 50% duty cycle shows significant reduction compared to steady-state (SS) values.

varactor control voltages at their nominal values. The plot of current drawn from separate MILO supplies in Fig. 9 shows the point at which the Frequency Offset Compare automatically switches from MILO1 to MILO2 as the reference frequency is increased. This transition occurs well within the overlap region although not quite in its center because of the relatively coarse resolution of the TDCs.

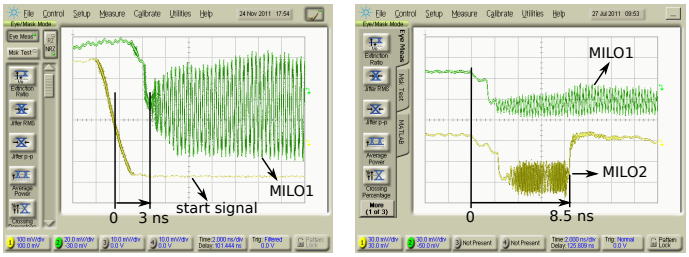
Although each MILO draws 55 mA from a 1.1 V supply during steady-state (SS) operation, the average (avg) current is reduced to 32.2 mA when the multiplier circuit is on 50% of the time for 50-ns bursts. Furthermore, this average continues to shrink as the percentage of active time decreases. This is in contrast to traditional clock synthesizers which must either be left on at all times [4] or sacrifice their frequency agility in order to achieve fast power-on [2].

B. Power-Up Transients

Fig. 10(a) illustrates the behavior of one MILO during a power-up cycle and verifies that startup occurs in approximately 3 ref clock cycles. When the start signal arrives, Fig. 10(b) shows how both MILOs are powered up and on-chip logic begins counting the reference clock cycles. After waiting 8 reference clock cycles for lock, the unlocked MILO2 is identified and powered down. After this brief period no power is drawn by MILO2.

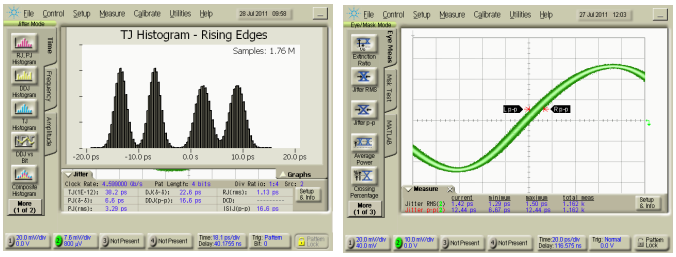
C. Jitter

The use of two cascaded ILOs provides a decrease in the DJ introduced by the edge detectors with fixed pulse



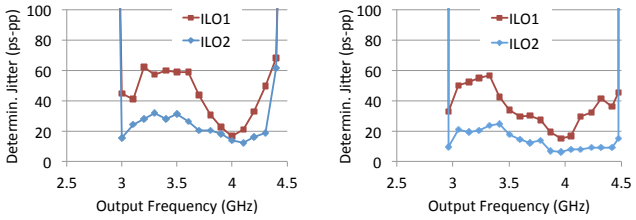
(a) (b)

Fig. 10. Measurements of the power-on sequence show (a) startup within 3 ns of the start signal and (b) the unlocked signal is identified and powered down in under 10 ref clock cycles.



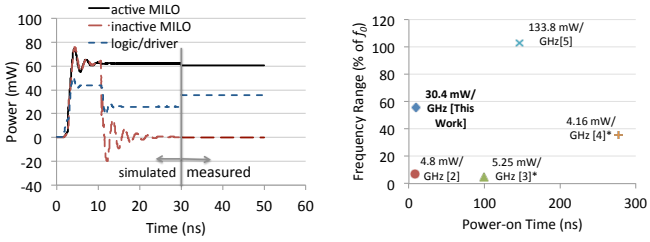
(a) (b)

Fig. 12. Total jitter (a) shows distinct peaks (DJ) caused by the low signal swing with Gaussian distributions due to the RJ. Isolating a clock edge from the DJ (b) shows measured RJ of 1.4 ps-rms.



(a) (b)

Fig. 11. The addition of ILO2 improves DJ performance (a) and increasing the swing of the output clock improves DJ (b), indicating that measured results are overly pessimistic due to poor output driver performance.



(a) (b)

Fig. 13. Simulated power consumption during power-up (a) shows good agreement with measured steady-state results. Comparison with previous work (b) puts compares power consumption to power-on time and frequency range.

widths. In Fig. 11(a) measurements show a drop in worst-case peak-to-peak DJ ranging from 2.5 to 30.5 ps over the lock range of one MILO. Unfortunately, attenuation caused by the package parasitics resulted in a small signal swing of only 50 mV_{pp} per side at the chip outputs. Since these parasitics attenuate the output frequency more than the low-frequency reference signal, this creates artificially large values of DJ. Fig. 11(b) verifies this by showing a reduction in DJ when power consumption, and therefore signal swing, of the output drivers is increased. Since driver power consumption could not be separated from the rest of the chip, this operating condition was not used for other measurements.

Measured results of the total jitter are shown in histogram form in Fig. 12(a) where the peaks due to the DJ can be seen as well as Gaussian distributions about each peak due to the RJ present. In Fig. 12(b) a clock edge has been isolated from the DJ by triggering the scope with the reference frequency at $\frac{f_0}{4}$. This shows measured RJ of 1.4 ps-rms, which remains relatively constant across the entire lock range of the multiplier.

D. Power Consumption

The power consumed by the multiplier varies during a power-up sequence. Since this variation occurs during a period of only 10 reference clock cycles, measurement of these variations is difficult. Instead simulation results of a power-up sequence are shown in Fig. 13(a) along with measured values of the steady-state power consumption showing 60.5 mW consumed by the active MILO, 0 mW consumed by the inactive MILO, and 35.5 mW consumed by the Frequency Offset Compare logic and the output driver.

A comparison with previous work in Fig. 13(b) highlights the improvement in power-on time and frequency agility achieved by this multiplier. Steady-state power consumption levels are reported for comparison but these do not capture any savings achieved through link power-down.

V. Conclusion

The presented clock multiplier uses two MILOs to achieve a frequency lock range of 55.7% of the 3.16 GHz centre frequency. The DJ introduced by the pulse injection scheme is mitigated by the addition of a second ILO. Transient tests of the power-on behaviour of the multiplier verify that the control logic is able to correctly identify the optimum output clock and power down the unused MILO within 10 reference clock cycles of the arrival of a start signal. The active MILO and its associated logic and output drivers consume a total of 96 mW during steady-state operation, which scales with the amount of time during which the link is active.

References

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