All-Digital Calibration Algorithms to Correct for Static Non-Linearities in ADCs

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***Abstract*—This paper presents all-digital calibration algorithms for correcting static non-linearities in an ADC. A bit-by-bit (BB) calibration is proposed as an alternative to the existing radix calibration. The proposed calibration algorithm is initially demonstrated using a non-uniform ADC model generated in Matlab. A hybrid radix/bit-by-bit calibration is also developed to reduce the computational complexity of BB calibration. The calibration algorithms are then applied to measurement data from two different ADCs: a 6-bit folding-flash; and a 10-bit dual-split capacitor (DSC)-DAC SAR ADC. In both ADC architectures, the BB and hybrid calibrations outperform radix calibration. The BB calibration improved the SNDR and SFDR of the folding-flash ADC from 29.5 dB to 31.9 dB and 33.3 dB to 43.6 dB, respectively. Likewise, after applying the hybrid calibration on the DSC-DAC SAR ADC, the SNDR and SFDR improved from 31.8 dB to 47 dB and 33.6 dB to 58.9 dB, respectively. The hybrid calibration achieves performance similar to that of BB calibration while demonstrating a significant reduction in computational complexity.**

I. Introduction

Static non-linearities in ADCs can be a significant performance impairment. They may be caused by device mismatches. For example, in a flash ADC, they arise due to the random offsets in the comparators and mismatches in the resistor ladder, whereas in a SAR ADC, they arise due to mismatches in the capacitive DAC. Fortunately, ADC non-linearities, if known, can be calibrated and corrected.

Calibration may be performed in either the analog or digital domains. Fig. 1(a), illustrates an analog calibration technique where the non-uniform quantization levels of an ADC are restored to uniformly-spaced levels using analog-mixed signal circuit adjustments or tuning. On the other hand, Fig. 1(b) illustrates a digital calibration technique where non-linearities are corrected by inverting the non-linearity of the ADC using, for example, a lookup table. With digital calibration, the quantization levels remain non-uniform during operation and may result in varying degrees of quantization error depending on the input distribution.

All-digital calibration techniques can be desirable because they do not require additional analog circuitry. Radix calibration is an example of digital calibration that has been used in pipelined ADCs [1] and in SAR ADCs [2]. Although effective for correcting radix errors, it can not correct other forms of static non-linearity. In this work, we propose a bit-by-bit (BB) calibration technique capable of linearizing any static non-linearity. A hybrid of radix and BB calibration is also proposed to reduce the computational complexity of BB calibration. The effectiveness of these calibration algorithms is then demonstrated on measured data from a flash ADC and a SAR ADC.

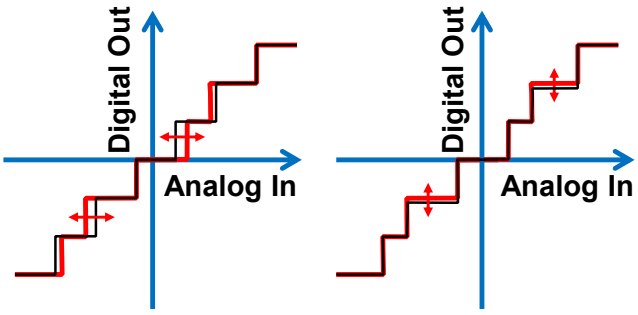


Fig. 1: Non-linearity calibration methods: (a) Analog calibration (b) Digital calibration

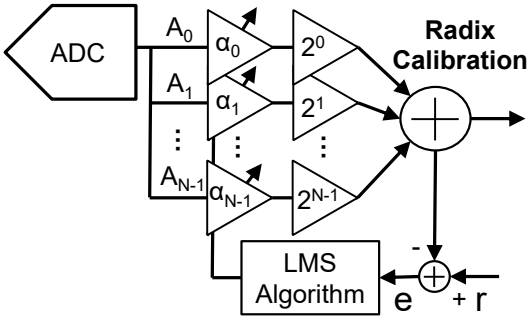


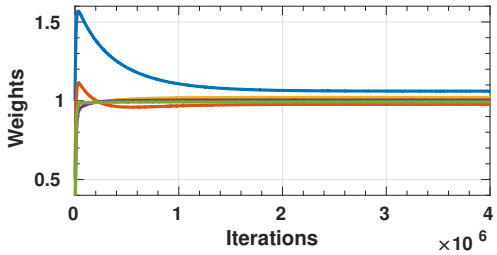
Fig. 2: Radix calibration [2]

II. All-Digital Calibration Algorithms

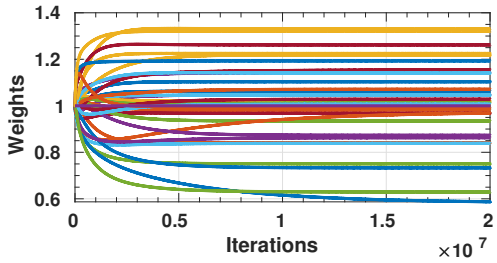
The basics of radix calibration are first described in the following subsection followed by a detailed discussion of the proposed BB calibration and the hybrid radix/bit-by-bit calibration technique.

A. Radix Calibration

Radix calibration as described in [2] is shown in Fig. 2. This foreground calibration algorithm alters the ideal radix-2 weighting by applying an adaptive scaling coefficient α_i to each binary output of the ADC. These α-coefficients



(a)



(b)

Fig. 3: Convergence of weights during the LMS adaptation: (a) Radix α-coefficients, (b) Bit-by-bit β-coefficients

are found using a least-mean squares (LMS) algorithm that minimizes the error between the ADC output and an ideal known reference. This reference, $r(k)$, may be a ramp signal, sinusoidal signal or any other signal with the characteristics necessary to quantify the non-linearities within the ADC. The error is,

$$e(k) = r(k) - \sum_{i=0}^{N-1} A_i 2^i \alpha_i(k) \tag{1}$$

where N is the resolution of the ADC, $A_i(k)$ are the binary outputs of the ADC and α_i are the adapted weighting coefficients. The α-coefficients are iteratively updated

$$\alpha_i(k+1) = \alpha_i(k) + \frac{\mu e(k) A_i(k)}{2^i} \tag{2}$$

where k is the current iteration and μ is the rate of convergence of the LMS adaptation algorithm.

To demonstrate the method, a 5-bit ADC with non-uniformly distributed quantization levels is generated in Matlab. The quantization levels are varied randomly around their ideal values with a Gaussian distribution having a mean of zero and standard deviation of 0.3 times a nominal LSB. Applying radix calibration on this ADC model, the α-coefficients are shown in Fig. 3(a) converging to values scattered around 1. The converged radix weights can then be stored and used continuously during the operation of the ADC. The performance of the non-uniform ADC generated in Matlab with no calibration, Fig. 5, has a SNDR of 29 dB and SFDR of 36.1 dB. After, radix calibration, the SNDR and SFDR improve marginally to 29.2 dB and 36.5 dB, respectively.

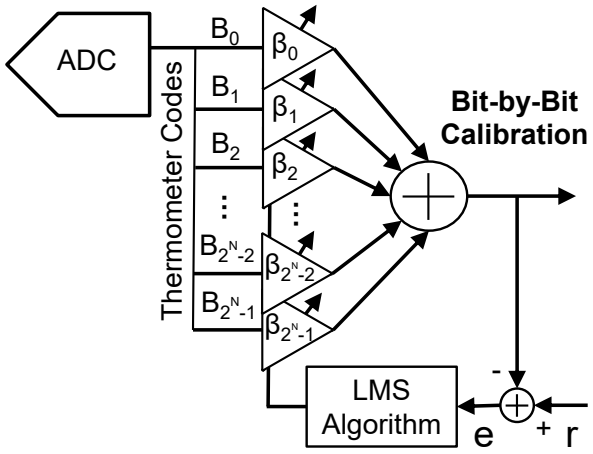


Fig. 4: Bit-by-bit Calibration

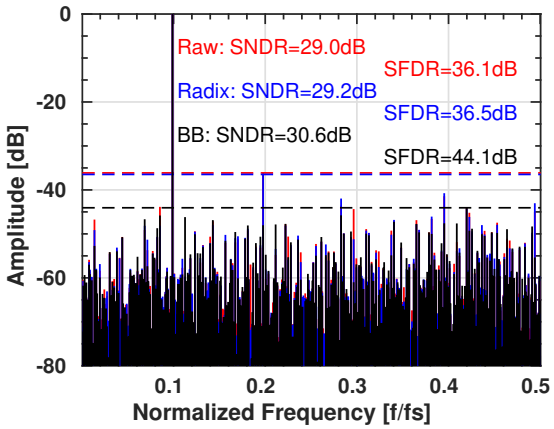


Fig. 5: FFT of 5-bit non-uniform Matlab ADC before and after calibration.

B. Bit-by-bit (BB) Calibration

In bit-by-bit calibration, instead of adapting N α-coefficients, one for each bit of the ADC, we adapt 2^N–1 β-coefficients, one for each thermometer-encoded digital signal, as shown in Fig. 4. Effectively, this adaptively populates a lookup table for each possible digital output code of the ADC. Like radix calibration, BB calibration uses the LMS algorithm to find the β-coefficients. Hence, given thermometer-coded outputs $B_i(k)$, the error is,

$$e(k) = r(k) - \sum_{i=0}^{2^N-1} B_i(k)\beta_i(k) \tag{3}$$

where N is the ADC resolution and β_i values are the adapted weighting coefficients. The β-coefficients are iteratively updated

$$\beta_i(k+1) = \beta_i(k) + \mu e(k) B_i(k) \tag{4}$$

Using the same 5-bit ADC model in Matlab, convergence of the β-coefficients using BB calibration is plotted in Fig. 3(b). The converged weights are used continuously during

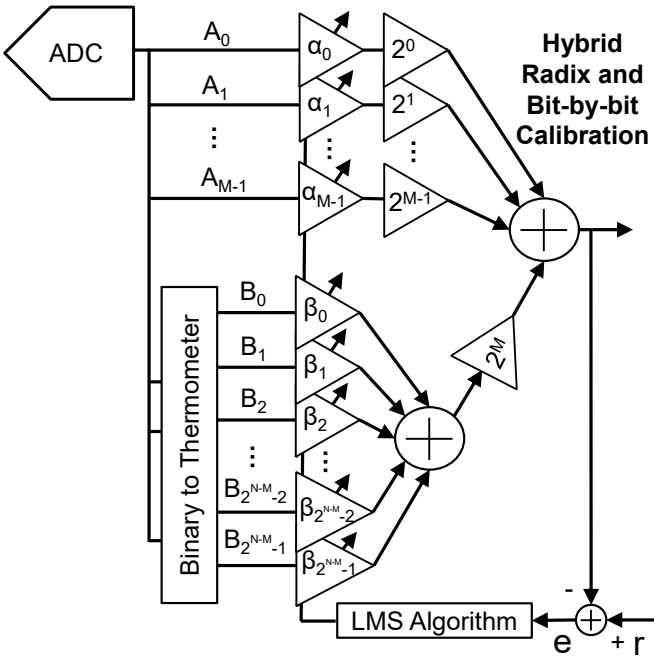


Fig. 6: Hybrid Radix/Bit-by-Bit Calibration

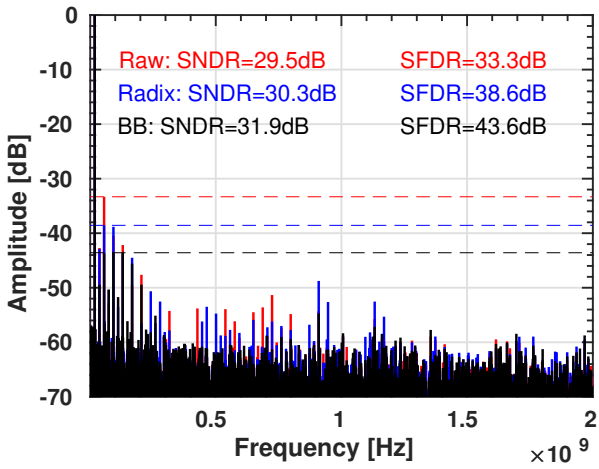


Fig. 7: FFT of 6 bit folding-flash ADC before and after calibration.

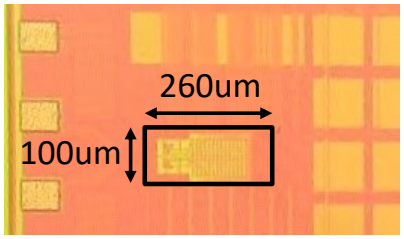


Fig. 8: Die photo of 10-Bit DSC-SAR ADC in 65 nm CMOS

operation to linearize the ADC. BB calibration provides more flexibility in inverting front-end static non-linearities, whereas radix calibration is a special case of BB calibration. Thus, BB calibration should always perform at least as good as radix calibration. In the unlikely case that radix calibration with appropriate coefficients provides the best possible non-linearity correction, then BB calibration would, indeed, converge to that exact same non-linear static transfer function and the two would perform exactly the same. As mentioned before, the Matlab ADC with no calibration, Fig. 5, has a SNDR of 29 dB and SFDR of 36.1 dB. BB calibration improves the SNDR to 30.6 dB while providing a considerable improvement in the SFDR to 44.1 dB.

C. Hybrid Radix and Bit-by-Bit Calibration

It is apparent in Fig. 3(b) that BB calibration requires more computation and coefficient storage than radix calibration. As the resolution of the ADC increases, the number of weights (β-coefficients), being 2^N-1, grows exponentially. This generally implies that the LMS adaptation loop requires more iterations for convergence.

We therefore also propose a hybrid of radix and BB calibration, shown in Fig. 6, that reduces the number of weights. For a N-bit ADC, the M least significant bits are used for the radix calibration and $N-M$ most significant bits are used for the BB calibration, where $M < N$. The number of calibration weights becomes $2^{N-M}+M-1$ providing a substantial reduction in both computational complexity, convergence time and memory while offering performance similar to BB calibration.

III. Measurement Results

The proposed calibration algorithms are first applied to a 6 bit folding-flash ADC and then a 10 bit DSC-DAC SAR ADC.

A. Folding-Flash ADC Architecture

With a flash architecture, random offset is a significant source of non-linearity to which the bit-by-bit method is well-suited. Other static non-linearities in flash ADCs can also arise from mismatch in reference generation (e.g. resistor ladder). Radix and BB calibration algorithms are applied to the measured data of the 6-bit ADC in [3] with an input frequency of 18.845 MHz and a sampling rate of 4 GHz. This ADC has a 1-bit folding stage to determine the sign bit, followed by a 5-bit flash ADC. The results are shown in Fig. 7. Without calibration, the SNDR and SFDR are 29.5 dB and 33.3 dB, respectively. With radix calibration, the SNDR and SFDR improves to 30.5 dB and 38.6 dB, respectively. Finally, after applying BB calibration, the SNDR and SFDR improve significantly to 31.9 dB and 43.6 dB, respectively.

B. Dual-Split Capacitor (DSC)-DAC SAR ADC Architecture

A 10-bit dual-split capacitor (DSC)-DAC SAR ADC was fabricated in 65 nm CMOS technology, shown in Fig. 8. The sampling switch and comparator are as described in [4] and [5], respectively. The DAC architecture is shown in Fig. 9. Split capacitors have been used [6] to reduce the area and capacitive load presented by the C-DACs. When multiple split capacitors are used, the sensitivity to parasitic capacitance increases; two are used in this design.

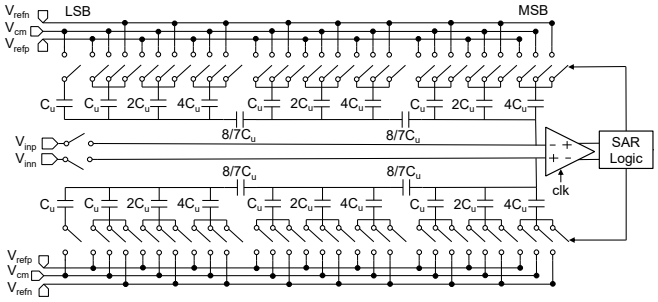


Fig. 9: Schematic of 10-Bit DSC-DAC SAR ADC

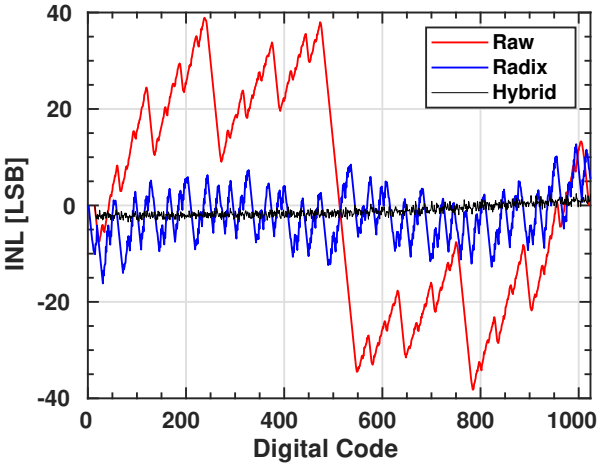


Fig. 10: INL of 10 bit DSC-SAR ADC before and after calibration.

Fig. 10 plots the ADC INL, generated using histogram method. Prior to any calibration, the maximum and the minimum values of the INL are +38.90 and –38.19 LSBs, with a standard deviation of 22.44 LSBs. Following the application of radix calibration, these values drop to +12.70, –16.17, and 5.09 LSBs, respectively. This significant improvement afforded by radix calibration is not surprising because mismatch and parasitic capacitance in binary weighted and/or split capacitors in the C-DAC result mainly in radix errors. Hybrid calibration is also applied with $M = 4$ which further improves the INL values to +2.92, –2.23, and 0.77 LSBs, respectively. Thus, hybrid calibration outperforms radix calibration significantly since it can further correct non-linearities that radix calibration can not. Similar trends are shown in Fig. 11, where the input frequency is 7.495 kHz and a sampling rate of 200 kHz. Before calibration, the SNDR and SFDR are 31.8 dB and 33.6 dB respectively. Once radix calibration is applied, the SNDR and SFDR improves to 40.4 dB and 47.4 dB, respectively. After applying hybrid calibration, the SNDR and SFDR drastically improve to 47.0 dB and 58.9 dB. Although radix calibration corrected for some of the spurs and harmonics generated by the ADC, hybrid calibration did better and could eliminate most visible spurs. Table I compares the hybrid calibration performance to radix and BB calibration on the DSC-DAC

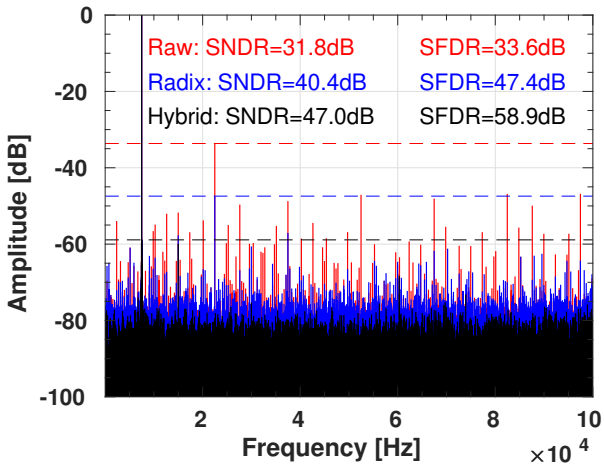


Fig. 11: FFT of 10 bit DSC-SAR ADC before and after calibration.

TABLE I: Comparison of the performance of digital non-linearity calibration methods on the 10 bit DSC-SAR ADC.

	SNDR (dB)	SFDR (dB)	# of Weights
Radix	40.4	47.4	10
Hybrid ($M = 4$)	47.0	58.9	67
Bit-by-bit	47.6	59.1	1023

SAR ADC. The bit-by-bit calibration is capable of improving the SNDR and SFDR to 47.6 dB and 59.1 dB, respectively which is a marginal improvement compared with the hybrid method, although 15 times more weights are required.

IV. Conclusion

In this paper, two new all-digital non-linearity calibration algorithms are proposed for ADCs. The BB and hybrid calibration methods are introduced and compared with a pre-existing all-digital non-linearity calibration method, radix calibration, using a Matlab model as well as measurement data from two different ADC architectures. Significant improvements in the INL, SNDR and SFDR were observed when applying the BB and hybrid calibrations. The hybrid calibration method significantly decreases the computational complexity, convergence time, and storage requirements of the BB calibration method while maintaining similar levels of performance.

Acknowledgment

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