ELECTRONIC EQUALIZATION OF POLARIZATION-MODE DISPERSION IN 40-GB/S OPTICAL SYSTEMS

by

Jonathan Sewter

A thesis submitted in conformity with the requirements
for the degree of Master of Applied Science
Graduate Department of Electrical and Computer Engineering
University of Toronto

ELECTRONIC EQUALIZATION OF POLARIZATION-MODE DISPERSION IN 40-GB/S OPTICAL SYSTEMS

Jonathan Sewter

2005

Degree of Master of Applied Science
Graduate Department of Electrical and Computer Engineering
University of Toronto

Abstract

Electronic equalization of polarization-mode dispersion (PMD) effects in 40-Gb/s optical systems is investigated through system-level analysis and integrated circuit (IC) design. A system-level analysis of first-order PMD effects is used to compare different electronic equalizer architectures as potential PMD compensators. It is found that a decision feedback equalizer (DFE) consisting of a 3-tap feedforward equalizer (FFE) and a 1-tap feedback equalizer (FBE) is able to increase the useful length of a PMD-limited optical system by more than eight times. Two modifications to the travelling-wave filter (TWF) topology are introduced which enable the decoupling of equalizer tap spacing and bandwidth. These new TWF topologies are used in the implementation of two 3-tap 40-Gb/s FFEs. The equalizer ICs are implemented in the TSMC 90-nm and 0.18-μm CMOS processes, and represent the first implementations of 40-Gb/s equalizers in CMOS.

Acknowledgements

I would like to sincerely thank my friend, Dr. Tony Chan Carusone, for his insight, guidance and support. It is an honour to have called him my colleague and supervisor these past two years.

I would like to thank Dr. Sorin Voinigescu for his expert advice at many stages along the course of this project.

Thank you to Dr. Voinigescu, Dr. David Johns and Dr. Amr Helmy for serving on my thesis examination committee. Their recommendations have benefited this work significantly.

Thank you to all of my fellow electronics graduate students. I am especially grateful to Adesh Garg, for his friendship and many contributions over the course of numerous discussions; to Michael Gordon for his assistance with circuit measurements; and to Tod Dickson, for access to his expert knowledge on many occasions.

I gratefully acknowledge the support provided by the Natural Sciences and Engineering Research Council of Canada (NSERC), Gennum Corporation, Micronet, the Canadian Microelectronics Corporation (CMC) and the Taiwan Semiconductor Manufacturing Company (TSMC).

As always, thank you to my family and friends for their support and encouragement.

To my wife, Sarah, I owe everything else.

Contents

List of Tables

List of Figures

List of Abbreviations

ADC	Analog to digital converter
BER	Bit-error rate
BiCMOS	Bipolar complementary metal-oxide semiconductor
CD	Chromatic dispersion
CML	Current-mode logic
CMOS	Complementary metal-oxide semiconductor
CP	Cumulative probability
CS	Common source
DA	Distributed amplifier
DFE	Decision-feedback equalizer
DGD	Differential group delay
DSP	Digital signal processing
EAM	Electro-absorption modulator
FBE	Feedback equalizer
FEC	Forward error correction
FFE	Feedforward equalizer
FIR	Finite impulse response
FSE	Fractionally-spaced equalizer
HEMT	High electron mobility transistor
IC	Integrated circuit
IIR	Infinite impulse response
ISI	Inter-symbol interference

LADFE	Look-ahead DFE
LMS	Least mean square
MiM	Metal-insulator-metal
MLSD	Maximum-likelihood sequence detection
MMF	Multi-mode fiber
NFET	n-Channel field effect transistor
OC-192	Optical carrier level 192
OC-768	Optical carrier level 768
PBS	Polarization beam splitter
PC	Polarization controller
PFET	p-Channel field effect transistor
PMD	Polarization-mode dispersion
PMF	Polarization-maintaining fiber
PRBS	Pseudorandom bit sequence
PSP	Principle state of polarization
RF	Radio-frequency
RX	Receiver
SMF	Single-mode fiber
SOP	State of polarization
TF	Transversal filter
TIA	Transimpedance amplifier
TWA	Travelling-wave amplifier
TWF	Travelling-wave filter
TX	Transmitter
WDM	Wavelength-division multiplexed

Chapter 1

Introduction

1.1 Motivation

Optical communications systems have been used since the 1970s for high-volume data transmission within wide-area, metropolitan-area and local-area networks [1]. Until recently, long-haul links over single-mode fiber (SMF) could be designed without concern for the bandwidth limitations of the fiber. By compensating for fiber loss with amplifiers the reach of these systems could be extended. To satiate the demand for greater network capacity, the data rate of current optical systems has been pushed to 10 and 40 Gb/s (OC-192 and OC-768). At these data rates, it is no longer possible to neglect the bandwidth limitations of SMF, as several dispersion mechanisms lead to frequency-dependent loss [2].

The two most important dispersion mechanisms for SMF are chromatic dispersion (CD) and polarization-mode dispersion (PMD). CD is a result of the wavelength-dependency of the refractive index of the fiber. PMD results from the variation in the refractive index of the fiber with respect to the polarization of the light signal. Since CD can be compensated by proper choice of optical fiber, PMD has been identified as the limiting factor in high-speed optical systems [3].

To mitigate the effects of PMD, optical systems must include some form of PMD compensation. This compensation can be achieved either optically or electronically. Electronic PMD compensation schemes are attractive because they allow greater integration with existing circuitry, leading to more compact, less expensive solutions. This is especially true for wavelength-division multiplexed (WDM) systems, in which every channel needs PMD compensation [4]. Also, because PMD fluctuates with changes in temperature and environment, PMD compensators must be able to adapt to varying channel conditions within milliseconds [5]. Fast and accurate adaptation is more easily performed in the electronic domain. Successful electronic equalization has been demonstrated at 10 Gb/s [2, 6–10] and more recently, at 40 Gb/s [11, 12].

The goal of this thesis is to specify the requirements for a 40-Gb/s electronic PMD compensator and to design and implement such a compensator in a suitable IC process.

1.2 Chromatic Dispersion (CD)

CD is a result of the wavelength-dependence of the refractive index $n(\lambda)$ of the fiber. Since the propagation velocity of light in the fiber ν is related to the velocity of light in free space c and $n(\lambda)$ by:

$$\nu = \frac{c}{n(\lambda)} \tag{1.1}$$

the signal components in different wavelengths will reach the receiver at different times, causing dispersion and possibly inter-symbol interference (ISI).

CD can be mitigated by proper choice of optical fiber. Optical fibers exist for which the zero-dispersion wavelength (the wavelength of light at which no dispersion occurs) is the transmission wavelength for the system (1.55 μm, for example). Also, certain fibers exhibit reduced dispersion slope (the change in dispersion as the wavelength diverges from the zero-dispersion wavelength) so that CD is minimized over a wider

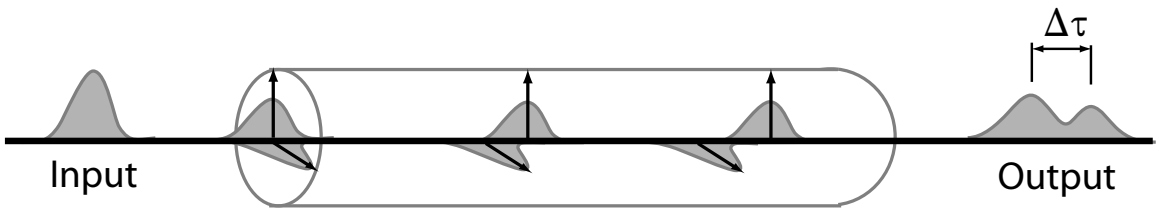


Figure 1.1: Pulse bifurcation due to PMD. The power in the input pulse is split between the two polarization modes of the fiber. Birefringence causes a difference in phase velocities between the two modes, resulting in ISI at the output.

range of wavelengths for WDM systems [13].

1.3 Polarization-Mode Dispersion (PMD)

PMD is a result of the phenomenon of birefringence which affects all real optical fibers. Birefringence refers to the difference in refractive index experienced by light in the two orthogonal polarization modes of the fiber. It is caused by ellipticity of the fiber cross-section due to asymmetric stresses applied to the fiber during or after manufacturing. Birefringence leads to fast and slow modes of propagation and consequently dispersion [14].

In terms of digital communications, PMD results to a first order in an input pulse being split into a fast and slow pulse which arrive at the receiver at different times, as shown in Figure 1.1. If the differential delay of the two pulses is significant compared to the bit period, ISI and an increase in bit-error rate (BER) will result.

1.3.1 Consequences of PMD for Optical Systems

To a first order, the impulse response of an optical fiber with PMD is [15]:

$$h_{\mathrm{PMD}}(t) = \gamma\delta(t) + (1-\gamma)\delta(t-\Delta\tau) \tag{1.2}$$

where γ is the proportion of the optical power in the "fast" state of polarization (SOP), (1-γ) is the proportion of power in the "slow" SOP and $\Delta\tau$ is the differential group delay (DGD) between the fast and slow components.

γ and $\Delta\tau$ vary depending on the particular fiber and its associated stresses. γ can by its definition take any value from zero to one, with uniform probability throughout this range [16]. $\Delta\tau$ varies statistically according to a Maxwellian distribution [17], given by:

$$\rho(\Delta\tau) = \sqrt{\frac{2}{\pi}}\frac{\Delta\tau^2}{\sigma^3}e^{-\frac{\Delta\tau^2}{2\sigma^2}} \tag{1.3}$$

The distribution is defined by σ, which is related to the average DGD, $\Delta\tau_{avg}$, by [18]:

$$\sigma = \frac{\sqrt{2\pi}\Delta\tau_{avg}}{4} \tag{1.4}$$

Therefore, though it can vary to large values, $\Delta\tau$ will for the most part remain close to some average value. $\Delta\tau$ varies with time and significant variations can be observed on the order of milliseconds [5].

The average DGD per unit length of a fiber is defined as its PMD parameter, which has units of ps/$\sqrt{\text{km}}$. Typical installed fibers exhibit a PMD of 0.5 - 2.0 ps/$\sqrt{\text{km}}$ [19]. New fibers can be manufactured with a PMD of as low as 0.05 ps/$\sqrt{\text{km}}$ [20]. Given the PMD parameter, the average DGD of a fiber of length L is given by:

$$\Delta\tau_{avg} = \text{PMD} \times \sqrt{L} \tag{1.5}$$

It has been calculated that to prevent PMD from causing system outages amounting to more than thirty seconds per year (corresponding to an outage probability of 10^{-6}), the average DGD must be less than approximately 15% of a bit period, T_B [3].

$$\Delta\tau_{avg} < 0.15T_B \tag{1.6}$$

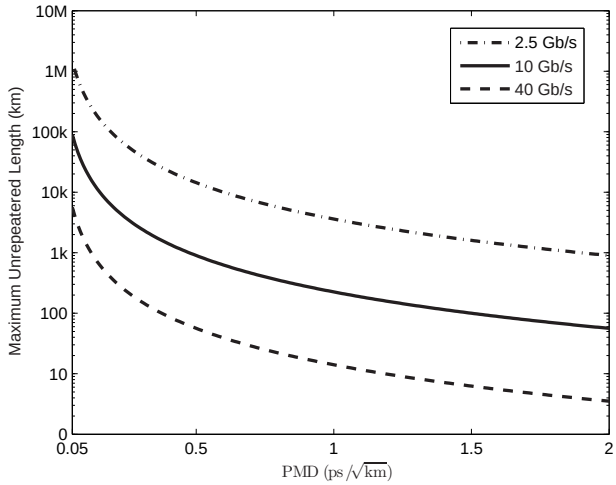


Figure 1.2: Plot of maximum unrepeatered link length for fibers with varying PMD parameters for 2.5-, 10- and 40-Gb/s optical systems, assuming PMD is the dominant limiting factor.

This has severe implications as the data rate of these systems is increased to 10 and 40 Gb/s. As the data rate is increased on a given fiber, the maximum useful length of the fiber decreases according to the square of the increase. For example, given a fiber with a PMD of 1.0 ps/$\sqrt{\text{km}}$ and using (1.6), the maximum length of a 2.5-, 10- and 40-Gb/s system is 3600, 225 and 14 km, respectively, if PMD is the limiting factor. This relationship is illustrated in Figure 1.2.

1.3.2 PMD Frequency-Domain Analysis

The frequency-domain characteristic of an optical fiber with PMD can be easily obtained by taking the Fourier transform of its impulse response, $h_{\text{PMD}}(t)$, as defined in (1.2). The transfer function, $H_{\text{PMD}}(f)$, is described by:

$$H_{\text{PMD}}(f) = \gamma + (1-\gamma)e^{-j2\pi f\Delta\tau} \tag{1.7}$$

which is equal to:

$$H_{\mathrm{PMD}}(f) = \gamma + (1-\gamma)[\cos(2\pi\frac{f}{f_{DGD}}) - j\sin(2\pi\frac{f}{f_{DGD}})] \tag{1.8}$$

where $f_{\mathrm{DGD}} = \frac{1}{\Delta\tau}$. By inspection of (1.8), it can be seen that $|H_{\mathrm{PMD}}(f)|$ has maximae at $f = kf_{\mathrm{DGD}}, k \in I$, and minimae at $f = \frac{(2k-1)}{2} f_{\mathrm{DGD}}, k \in I$.

Magnitude and phase plots of $H_{PMD}(f)$ for varying PMD conditions (γ and $\Delta\tau$) are shown in Figure 1.3. From these plots it is apparent that the frequency response of a PMD fiber varies greatly depending on the specific nature of the PMD conditions. In general, PMD causes notches in the frequency response of the fiber. The frequency of these notches is proportional to the DGD. The depth of these notches is dependent on γ, with the case $\gamma = 0.5$ resulting in nulls. The wide variation in potential frequency responses and the possibility of nulls in the frequency spectrum make equalization of this channel difficult.

1.4 PMD Compensation Methods

Forward error correction (FEC) [21, 22] and wavelength redundancy in WDM networks [23] have been suggested as means of mitigating the effects of PMD. However, direct compensation of PMD effects is often required either independent of or in conjunction with redundancy schemes [24, 25]. PMD can be directly compensated in any of the optical, optoelectronic and electronic domains. In this section, methods for compensation in each of these domains are described and compared.

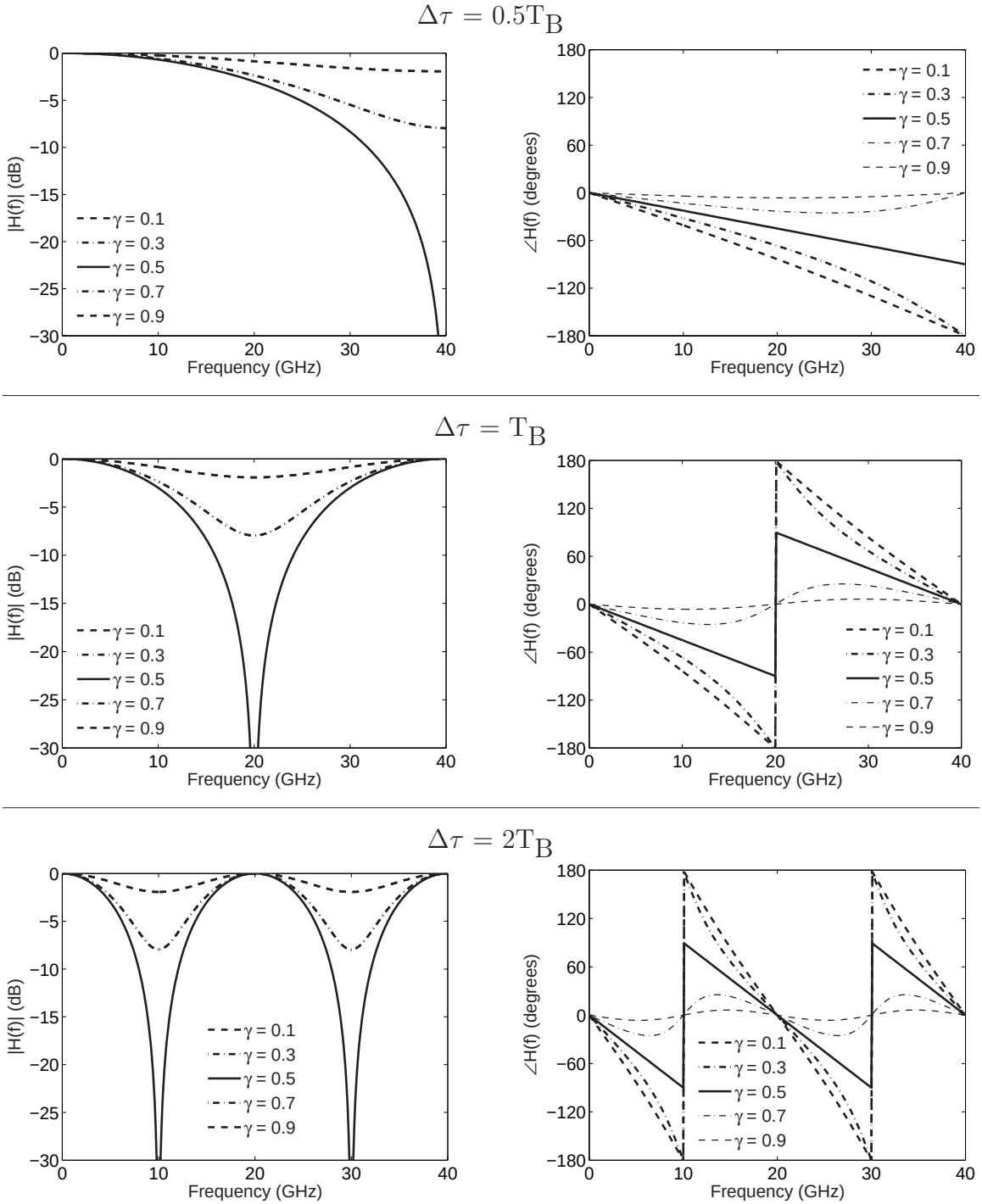


Figure 1.3: Magnitude and phase responses of PMD channels with varying γ and $\Delta\tau$ characteristics. T_B is a bit period (e.g. $T_B = \frac{1}{40Gb/s} = 25$ ps at 40 Gb/s).

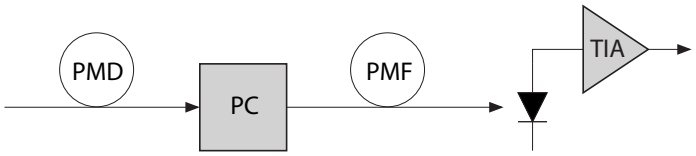


Figure 1.4: Simple optical PMD compensator architecture.

1.4.1 Optical PMD Compensation

Optical PMD compensation has been demonstrated to 160 Gb/s [26]. One of the most common optical PMD compensators requires a polarization controller (PC) and a length of polarization-maintaining fiber (PMF), as shown in Figure 1.4 [27]. The PC is used to align the polarization of the light signal such that it is aligned with the the principal states of polarization (PSPs) of the PMF. PMF is fiber which has been intentionally manufactured to have a large, but controlled, birefringence, and therefore can be used to generate a specific amount of DGD. In this way, the power in the fast SOP can be delayed by an amount equal to the DGD of the PMF, resulting in a reduction in the overall DGD. More complicated compensators can be made by replacing the fixed length of PMF with a variable delay to enable cancellation of arbitrary amounts of DGD, or by using multiple PC-PMF stages to increase the degrees of freedom and hence the accuracy of the compensation [28].

Despite the obvious advantages of compensating an optical phenomenon with optical components, optical compensation has several disadvantages. First, optical schemes require expensive and relatively bulky optical components. Also, because of the dynamic nature of PMD, compensators must be adaptive. Adaptation is not easily achieved in the optical domain because of the relative lack of flexibility in optical components, and because of the difficulty in extracting an appropriate error signal to control the adaptation.

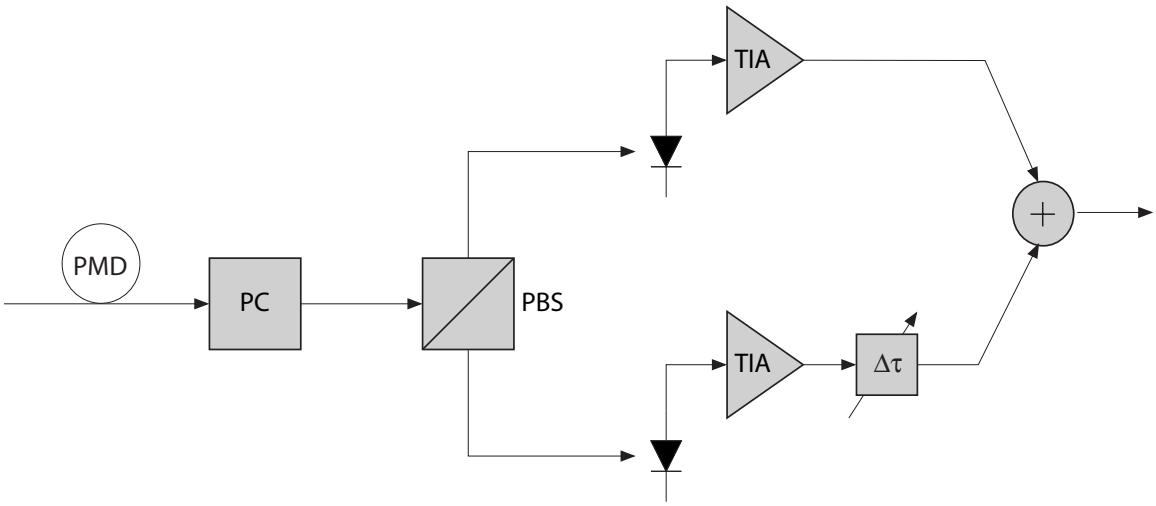


Figure 1.5: Typical optoelectronic PMD compensator architecture.

1.4.2 Optoelectronic PMD Compensation

It is also possible to compensate PMD using a scheme which involves both the optical and electronic domains. Typically, this scheme involves splitting the received light signal into its two polarization modes by a PC and a polarization beam splitter (PBS) [4]. The resulting light signals are then converted to electrical signals by two separate photodiode-transimpedance amplifier (TIA) front-ends. The electrical signal corresponding to the light in the fast SOP is then delayed by an interval equal to the DGD. Finally, the two signals are recombined to form a received signal that is free from PMD effects. This concept is illustrated in Figure 1.5.

The main advantage of optoelectronic compensation is that some of the compensation hardware is moved from the optical to the electronic domain, increasing the level of integration. However, optoelectronic compensation still requires extra optical components (PC and PBS), so greater integration is possible using an electronic scheme. Also, the addition of a second front-end is a significant expense.

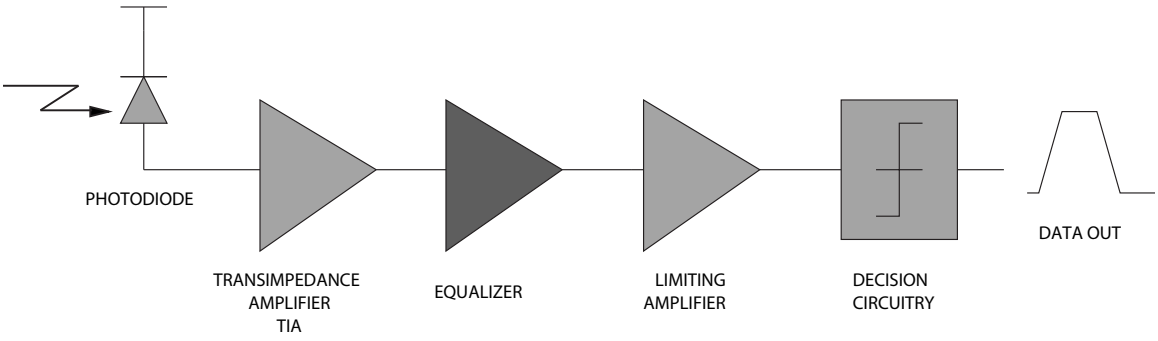


Figure 1.6: Block diagram of optical receiver including electronic PMD compensator.

1.4.3 Electronic PMD Compensation

Electronic PMD compensation is performed by equalization of the received signal after it has been converted from light to electricity by a photodiode and TIA. A system diagram of an optical receiver with an equalizer is given in Figure 1.6.

Electronic equalization is attractive because it offers a higher level of integration and hence a lower cost when compared to optical and optoelectronic solutions. A high level of integration is especially important in WDM systems, in which PMD compensation is required for each channel [4]. Also, the adaptation that is required to track changing PMD conditions is relatively simple to implement electronically, with established adaptation algorithms such as the least mean square (LMS) algorithm readily available. As a result of these considerations, electronic compensation is favoured when it is possible within the bounds of IC technology.

1.5 State of the Art

Because PMD has been identified as one of the factors limiting the effectiveness of high-speed optical links, significant effort has already been put into developing equalizers to compensate for it electronically in 10- and 40-Gb/s networks. The following represents a survey of reported equalizer implementations which have been

designed for PMD compensation in high-speed optical systems or which could be used for such a purpose.

It has been shown that nonlinear equalization using a decision feedback equalizer (DFE) is required to reduce the power penalty caused by PMD to acceptable levels [29]. The only 40-Gb/s DFE reported to date was reported by Nakamura *et al.* [11]. The DFE was implemented in a 150-GHz f_T InP process, and consists of a 3-tap feedforward equalizer (FFE) and a 1-tap feedback equalizer (FBE). Measurements have shown that this equalizer is able to compensate PMD with up to 20 ps of DGD while consuming a total of 2.12 W (FFE - 820 mW, FBE - 1.3 W).

A 10-Gb/s DFE was reported by Bülow *et al.* [6]. This DFE, consisting of an 8-tap (55 ps tap spacing) FFE and a 1-tap FBE was implemented in a SiGe process. Experimental measurements have shown that this equalizer is able to effectively equalize PMD for DGDs of up to one bit period.

Hazneci and Voinigescu [12] reported a 49-Gb/s transversal filter implemented in 0.18-μm SiGe BiCMOS. The filter has a tap spacing of 6.75 ps and cable equalization at 40 and 49 Gb/s was demonstrated. The equalizer makes use of a travelling-wave topology, with Gilbert cell tap multipliers distributed along the length of the input and output transmission lines. The nominal power consumption is 750 mW.

A 1-tap 10-Gb/s FBE implemented in an AlGaAs/GaAs high electron mobility transistor (HEMT) technology was described by Möller *et al.* [7]. The IC consumes 600 mW and equalization of PMD with DGDs up to 1.2 bit periods was demonstrated.

A 5-tap 10-Gb/s analog equalizer implemented in a 0.25-μm SiGe process was reported by Azadet *et al.* [2]. This IC targets equalization of both multi-mode fiber (MMF) and SMF, and equalization of PMD with DGD equal to half of a bit period was demonstrated.

Kanter *et al.* [8] reported a self-adaptive 10-tap FFE for equalization in a 10-Gb/s optical system. The stated objective of the equalizer is to increase the length of optical

links that use electro-absorption modulators (EAMs).

Wu *et al.* [9] reported a 7-tap (50 ps tap spacing) 10-Gb/s transversal equalizer for equalization of intermodal dispersion in MMF. The IC was implemented in a 0.18-μm SiGe BiCMOS process and consumes 40 mW. This equalizer makes use of a travelling-wave topology, with delays implemented using artificial L-C transmission lines and gain cells composed of Gilbert cell multipliers.

Pelard *et al.* [10] reported a 4-tap (33 ps tap spacing) FIR filter for 10-Gb/s MMF and backplane equalization. This equalizer was fabricated in a 0.18-μm CMOS process and consumes 7.3 mW from a 1.8-V supply. This equalizer also makes use of a travelling-wave topology.

1.6 Outline

In Chapter 2 a system-level analysis of a PMD channel using Matlab/Simulink is described. Chapter 3 contains a discussion of various circuit topology considerations pertinent to the design of a high-speed equalizer. Chapter 4 provides a description of a 40-Gb/s 3-tap transversal equalizer which has been designed and implemented in the TSMC 90-nm CMOS process. Chapter 5 provides a description of a 40-Gb/s 3-tap transversal equalizer which has been designed and implemented in the TSMC 0.18-μm CMOS process. Chapter 6 provides conclusions and a discussion of future research opportunities.

Chapter 2

System-Level Analysis

2.1 Introduction

As discussed in Section 1.4, electronic compensation of PMD is preferable to optical compensation in terms of ease of integration, cost and flexibility. However, the tradeoffs between different electronic equalizer architectures are not evident. In this section, a system-level analysis of PMD effects in a 40-Gb/s optical system using Matlab/Simulink is used to compare several equalizer architectures in terms of overall system performance, as has been done for optical compensation schemes [28]. The goal of this analysis is to identify an equalizer architecture which can provide effective PMD compensation and which can realistically be implemented in a current IC process.

Section 2.2 provides a description of the system model used for the Matlab/Simulink simulations. In Section 2.3 the various equalizer architectures considered for PMD compensation are described. Section 2.4 explains the methodology of the simulations performed. Section 2.5 contains the results of these simulations and Section 2.6 concludes this chapter by identifying the most promising architecture for implementation.

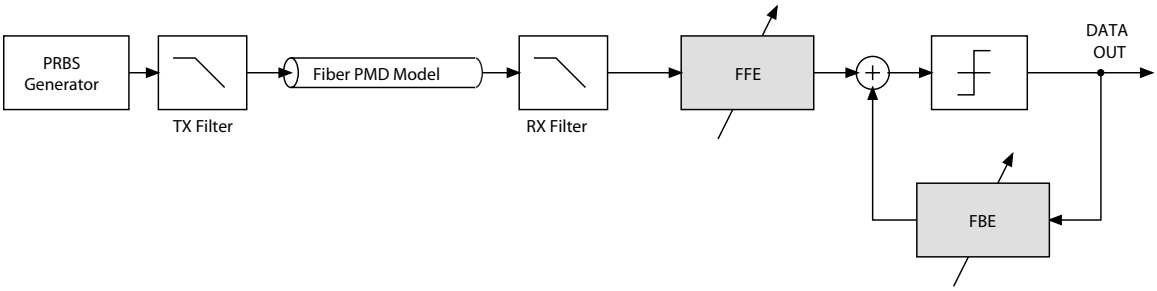


Figure 2.1: System model used for Matlab/Simulink simulations.

2.2 System Model

Matlab/Simulink was used to simulate the effects of PMD in an optical system and to compare various equalizer architectures in terms of their compensation abilities. A simplified block diagram of the system used in these simulations is given in Figure 2.1. A pseudorandom bit sequence (PRBS) generator is used to generate input data at a rate (R) of 40 Gb/s. This data is passed through a first-order lowpass filter ($f_{3dB} = 0.7 \times R$) used to simulate the effects of the finite bandwidth of the transmitter (TX). It is then passed through an optical fiber model which corrupts the data with PMD. The fiber is modelled using (1.2). At the output of the fiber model the data is filtered with another first-order lowpass filter ($f_{3dB} = 0.7 \times R$) to simulate the finite bandwidth of the receiver (RX). Equalization is then performed and the equalized waveform is sliced to generate the output data.

Not shown in Figure 2.1 are the clock recovery and adaptation components of the system. The sampling phase was determined by automatically selecting the clock phase corresponding to the largest eye opening at the output of the channel. Coefficient adaptation for both the FFE and FBE was performed using the LMS algorithm.

Figure 2.1 shows the equalizer as a DFE, though several equalizer architectures were considered.

2.3 Equalizer Architectures

2.3.1 Analog Equalizer

Analog or "peaking" equalizers have been used in the past for equalizing simple low-pass channels [30]. The potential advantage of this architecture is its relatively simple implementation. However, the analog equalizer is unsuitable as a PMD compensator because it is not flexible enough to adapt to the wide range of potential PMD conditions. Also, because it is a linear circuit it is unable to compensate for the deep null in the frequency spectrum caused by PMD with γ values near 0.5.

2.3.2 IIR Equalizer

The infinite impulse response (IIR) equalizer would seem to have great potential as a PMD compensator. Because the frequency response of the PMD channel is given by (1.7), the inverse of the channel transfer function is:

$$H_{\mathrm{PMD}}^{-1}(f) = \frac{1}{\gamma + (1-\gamma)e^{-j2\pi f \Delta\tau}} \tag{2.1}$$

$H_{\mathrm{PMD}}^{-1}(f)$ also relates the input $X(f)$ and output $Y(f)$ of the inverse filter:

$$H_{\mathrm{PMD}}^{-1}(f) = \frac{Y(f)}{X(f)} \tag{2.2}$$

Solving for $Y(f)$ we get the input-output relationship:

$$Y(f) = \frac{1}{\gamma}X(f) + \frac{\gamma - 1}{\gamma}e^{-j2\pi f \Delta\tau}Y(f) \tag{2.3}$$

Taking the inverse Fourier transform of (2.3) we get the difference equation:

$$y(t) = \frac{1}{\gamma}x(t) + \frac{\gamma - 1}{\gamma}y(t - \Delta\tau) \tag{2.4}$$

This difference equation describes an IIR filter. While this architecture would seem to offer perfect (zero-forcing) equalization of a PMD channel, the nature of the feedback loop creates problems in practice. Specifically, for $\gamma \leq 0.5$, the equalizer loop gain, which is equal to $\frac{\gamma-1}{\gamma}$ by inspection of (2.4) is less than -1, meaning that the equalizer is unstable. Thus, since it is unable to compensate PMD for all values of γ, the IIR filter is unsuitable for implementation as a PMD compensator.

2.3.3 FIR Equalizer

The finite impulse response (FIR) filter is a versatile equalizer architecture which is widely used. FIR filters can, given enough taps, approximate any linear transfer function, making them attractive because of their flexibility. However, the usefulness of an FIR filter as a PMD compensator is severely limited because, as a linear filter, it is unable to compensate for the deep nulls caused by PMD with γ values near 0.5.

2.3.4 Decision Feedback Equalizer

Figure 2.1 illustrates the basic DFE topology. The DFE consists of an FFE and an FBE, both of which can be implemented as FIR filters for maximum flexibility. The most important advantage of the DFE architecture in terms of PMD compensation is that the use of an FBE introduces nonlinear equalization, allowing compensation of the nulls resulting from γ values near 0.5 [29]. Because of this, the DFE is the only architecture surveyed that meets the requirements for an electronic PMD compensator.

The main disadvantage of the DFE is its difficult implementation at high speeds,

as a result of the feedback loop inherent to the FBE. However, architectural techniques such as the look-ahead DFE (LADFE) architecture [31] can alleviate this problem.

2.4 Simulation Methodology

Having identified the DFE architecture as the most suitable, simulations were performed to identify the performance tradeoffs with respect to number of equalizer taps (FFE and FBE). All simulations were performed with symbol-spaced equalizer taps unless otherwise noted.

For each equalizer configuration, it was necessary that a wide range of PMD conditions were considered. $\Delta\tau$ was varied from 0 to 100 ps (4 bit periods at 40 Gb/s) and γ was varied from 0 to 1. For each ($\Delta\tau$,γ) pair the equalizer was allowed to converge to the ideal tap weights as determined by the LMS algorithm. Then, the ISI penalty was determined by calculating the amount of eye closure using [32]:

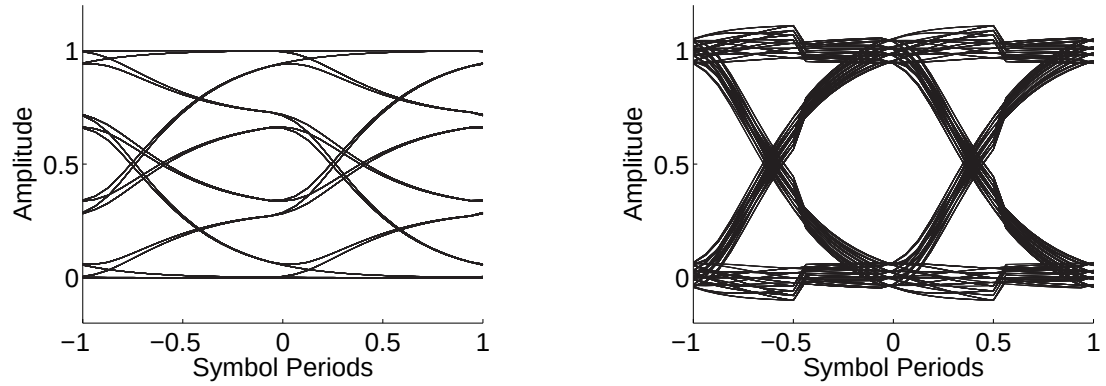
$$\text{ISI penalty (dB)} = 10 \times \log_{10}(\frac{max.\ eye\ opening}{min.\ eye\ opening}) \tag{2.5}$$

Figure 2.2 shows representative eye diagrams for the unequalized and equalized case for one particular ($\Delta\tau$,γ) pair. Figure 2.3 shows surface plots of the ISI penalty for the unequalized and one equalized case over a range of ($\Delta\tau$,γ) pairs. This plot demonstrates the elimination of the penalty pole at $\Delta\tau = 25$ ps, $\gamma = 0.5$ by equalization with a DFE.

Once the ISI penalty had been calculated for all ($\Delta\tau$,γ) pairs, the cumulative probability (CP) of a system outage given a particular power margin was calculated using [16]:

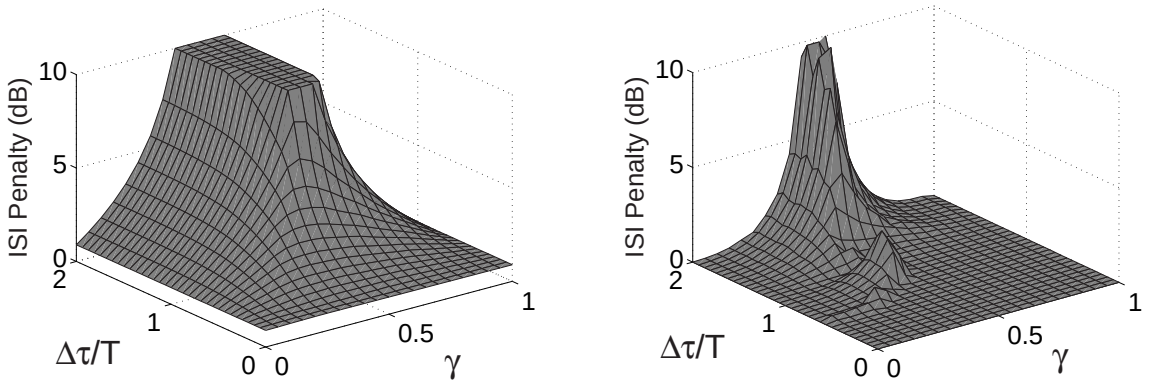
$$\text{CP} = \sum_{(\Delta\tau,\gamma)'} \rho_1(\Delta\tau)\rho_2(\gamma) \tag{2.6}$$

where $\rho_1(\Delta\tau)$ is the probability distribution of $\Delta\tau$ as described by (1.3), $\rho_2(\gamma)$ is the



a) b)

Figure 2.2: Eye diagrams for $\Delta\tau = 25$ ps, $\gamma = 0.3$. a) No equalization. b) Equalization by 3-tap FFE and 1-tap FBE.



a) b)

Figure 2.3: ISI penalty vs. $\Delta\tau$ and γ. ISI penalty is truncated at 10 dB. a) No equalization. b) Equalization by 3-tap FFE and 1-tap FBE.

probability distribution of γ (uniform) [16] and $(\Delta\tau, \gamma)'$ is the set of $(\Delta\tau, \gamma)$ pairs for which the ISI penalty is greater than the power margin. Power margin represents the ratio of the transmitted power to the transmitted power required for a given BER (e.g. 10^{-12}). When the ISI penalty exceeds the power margin, a system outage occurs because the excess transmitted power cannot overcome the eye closure caused by the ISI, and the BER increases above the specified maximum tolerable level.

As described in Section 1.3.1, $\rho_1(\Delta\tau)$ depends on the average DGD of the particular fiber. For each equalizer configuration, the probability distribution was varied by adjusting the average DGD to find the maximum average DGD that would result in a CP of less than 10^{-6} (30 seconds per year).

To summarize, for each equalizer configuration (number of taps) the ISI penalty contour is calculated over all γ and $\Delta\tau$. For a given power margin, the $(\gamma, \Delta\tau)'$ pairs corresponding to a system outage are those pairs that give an ISI penalty greater than the power margin. The joint probabilities of occurrence for all of the $(\gamma, \Delta\tau)'$ pairs contributing to system outage are then summed to find the overall system outage probability. As long as this overall system outage probability remains lower than 10^{-6}, the average DGD is increased and the calculation repeated. The maximum average DGD that results in an overall outage probability of less than 10^{-6} is then recorded as a measure of performance for comparison with other equalizer configurations.

2.5 Simulation Results

Figures 2.4, 2.5 and 2.6 show the results of these simulations for an FFE only, a DFE with a 1-tap FBE and a DFE with a 2-tap FBE, respectively. In each case, the maximum average DGD that is tolerable from a system point of view is plotted against the power margin for different numbers of FFE taps. In addition, the unequalized case is included as a reference for comparison. Figure 2.4 shows that using an FFE

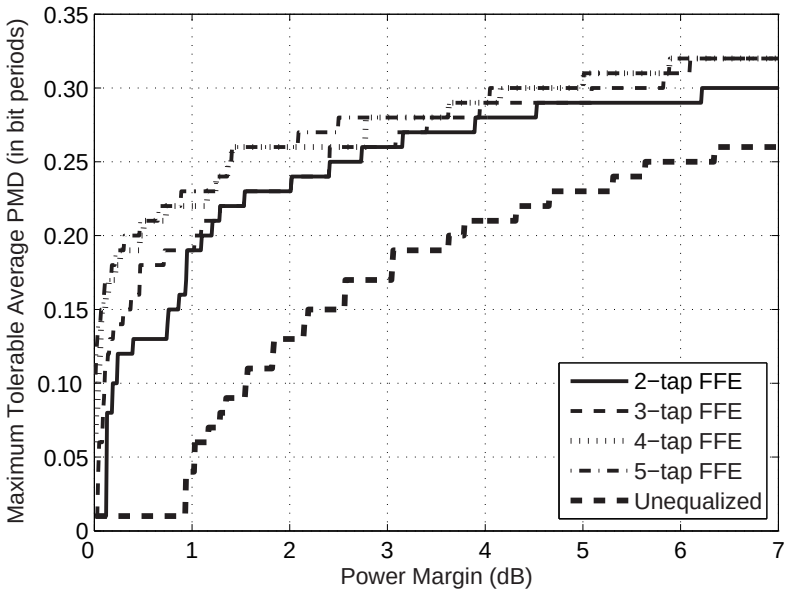


Figure 2.4: Plot of maximum tolerable PMD vs. power margin for FFEs with varying number of taps (No FBE).

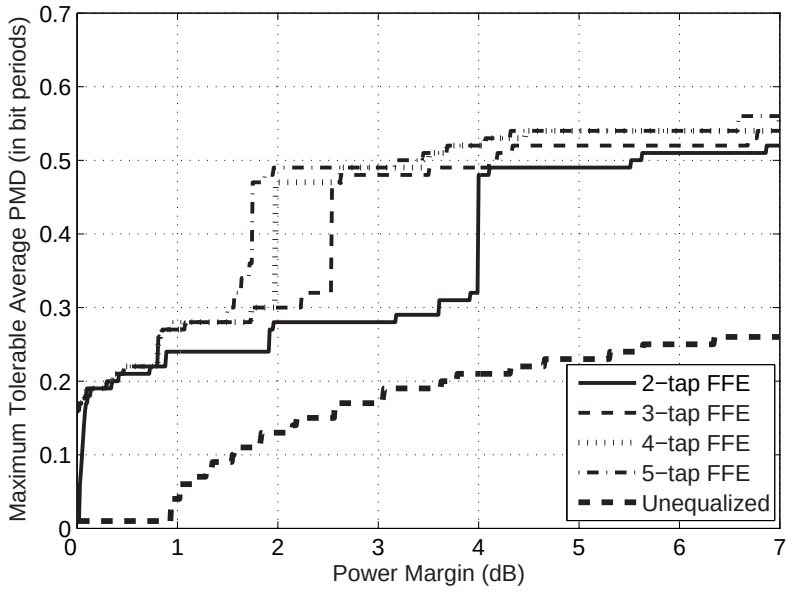


Figure 2.5: Plot of maximum tolerable PMD vs. power margin for FFEs with varying number of taps (1-tap FBE).

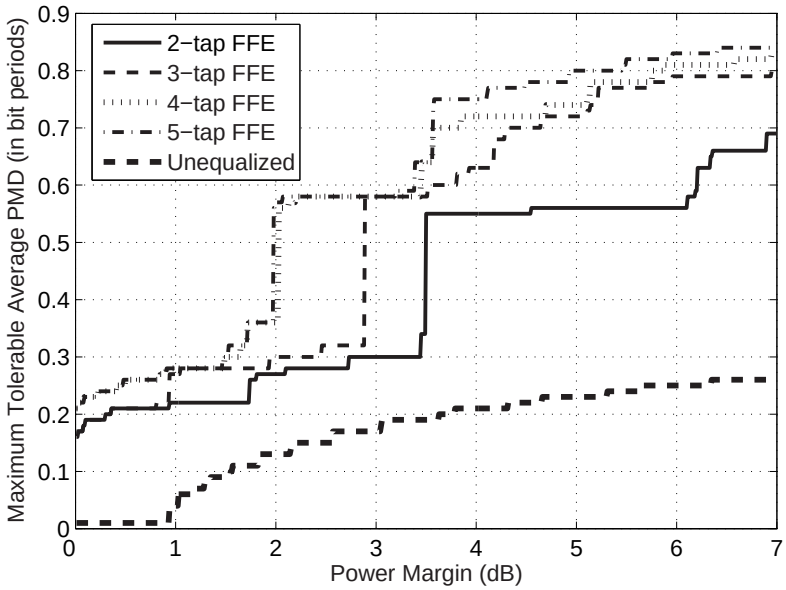


Figure 2.6: Plot of maximum tolerable PMD vs. power margin for FFEs with varying number of taps (2-tap FBE).

only, a modest increase in maximum average DGD is possible, from roughly $0.15T_b$ to $0.25T_b$. Only minor improvements are achievable by increasing the number of FFE taps because regardless of the number of taps the FFE is unable to compensate for the case $\Delta\tau = 25$ ps, $\gamma = 0.5$. Figure 2.5 demonstrates that by using a 1-tap FBE, a significant performance increase is possible, with the maximum average DGD increasing to approximately $0.5T_b$. For this case, the number of FFE taps offering the best balance between performance and complexity is dependent on the power margin. For power margins below 3 dB, four taps offer the best balance, while three taps offer the best balance for power margins above 3 dB. Figure 2.6 shows that a further increase in maximum average DGD is possible by using a 2-tap FBE, but significant gains are limited to power margins above 4 dB. Once again, four FFE taps offer the best balance for power margins below 3 dB, while three taps offer the best balance for power margins above 3 dB.

Figure 2.7 shows the maximum average DGD plotted against the number of FFE

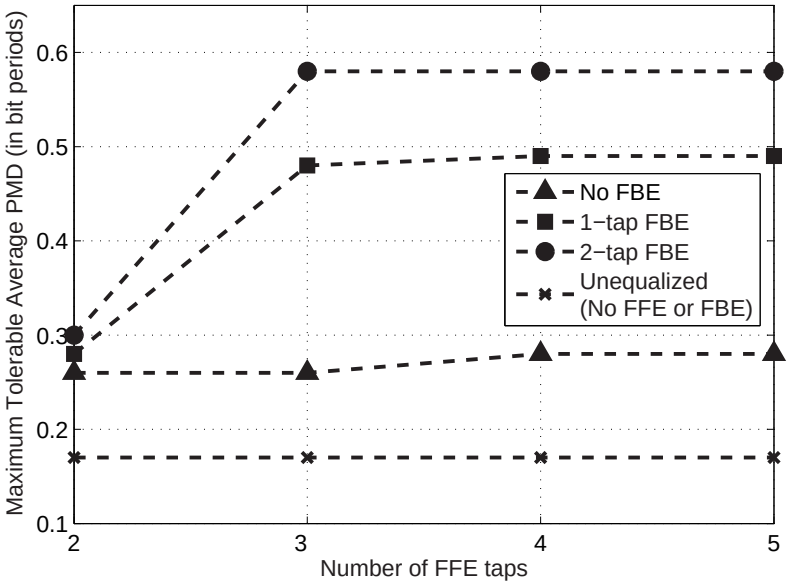


Figure 2.7: Plot of maximum tolerable PMD vs. number of FFE taps for no FBE, 1-tap FBE and 2-tap FBE at a power margin of 3 dB.

taps for a power margin of 3 dB. Once again, the unequalized case is included for comparison. This plot more clearly shows the performance of each of the equalizer architectures. It is clear from this plot that for a power margin of 3 dB, a 3-tap FFE offers performance nearly equal to the more complex 4- and 5-tap FFEs. As expected, the 2-tap FBE offers a modest performance increase over the 1-tap FBE. However, the 1-tap FBE may be a more attractive choice when this performance increase is weighed against the added complexity of a second tap.

These results are significant because they imply that the useful length of high-speed optical systems affected by PMD can be greatly increased by including electronic PMD compensation in the form of a DFE. To keep system outage levels at an acceptable level, $\Delta\tau_{avg}$ must be less than the maximum average DGD. Therefore, using (1.5) it is found that the useful length of the fiber increases with the square of the increase in maximum average DGD. As an example, consider a 40-Gb/s system for which the PMD of the fiber is 1.0 ps/$\sqrt{\text{km}}$, and the power margin is 3 dB. From

Figure 2.7, the maximum average DGD for an unequalized system at a power margin of 3 dB is $0.17T_b$, corresponding to a maximum system length of 18 km, using (1.5). The maximum average DGD for a system using a DFE with a 3-tap FFE and 1-tap FBE is $0.49T_b$, corresponding to a maximum system length of 150 km. Therefore, an increase in maximum length of more than eight times is achieved by equalization.

While considering the increase in system length due to equalization, it must be noted that this calculation assumes that PMD is the dominant factor limiting the length of the system. In practice, other impairments (noise, CD) would likely replace PMD as the limiting factors once PMD had been compensated (although equalization would also help to compensate CD). As a result, the increase in system length would be less than predicted. The main conclusion, however, is still valid: electronic equalization using only a few taps can significantly reduce the impact of PMD on 40-Gb/s optical systems, resulting in an increase in system reach and the elimination of PMD as the dominant length-limiting factor.

2.5.1 Fractionally-Spaced Equalization

Fractionally-spaced equalizers (FSEs), for which the tap spacing is $T_B/2$, were also considered for the FFE. Figure 2.8 shows the maximum average PMD for fractionally-spaced and symbol-spaced FFEs with a 1-tap FBE for a system power margin of 3 dB. The two equalizer configurations are compared in terms of equalizer span, i.e. the difference in delay between the first tap and the last tap of the equalizer. Equalizer span is important in PMD compensation because it determines the maximum amount of DGD that the equalizer can handle. From this plot, it is seen that for a given span, the FSE provides a performance increase over the symbol-spaced equalizer. However, the gain through each tap of an FSE may be limited to one half that through each tap of a symbol-spaced equalizer because of topological considerations. For the case where noise is the limiting factor (PMD is negligible) and only one equalizer tap is needed,

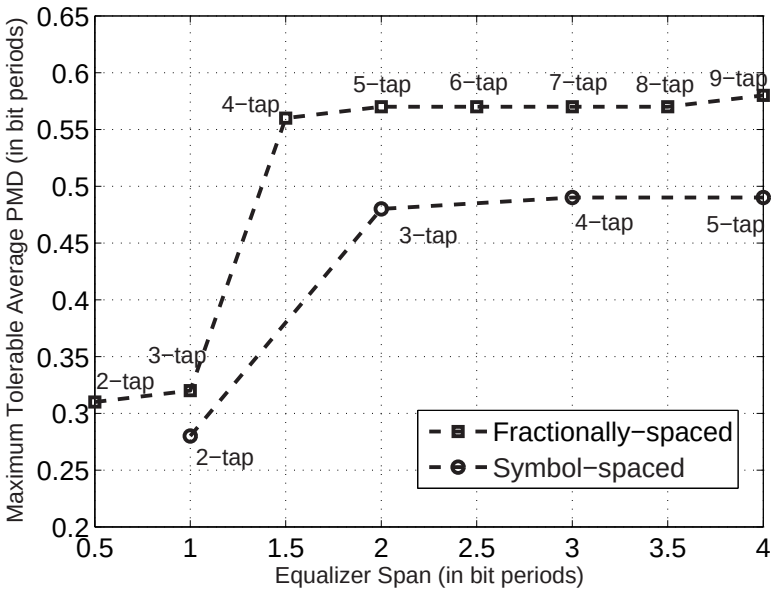


Figure 2.8: Plot of maximum tolerable PMD vs. equalizer span for fractionally-spaced and symbol-spaced FFEs and a 1-tap FBE at a power margin of 3 dB.

an FSE with only half the tap gain will require a power margin 3 dB higher than a symbol-spaced equalizer for equal performance. Therefore, the performance increase demonstrated in Figure 2.8 is exaggerated somewhat. Also, increasing the number of taps by decreasing the tap spacing increases the complexity of the adaptation required, making it more difficult to achieve convergence of tap values. Finally, for digital signal processing (DSP) applications, an FSE is often chosen over a symbol-spaced equalizer because the FSE enables matched filtering at the receiver for optimal noise performance. This advantage is reduced for analog applications, for which the limited bandwidth of the analog electronics provides some measure of noise filtering. For these reasons the FSE was not considered further in this study.

2.5.2 Variable Tap Delays

One observation from these simulations is that the usefulness of a PMD compensator is limited by its span. An equalizer is powerless to compensate for PMD with DGD exceeding its span. To increase the amount of DGD that can be compensated, more taps can be added. However, in a PMD compensator with many taps, only the first taps will be utilized for small DGD values while only the first and last taps will be utilized for large DGD values. Alternatively, an equalizer with only a few taps can perform equally as well as one with many taps if the tap delays can be made variable. Variable tap delays allow the tap spacing to be aligned with the DGD, maximizing the compensation accuracy with the fewest possible taps. Such an equalizer is left for future consideration, however, as there is currently no acceptable method of implementing variable delays with the required tuning range and bandwidth.

2.6 System-Level Conclusions

A system-level analysis using Matlab/Simulink has been performed to compare the performance of different electronic PMD compensator architectures at 40 Gb/s. It has been demonstrated that equalization by a DFE with a 3-tap FFE and a 1-tap FBE is able to increase by nearly three times the maximum average DGD that is tolerable from a system point of view, from $0.17T_b$ to $0.49T_b$. This is significant because it implies an increase in the useful length of a given PMD-limited system of more than eight times (e.g. from 18 km to 150 km for a fiber with a PMD of 1.0 ps/$\sqrt{\text{km}}$).

Based on these results, it is suggested that a DFE with a 3-tap FFE and a 1-tap FBE would be a suitable candidate for implementation. This architecture offers the most attractive balance between performance and complexity. The remainder of this thesis is concerned with the design and implementation of the FFE portion of the DFE. The implementation of an FBE is left for future study.

Chapter 3

Circuit Topologies for High-Speed FIR Filters

The design of a circuit operating at 40 Gb/s requires proper selection of topology to ensure that it can provide the required performance and to ensure that its layout is feasible. In this chapter, topological considerations for the design of 40-Gb/s equalizers are described. Section 3.1 discusses the tradeoff between analog and digital implementations. Section 3.2 compares two FIR topologies, the transversal filter (TF) and the travelling-wave filter (TWF). Section 3.3 describes the design of TWFs, and introduces two new TWF topologies. Conclusions are drawn in Section 3.4.

3.1 Analog vs. Digital Equalizer Implementation

The first major choice that must be made regarding the implementation of a high-speed FIR equalizer is whether to implement it in the analog or the digital domain.

Digital FIR equalizers are very powerful and robust. Digital delays can be easily implemented using flip-flops, and the accuracy of the multiplication and summation blocks is limited only by the numeric precision of the digital circuitry. However, a

digital FIR filter must be preceded by a very high-speed analog to digital converter (ADC). For a 40-Gb/s optical communications system, the ADC would need to operate at 40 GS/s, have an input bandwidth of at least 20 GHz, and provide at least a few bits of resolution. The design of such an ADC is not trivial and currently no suitable ADC exists. The current state of the art in ADCs is a 10-GS/s, 5-bit ADC consuming 3.6 W which has been implemented in a 0.18-μm SiGe BiCMOS process [33]. Even if a suitable ADC did exist, the large power consumption and size of the conversion circuitry would still potentially leave the analog FIR filter as the most attractive choice. Therefore, the digital FIR equalizer was not considered further in this study.

Analog FIR equalizers are made up of analog multipliers and summers. Discrete-time analog equalizers make use of clocked sample and hold blocks to implement delays. Continuous-time analog equalizers must implement continuous delays with either active or passive components. For this study, the continuous-time architecture was chosen because it was judged that passive analog delays would be simpler to implement at 40 Gb/s than sample and hold blocks.

3.2 FIR Filter Topologies

In this section, two FIR filter topologies are described. Section 3.2.1 describes the conventional FIR topology, the transversal filter. Section 3.2.2 describes the travelling-wave FIR topology, which is more suitable for high-speed implementation.

3.2.1 Transversal FIR Topology

The topology that is conventionally used to represent an FIR filter is the transversal filter topology, shown in Figure 3.1. For an N-tap filter, the delay line is tapped at specific intervals to generate N delayed versions of the input signal $x(t)$. These delayed

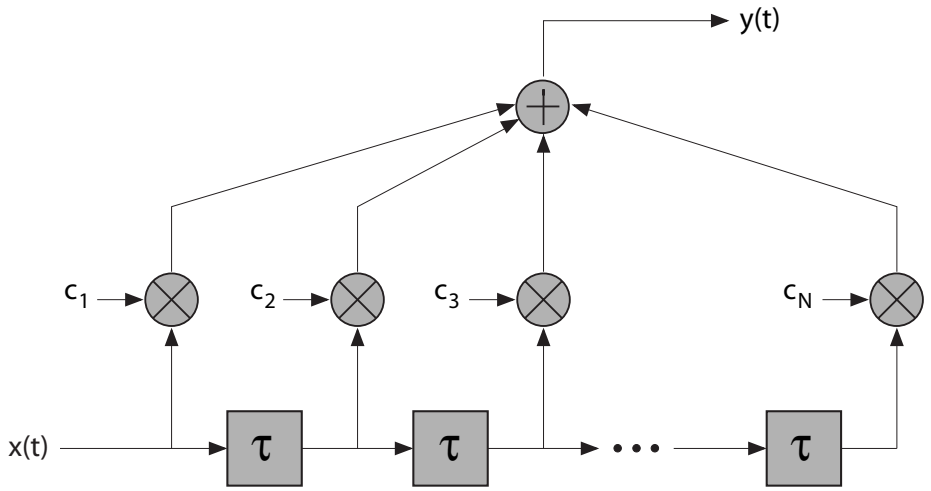


Figure 3.1: Transversal FIR filter topology.

versions are scaled by the tap weights c_k and then combined to form an output $y(t)$ of the form:

$$y(t) = \sum_{k=1}^{N} c_k x(t - (k-1)\tau) \tag{3.1}$$

where τ is the tap spacing.

While Figure 3.1 describes the TF topology in its most general form, Figure 3.2 illustrates the TF topology as it would appear for a high-speed implementation [34]. The delay line is implemented using passive components and terminated to prevent reflections. The tap multipliers are implemented as transconductors, with the summation performed in the current domain. Figure 3.2 will be used to illustrate why the TF topology is suitable for most low-speed analog and digital FIR implementations but is not well-suited for high-speed designs.

First, the outputs of the tap multipliers are tied together at the summation node. As a result, the capacitance at this node is very large and potentially speed-limiting. In addition, if the delay line is implemented using passive elements the inter-tap spacing may be quite large, making it physically difficult to tie these outputs together at a single node without introducing skew and signal degradation.

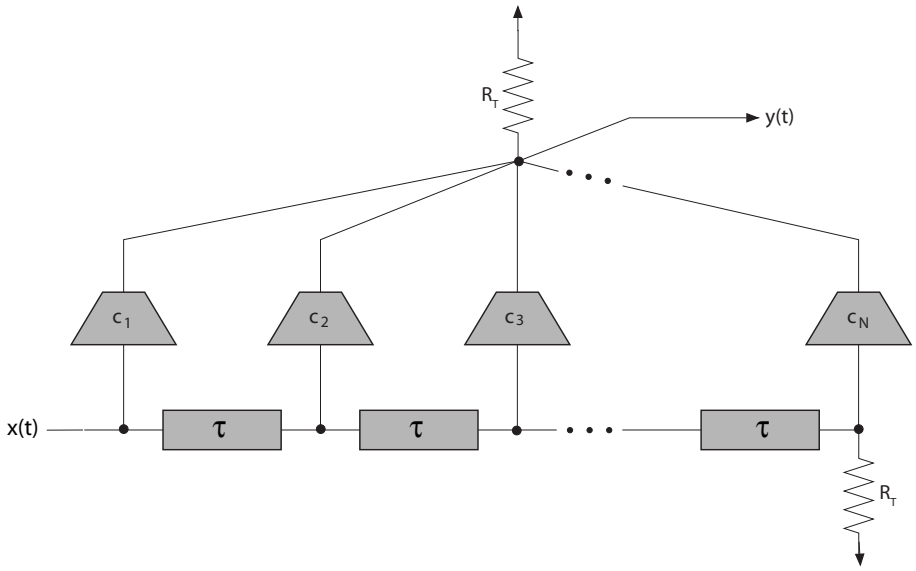


Figure 3.2: High-speed implementation of transversal FIR filter.

Finally, because the delay line is equal to the span of the equalizer, reflections which occur at the end of the delay line can be detrimental to the equalizer performance. For example, consider a 3-tap symbol-spaced equalizer. A reflection at the end of the 2-section delay line will traverse back to the first tap after four symbol periods. Thus, if Γ_T is the reflection coefficient at the end of the delay line, the output will not be equal to (3.1), but:

$$y(t) = c_1[x(t) + \Gamma_T x(t-4\tau)] + c_2[x(t-\tau) + \Gamma_T x(t-3\tau)] + c_3 x(t-2\tau) \qquad (3.2)$$

assuming that the higher-order Γ_T terms (Γ_T^2, Γ_T^3, etc.) are negligible. Therefore, the output contains terms involving $x(t-4\tau)$ and $x(t-3\tau)$ that are outside the span of the equalizer and that cannot be eliminated by adjusting the equalizer coefficients. In effect, these terms serve to increase the ISI at the output [34].

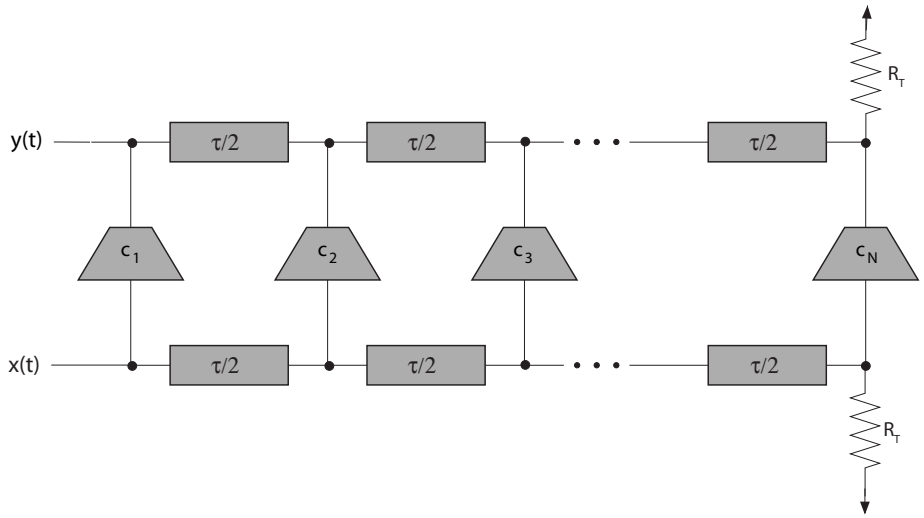


Figure 3.3: High-speed implementation of travelling-wave FIR filter topology.

3.2.2 Travelling-Wave FIR Topology

The travelling-wave filter FIR topology was first suggested by Rauscher [35], and is shown in Figure 3.3. The main difference between this topology and the TF is that this topology makes use of delay lines at both the input and the output. While the output $y(t)$ is still given by (3.1), this topology addresses some of the major issues with the TF topology that arise at high speeds.

First, there is no longer a lumped node at which all of the outputs are tied together. The capacitance at the inputs and outputs of the tap multipliers serve only to increase the capacitance of the input and output delay lines, respectively. In other words, the device capacitances are distributed along the length of the delay lines.

Also, this topology lends itself to an efficient layout because the inter-tap spacing is the same for both the input and output lines. The input and output lines can be laid out parallel to one another, with the tap multipliers interspersed between them.

Finally, this topology offers an improvement over the TF in terms of robustness in the presence of reflections. Using the example of a 3-tap filter, the output in the

presence of reflections is:

$$y(t) = c_1[x(t) + 2\Gamma_T x(t-2\tau)] + c_2[x(t-\tau) + 2\Gamma_T x(t-2\tau)] + c_3 x(t-2\tau) \quad (3.3)$$

In contrast to (3.2), (3.3) does not contain any terms outside the span of the equalizer. Therefore, the extra $x(t-2\tau)$ terms caused by the reflections can be compensated for by properly adjusting the weighting coefficient for the third equalizer tap [34].

Because of these benefits, many of the reported FFE implementations make use of the TWF topology [9–12].

Distributed Amplifier Analogues

The TWF is closely related to the travelling-wave or distributed amplifier (TWA or DA). The basic DA topology with common source (CS) amplification devices is shown in Figure 3.4. The delay from input to output is equal for all signal paths, such that the signal adds constructively at the output. The DA allows amplification with a very high gain-bandwidth product by distributing the amplification device capacitances along input and output transmission lines. In effect, the DA trades delay for increases in gain and bandwidth [14].

Figure 3.5 illustrates the TWF topology with CS tap multipliers. An immediate observation from Figures 3.4 and 3.5 is that the TWF topology is identical to that of the DA topology with the exception that the output is taken from the opposite end of the output transmission line. This observation is quite useful for the design of TWFs, as the operational and design principles of DAs are well established and can be extended to TWFs without modification.

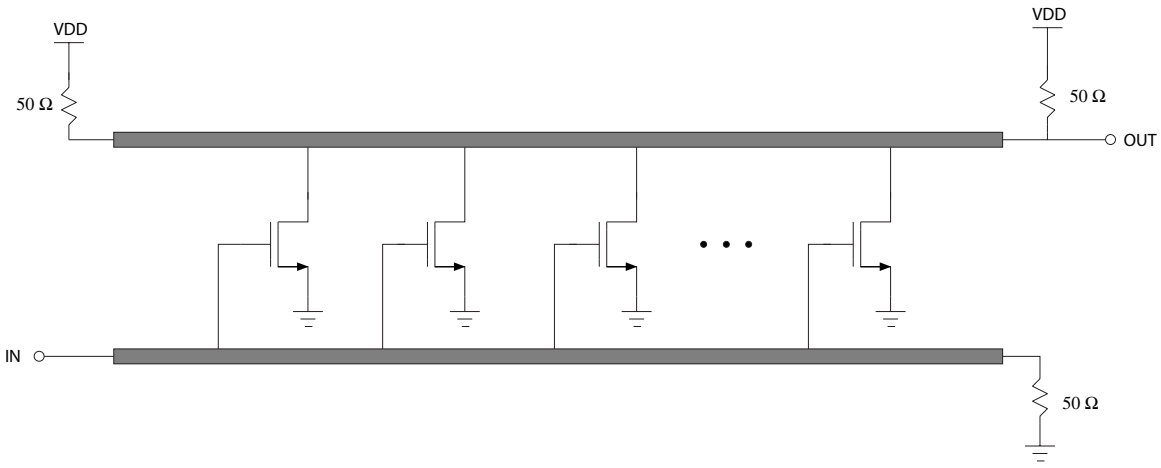


Figure 3.4: Distributed amplifier topology.

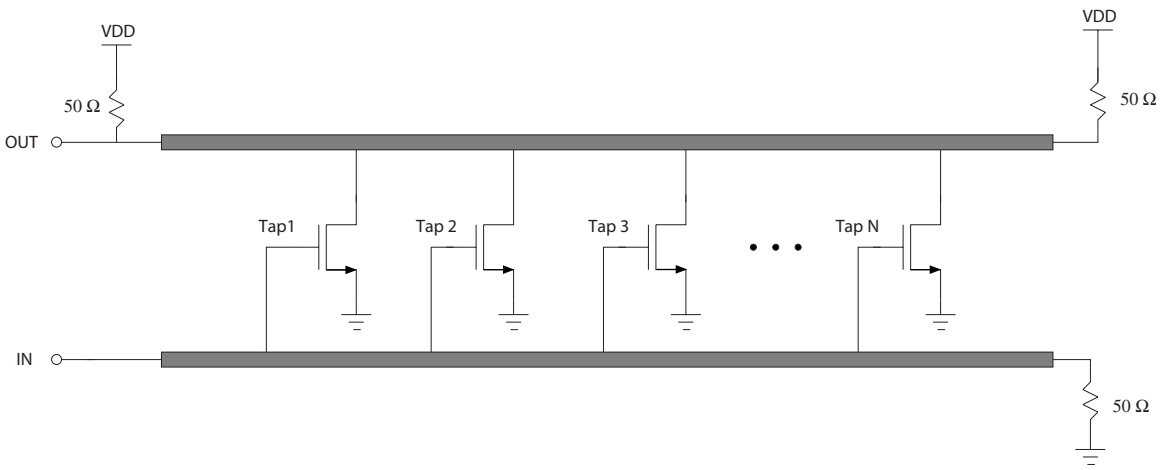


Figure 3.5: Travelling-wave filter topology.

3.3 Travelling-Wave Filter Design

This section describes the basic methodology used in the design of a TWF, which was identified in Section 3.2 as an appropriate implementation of an FIR filter for high-speed design. As described in Section 3.2.2, the TWF can be thought of as a DA with its output taken from the opposite end. Therefore, the design methodology closely parallels that of a DA [14].

The basic TWF design is shown in Figure 3.3. The input and output transmission lines are chosen such that their characteristic impedance is matched to the system impedance and their delays implement the proper tap spacing. The input and output capacitances of the tap multipliers serve to capacitively load the input and output transmission lines, respectively. This loading effectively reduces the characteristic impedance of the transmission lines and must be considered in the design.

3.3.1 Artificial L-C Transmission Lines

To achieve the required delays for a 40-Gb/s equalizer, the transmission lines used in the input and output must be very long (on the order of several millimeters). As a result, the size of the equalizer IC can become prohibitively large. In addition, long transmission lines introduce significant series loss. For both of these reasons, it is desirable to minimize the length of these lines.

Using artificial transmission lines made up of lumped inductors and capacitors addresses both problems associated with distributed transmission lines. By winding the transmission line into spiral inductors, the inductance per unit length is greatly increased because of the mutual inductance between adjacent windings. Thus, the overall length of transmission line is decreased, reducing the chip area as well as any resistive losses.

The design of a TWF with artificial transmission lines is fairly straightforward,

as most of the design variables are fixed by the desired configuration of the equalizer. The delays of the input and output transmission lines are determined by the desired tap spacing. The delay ΔT of a lumped L-C transmission line section is approximately equal to:

$$\Delta T = \sqrt{L'C'} \tag{3.4}$$

where L' and C' are the inductance and capacitance of each section of the transmission line, respectively. Also, the characteristic impedance of the input and output transmission lines (Z_0) is determined by the system impedance (e.g. 50 Ω), and is equal to:

$$Z_0 = \sqrt{\frac{L'}{C'}} \tag{3.5}$$

Substituting (3.5) into (3.4) we can solve for L' and C':

$$L' = Z_0 \Delta T \tag{3.6}$$

$$C' = \frac{\Delta T}{Z_0} \tag{3.7}$$

As an example, consider a 3-tap symbol-spaced equalizer operating at 40 Gb/s with a system impedance of 50 Ω. The delay per transmission line section should be $\frac{T_B}{2}$, or 12.5 ps. Using (3.6) and (3.7) L' is equal to 625 pH and C' is equal to 250 fF. The input and output capacitances of the tap multipliers effectively add to the capacitance of the input and output transmission lines, respectively. Therefore, C' is made up of the sum of the transmission line capacitances and the device capacitances. The termination resistors R_T are set equal to the system impedance. The resulting equalizer design is shown in Figure 3.6. Note that $L'/2$ inductors have been added to the ends of each transmission line. This improves the symmetry of the transmission lines and ensures that the total inductance ($3L'$) matches the total capacitance ($3C'$).

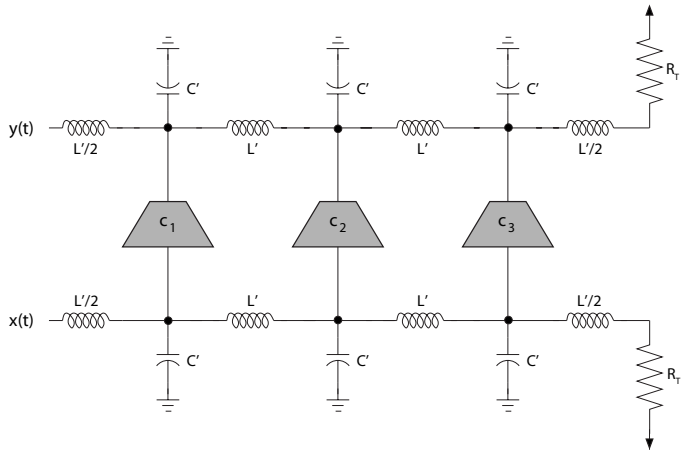


Figure 3.6: TWF design with 3-section input and output transmission lines.

The 3-dB bandwidth of an L-C section is equal to:

$$f_{3dB} = \frac{1}{\pi\sqrt{L'C'}} = \frac{1}{\pi\Delta T} \tag{3.8}$$

For a TWF, the delay of each section, ΔT, is equal to one half the tap spacing, or $\frac{\tau}{2}$. Thus, there is an inverse relationship between the bandwidth and the tap spacing of a TWF, as given by:

$$f_{3dB} = \frac{2}{\pi\tau} \tag{3.9}$$

For our example above, (3.9) yields a bandwidth of 25 GHz. This is insufficient for a 40-Gb/s equalizer. To extend the bandwidth, the L-C stages must be made smaller, or the transmission line must be made less "lumpy". Figure 3.7 shows an equalizer which is half as lumpy as the equalizer shown in Figure 3.6. The bandwidth of each transmission line section is doubled to 50 GHz, using (3.8). Plots of the magnitude response and group delay for 3- and 6-section lumped transmission lines are given in Figure 3.8. These plots demonstrate the doubling of the bandwidth corresponding to a reduction of the lumpiness by a factor of two. From the group delay plots it is also observed that the group delay is flat only within the bandwidth of the transmission

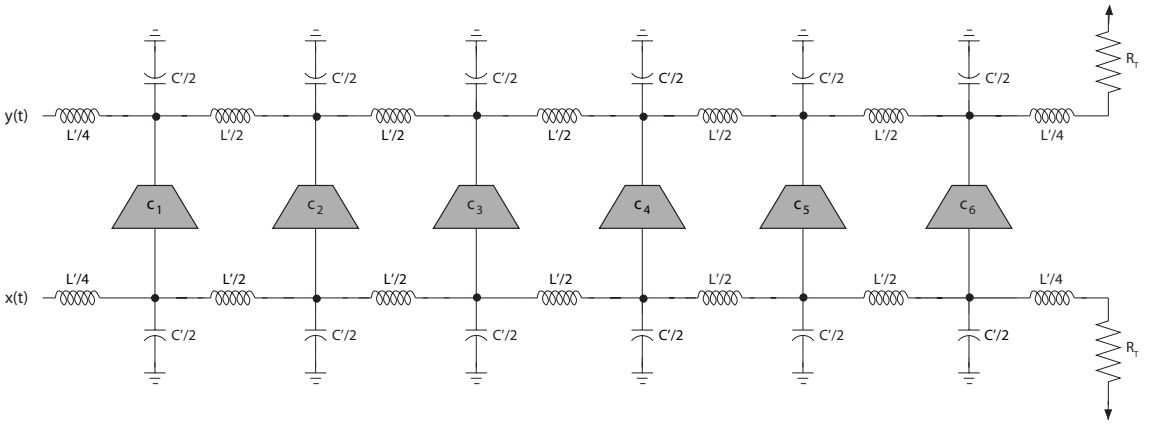
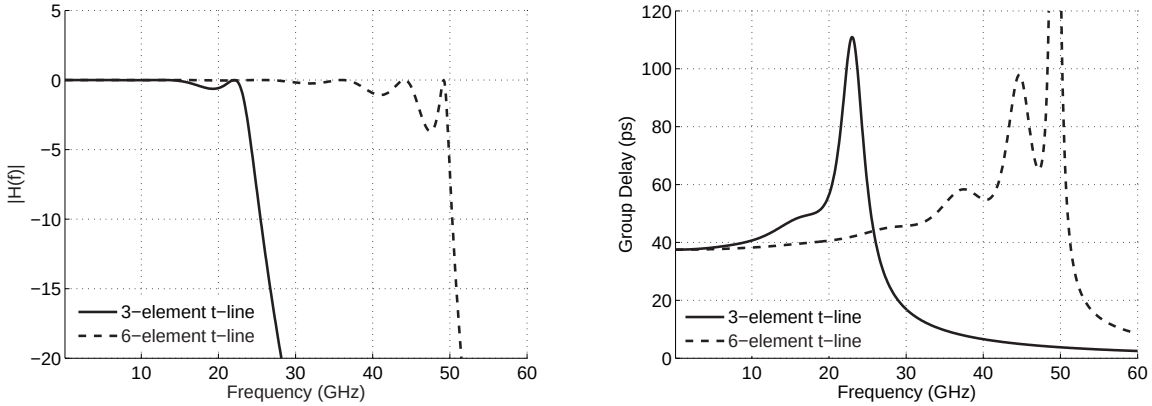


Figure 3.7: TWF design with 6-section input and output transmission lines.



a) b)

Figure 3.8: Comparison between 3- and 6-element transmission lines. a) Magnitude response. b) Group delay.

line, another important reason for making the transmission line more distributed.

Note that since the node capacitances C' are made up in part by the device capacitances, when C' is scaled the device sizes must scale accordingly. Therefore, the gain through each stage of a 6-section equalizer is only half that through each stage of a 3-section equalizer, for the same equalizer span.

3.3.2 Crossover TWF Topology

While the equalizer in Figure 3.7 does exhibit a wider bandwidth and flatter group delay response than that in Figure 3.6, it implements a 6-tap FSE instead of a 3-tap symbol-spaced equalizer. While an FSE might be desirable in some cases, splitting the three gain cells into six gain cells effectively halves the maximum possible gain through any particular tap. This limits the performance of the equalizer for operation in the absence of channel impairments, when only one tap needs to be on, for example.

To implement a symbol-spaced equalizer without increasing the lumpiness of the transmission lines, a modification to the topology is necessary. The trivial method of converting the FSE into a symbol-spaced equalizer is to replace the extra taps with appropriately sized capacitors. Replacing the extra taps with capacitors, each L-C section would have a delay ΔT equal to one quarter of the tap spacing, or $\frac{\tau}{4}$. Therefore, the bandwidth of the TWF would be given by:

$$f_{3dB} = \frac{4}{\pi\tau} \tag{3.10}$$

This represents a doubling in the bandwidth compared to that predicted by (3.9). The drawback to this solution is that the unused tap multipliers effectively result in a reduction in the tap gains.

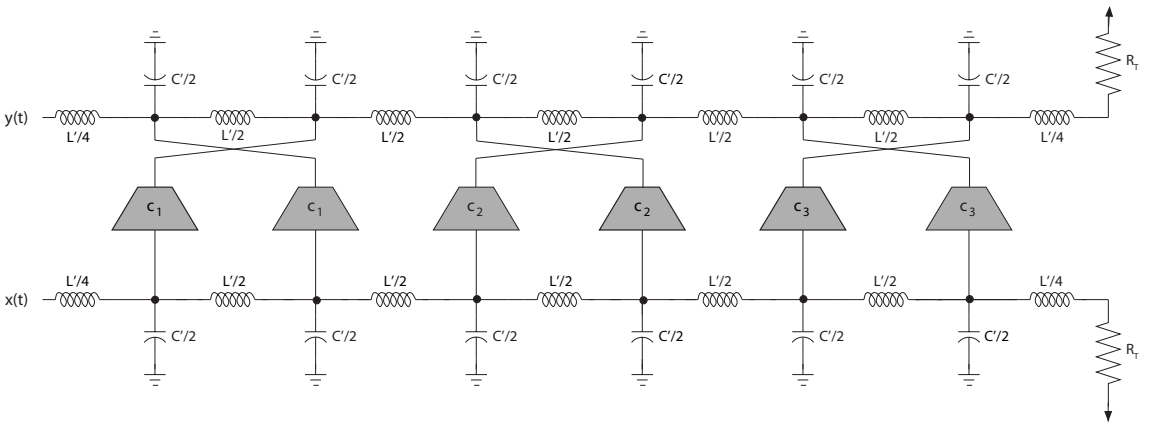


Figure 3.9: 3-tap equalizer using the crossover TWF topology.

Alternatively, a slightly modified version of the TWF topology, which will be referred to as the crossover TWF topology, can be used to allow symbol-spaced equalization without increasing the lumpiness of the transmission lines or sacrificing any gain. The crossover TWF topology is illustrated in Figure 3.9. It is simple to verify that this topology implements a 3-tap symbol-spaced equalizer. Since this topology uses 6-section transmission lines, it has a bandwidth given by (3.10), which is twice the bandwidth of the 3-tap symbol-spaced equalizer described by Figure 3.6.

3.3.3 Folded-Cascade TWF Topology

The crossover TWF topology introduced in Section 3.3.2 allows the implementation of a symbol-spaced equalizer as a TWF while decreasing the lumpiness of the transmission lines by a factor of two. It is not practical, however, to decrease the lumpiness of the transmission lines by a factor greater than two using the crossover TWF topology. The crossover routing between two taps cannot easily be reproduced for three or more taps without introducing asymmetries and skew between the different paths.

The following topology allows a reduction in the lumpiness of the transmission line by an arbitrary amount while allowing any tap spacing desired. This topology

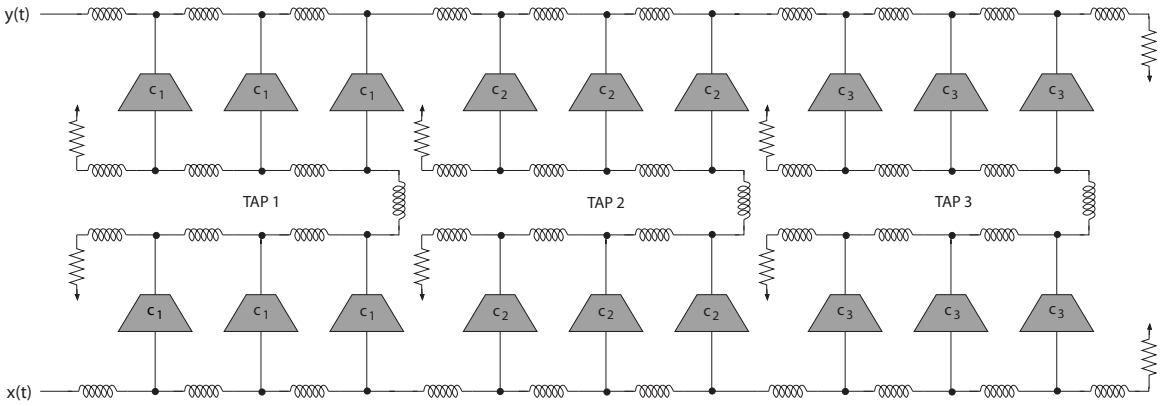


Figure 3.10: 3-tap equalizer using the folded-cascade TWF topology.

will be referred to as the folded-cascade TWF topology, and is shown in Figure 3.10. The equalizer in Figure 3.10 is a 3-tap equalizer for which the lumpiness of the input and output transmission lines has been reduced by a factor of three. Each tap is essentially a cascade of two distributed amplifiers. It is easily verified that the total delay through any particular tap is the same regardless of the path taken. If each tap of a symbol-spaced folded-cascade TWF is composed of two cascaded stages of M gain elements each, the bandwidth of the equalizer is given by:

$$f_{3dB} = \frac{2M}{\pi\tau} \tag{3.11}$$

For all TWF topologies, the maximum gain per tap for a given tap spacing and process technology is effectively fixed. The capacitance per node is fixed by the tap spacing, according to (3.7), and the gain is proportional to the size of the amplification devices, which is proportional to the capacitance of those devices. Aside from optimization of biasing, the only way to increase the gain per tap is to use a more advanced technology, for which higher gain is possible with the same capacitance. For a general TWF design, the bandwidth is also fixed by the tap spacing. The benefit

of the the folded-cascade TWF is that its bandwidth can be set arbitrarily by choosing an appropriate level of distribution for the transmission lines. The bandwidth is limited only by the number of segments that the transmission line can practically be distributed into.

This topology is not without certain drawbacks. First, because it requires two cascaded stages per tap, the power requirement is basically doubled. Also, distributed amplifiers generally have more group delay variation than lumped amplifiers, and cascading them increases this variation. Careful design is required to ensure that the group delay performance is acceptable.

3.4 Conclusions

In this section, topics pertaining to the design of a high-speed equalizer have been discussed. The analog equalizer has been shown to possess power and area advantages over the digital equalizer at high speeds. The TWF topology has been shown to be superior to the TF topology for high-speed design and the major TWF design considerations have been described. Finally, the crossover TWF and folded-cascade TWF topologies have been introduced as new topologies allowing the decoupling of bandwidth and tap spacing for more flexible equalizer configurations.

Chapter 4

40-Gb/s 3-tap Equalizer in 90-nm CMOS

4.1 Introduction

This chapter provides a description of a 40-Gb/s equalizer IC which has been designed for and fabricated in the TSMC 90-nm CMOS process. The equalizer has been designed to serve as the FFE component of a DFE to be used for mitigation of PMD effects in 40-Gb/s optical communication systems. It could also be used in high-speed chip-to-chip applications. The equalizer is a fully-differential 3-tap equalizer designed with a travelling-wave topology. Digital control of tap weights, gain control and tuning is provided through a serial interface.

Section 4.2 provides a description of the equalizer design. Section 4.3 describes the results of circuit simulations designed to test the suitability of the design for implementation. No measurable dice have yet been received; this is discussed in Section 4.4. Finally, conclusions are drawn in Section 4.5.

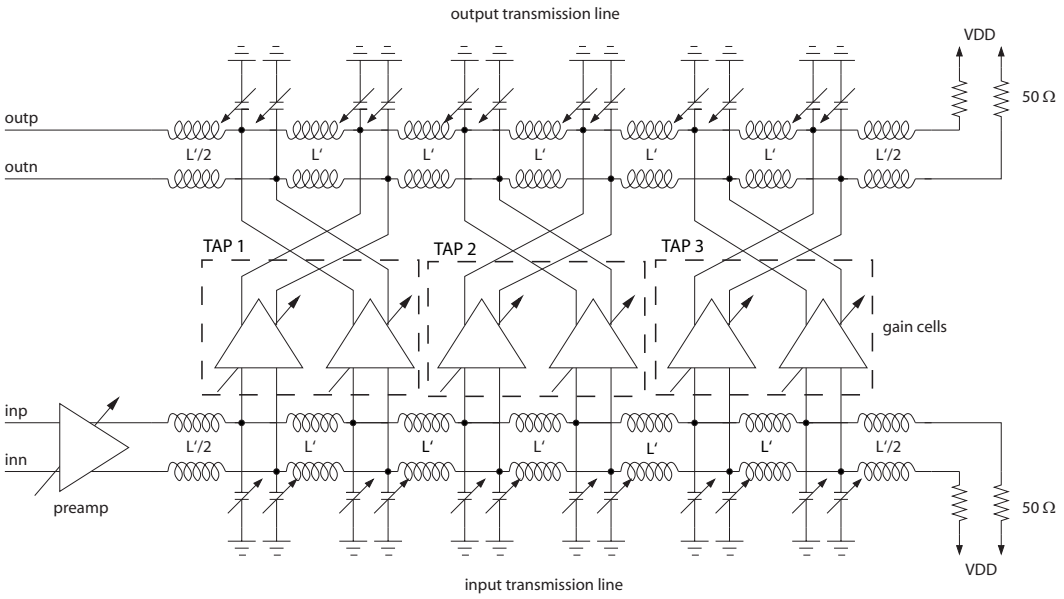


Figure 4.1: Symbolic top-level circuit schematic for 90-nm equalizer IC.

4.2 Circuit Description

This section describes the overall topology and the constituent circuit blocks of the equalizer IC design.

4.2.1 Circuit Topology

This equalizer makes use of the crossover TWF topology described in Section 3.3.2. This topology is attractive for a high-speed implementation because it makes use of distributed circuit techniques and because it lends itself to efficient layout. A fully-differential design has been chosen to improve noise immunity, and the circuit has been designed for use with a 100-Ω (differential) system impedance. The equalizer has been designed with three symbol-spaced taps based on the conclusions drawn in Section 2.6. A block diagram of the entire circuit is given in Figure 4.1.

A lumped preamplifier stage accepts differential inputs and performs a variable

gain function to condition the input signal so as to maximize the dynamic range of the equalizer. It also performs a single-ended to differential conversion function when the circuit is driven by an unbalanced input.

The preamplifier drives the differential 50-Ω input transmission line. The input and output transmission lines are made up of differential inductors and capacitances, and generate the delays necessary in an FIR filter.

Three gain cells tap this transmission line at intervals such that the difference in delay from one tap to the next is 25 ps (or one symbol period at 40 Gb/s). As described in Section 3.3.2, the cross-over present in the output of each gain cell allows implementation of a symbol-spaced equalizer with more ideal transmission lines for greater bandwidth and better phase response.

Not shown in Figure 4.1 is the digital control path. Each of the variable elements shown in Figure 4.1 is controllable through a set of registers which can be loaded serially.

4.2.2 Preamplifier

A schematic of the lumped preamplifier stage is given in Figure 4.2. The preamplifier consists of two cascaded differential pairs.

The inputs of the first differential pair are terminated into 50-Ω loads for input matching to the 100-Ω (differential) system impedance. A differential inductor is placed in series with the 50-Ω loads to partially compensate for the large input capacitance, allowing a better input match over a larger bandwidth. The first differential pair is loaded with 100-Ω resistors, which allow it to provide reasonable gain. Another differential inductor is used in series with the 100-Ω resistors to extend the bandwidth of the first stage to over 30 GHz.

The second differential pair acts as an open-drain line driver, driving the input

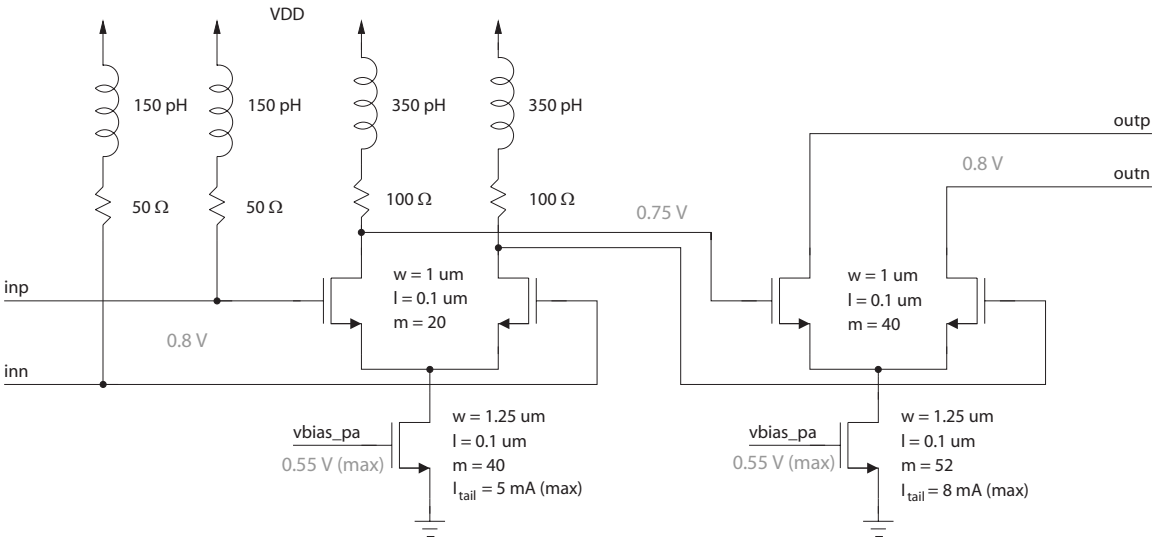


Figure 4.2: Circuit schematic of preamplifier block.

signal onto the 50-Ω input transmission lines. The open-drain configuration was chosen for several reasons. Firstly, it offers a power savings over a doubly-terminated configuration because it allows the power consumption to be halved for the same voltage gain. Secondly, since it requires a lower bias current, the transistors in both stages can be made smaller, making it easier for the first stage to achieve high bandwidth and a good input match. Thirdly, since the devices have very short channel lengths, the output resistance of the differential pair is on the order of a few hundred ohms, such that partial matching is achieved at this node without any termination. Finally, any energy travelling back to the preamplifier along the transmission line would be attenuated somewhat by the lossy nature of the transmission lines, reducing the magnitude of the reflections resulting from the open-drain configuration. These considerations, supported by simulations, led to the choice of the open-drain configuration. However, at such high speeds the validity of this choice can only be verified through measurement.

The gain of the preamplifier stage is digitally-controllable. This gain control

is provided both to allow tuning of the preamplifier bias currents for performance optimization and to allow compensation for possible variations in input power. The current source of each differential pair in the preamplifier is controlled by a single digitally-controllable, switched-resistor current mirror, which is described in Section 4.2.5. The tail currents, I_{tail}, depend on the state of the 6-bit register controlling this current mirror. The differential DC gain A_v of each stage is given by:

$$A_v = -g_m R_L \tag{4.1}$$

where R_L is the total load resistance and g_m is the transconductance of the input transistors, which is given by [36]:

$$g_m = \sqrt{\mu_n C_{ox}(W/L) I_{tail}} \tag{4.2}$$

Therefore, the gain of each stage of the preamplifier stage is proportional to $\sqrt{I_{tail}}$ and since the two stages are cascaded, the gain of the entire preamplifier is proportional to I_{tail}.

I_{tail} for each of the two stages is chosen to give an output common-mode level of 0.75 - 0.8 V. The transistors are sized as near to peak f_T current density as is possible for the limited supply voltage. For this case this corresponds to roughly one half of peak f_T current density.

The threshold voltage for the transistors V_{THn} is approximately 0.35 V. The common-mode voltages are shown in Figure 4.2. The bias levels were chosen to keep all transistors in saturation while allowing differential signal swings of up to 400 mV_{p-p}.

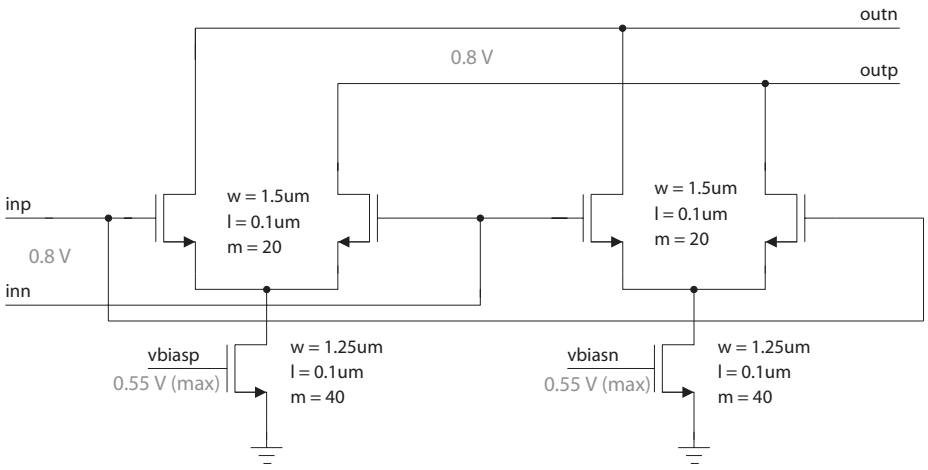


Figure 4.3: Circuit schematic of variable gain cell.

4.2.3 Gain Cell

A schematic of the gain cell is given in Figure 4.3. Two of the gain cells shown in Figure 4.3 are combined using the cross-over technique to implement a single tap of the filter.

Each of the gain cells is composed of two differential pairs. The two differential pairs are connected with opposite polarity. This allows the filter to implement both positive and negative tap weights. To implement a positive tap weight, the bias current for the differential pair connected with negative polarity is first zeroed, leaving only the positive path from input to output. The gain in this positive path is controlled by adjusting the bias current of the differential pair connected with positive polarity. A negative tap weight is implemented using the converse of this procedure. The tap weights are controlled in the same manner as the gain is controlled in the preamplifier, which was described in Section 4.2.2.

The size of these transistors has been chosen such that a balance is reached between the competing objectives of maximum gain and maximum tuning ability. The capacitance at each node is fixed by (3.7), and is made up of the device capacitances,

parasitic capacitances and a variable capacitance which is added to the node to allow tuning of characteristic impedance and delay. For large gain, the transistors should make up a large portion of the node capacitance. However, the varactors should also be made large to maximize the tuning ability. For this circuit, an appropriate balance between gain and tuning range is achieved by sizing the transistors such that they provide approximately 65% of the total node capacitance, with the remainder provided by the varactors.

The maximum current that can be drawn by all three taps is limited to 8 mA by the requirement that the output common-mode voltage must not drop below approximately 0.8 V. Therefore, the current through any particular gain cell can range from 0 when the tap is off to 4 mA, when the tap is fully on (two gain cells drawing 4 mA each).

4.2.4 Input and Output Transmission Lines

The differential input and output transmission lines generate the delays necessary in an FIR filter. As described in Section 3.3.1, transmission lines can be approximated with lumped inductors and capacitors to minimize circuit area and reduce series losses.

For this design, a 6-element transmission line is used. While a 3-element transmission line would be a more obvious choice for a 3-tap filter, it was shown in Section 3.3.1 that a 3-element transmission line with a delay of 12.5 ps per element has only a 25 GHz bandwidth, which is insufficient for a 40-Gb/s circuit. Conversely, a 6-element transmission line with a delay of 6.25 ps per element has a bandwidth of 50 GHz. Therefore, the three taps have been distributed into a total of six gain cells, and the cross-over technique described in Section 3.3.2 has been used to convert the circuit so that it can be implemented using a 6-element transmission line.

From (3.6), the inductance per element (L') required for these transmission lines is 312.5 pH per side. From (3.7), the capacitance per element (C') is 125 fF per side.

The transmission lines contain six nodes, one for each gain cell. The capacitance at each of these nodes is C'. Between these six nodes are five inductances of L' each. Inductances of $\frac{L'}{2}$ are added to each end of the transmission line so that the total inductance of the line is $6L'$, which matches the total capacitance of $6C'$.

The inductances L' are implemented by differential spiral inductors. The capacitances C' at each node are composed of the device capacitances attached to the node supplemented by a variable capacitance created by a digitally-controlled varactor. The varactor allows tuning of C' to compensate for model inaccuracies and process variation. The characteristic impedance and delay can both be tuned by this varactor.

Differential Inductor Design

A total of four different differential inductors are used in this design. Two are used for input matching and bandwidth extension in the preamplifier, and two are used for implementing the transmission lines.

In each of these inductor designs, the differential nature of the signal has been used to reduce the circuit area required for implementation. In general, to increase the inductance of a planar inductor, its length and therefore its area must be increased. When inductors are needed for two separate paths, they must be placed relatively far apart to reduce the cross-coupling of energy from one spiral to the other. However, when two spirals are properly interwound, and driven by a differential signal, the mutual inductance from one spiral to the other increases the effective inductance of each path. This allows the two spirals to be co-located, and their lengths decreased by an amount proportional to the mutual inductance. This offers a large area savings over the use of two, isolated spirals.

Each of the inductors was designed using the ASITIC inductor modelling software. Custom layouts were generated and the simulated 2-port parameters for each

of the inductors were calculated. The inductors were then modelled in SPICE using π-models. The parameters for these models were found by fitting the network parameters of the model to the network parameters generated by ASITIC.

Inductor models and plots of modelled and simulated inductance and quality factor are given in Appendix A.

Digital Varactor Design

Digitally-controllable varactors are added to each of the nodes in the lumped transmission line to allow tuning of the characteristic impedance and delay. These varactors are composed of switched native metal-insulator-metal (MiM) capacitors. These capacitors are built using the top four metal layers of the IC process. On each layer, two interdigitated structures form the two capacitor plates. Between each consecutive layer, the orientation of the two plates is reversed. This capacitor achieves high capacitance per unit area because it makes use of both the horizontal capacitance between interdigitated structures, and the vertical capacitance between adjacent metallization layers [14].

The top plate of each of these MiM capacitors is connected to a node in the transmission line. The bottom plate is connected to ground through a MOS switch. When the switch is on, the bottom plate is connected to ground and the capacitance as seen by the node is the capacitance of the MiM capacitor, C_{MiM}. When the switch is off, the MOS transistor has some capacitance from its drain to ground, C_0. Thus, the capacitance seen by the node is C_{MiM} in series with C_0, which is smaller than C_{MiM} but nonzero.

Digital control of these varactors is achieved with binary weighting of these capacitors. Five bits of control are assigned to each of the input and output varactors, with each bit b_i controlling the switch for 2^i capacitors. The least significant bit (LSB), b_0, controls the switch for one varactor. The most significant bit (MSB), b_4, controls the

switch for sixteen varactors. In this manner, the total capacitance of the varactor at each node C_{var} can vary from a maximum of:

$$C_{var}^{MAX} = 31C_{MiM} \tag{4.3}$$

when all bits are high to a minimum of:

$$C_{var}^{MIN} = 31\frac{C_{MiM}C_0}{C_{MiM} + C_0} \tag{4.4}$$

when all bits are low.

The specifications for the input and output varactor designs are summarized in Table 4.1. These varactors have been designed differently because the input transmission line is connected to the gates of transistors, while the output transmission line is connected to the drains. Consequently, the contribution of the transistor capacitances to C' at the input is different than the contribution of the transistor capacitances to C' at the output. This necessitates design of each of these varactors independently.

Table 4.1: Table of specifications for digitally-controllable varactor designs. Expected C_{var} is the expected value of the variable capacitance that will be required to achieve the desired node capacitance (C') based on estimates for the transistor and parasitic capacitances attached to the node.

Varactor	C_{MiM}	C_0	C_{var}^{MAX}	C_{var}^{MIN}	Tuning Range	Expected C_{var}
Input	1.52fF	0.64fF	47fF	14fF	335%	30fF
Output	2.27fF	0.89fF	70fF	20fF	350%	55fF

4.2.5 Switched-Resistor Current Mirror

To allow digital control of the preamplifier gain and the tap weights, switched-resistor current mirrors are used to convert digital control words into bias currents. As described in Section 4.2.2, controlling the bias current allows control of the gain of a

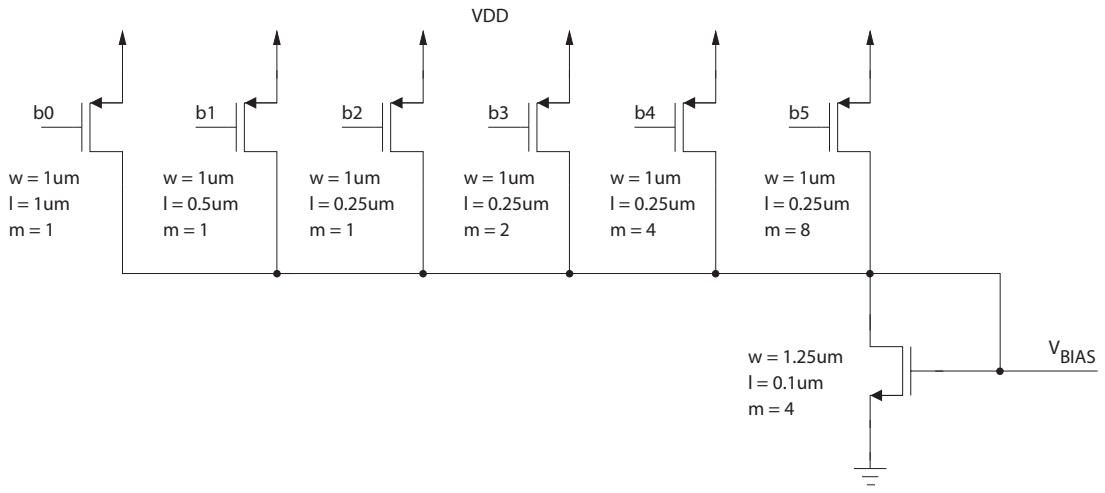


Figure 4.4: Circuit schematic of switched-resistor current mirror.

differential pair. A schematic of the switched-resistor current mirror is given in Figure 4.4.

Six binary-sized PFET transistors form the load of a diode-connected NFET current source. The gate of each of these PFET transistors is driven by a digital control bit. The LSB of the digital control word, b_0, controls a PFET with width-to-length ratio $(W/L)_0$. The other bits, b_i, control PFETs with width-to-length ratios $(W/L)_i$ equal to $2^i(W/L)_0$. When the control bit is high, the corresponding PFET is in cut-off, such that no current is passed to the mirroring NFET current source. When the control bit is low, the corresponding PFET is in triode. In triode, it acts as a resistor with a value r_{ds_i} of [36]:

$$r_{ds_i} = \frac{1}{\mu_p C_{ox}(\frac{W}{L})_i(V_{DD} - V_{THp})} \tag{4.5}$$

where V_{DD} is the supply voltage and V_{THp} is the PFET threshold voltage. It can be seen from (4.5) that the resistances of the binary-sized PFETs are binary-weighted.

The current I_{mirror} that is mirrored is equal to:

$$I_{mirror} = \sum_i \frac{V_{DD} - V_{BIAS}}{r_{ds_i}} \tag{4.6}$$

where V_{BIAS} is the bias voltage output from this block as labelled in Figure 4.4. I_{mirror} is linearly related to the digital control word only if V_{BIAS} remains constant as the control word changes. This is obviously not the case, as V_{BIAS} is the control voltage that is generated, and must change with the control word to allow variation in biasing. This poor linearity is not a great concern since the block still performs the goal of allowing a wide range of possible bias currents. Also, V_{BIAS} represents the gate to source voltage of the NFET current source V_{GSn}, which is dependent on I_{mirror} as follows:

$$V_{BIAS} = V_{GSn} = \sqrt{\frac{2I_{mirror}}{\mu_n C_{ox}(\frac{W}{L})_n}} + V_{THn} \tag{4.7}$$

where $(\frac{W}{L})_n$ is the width-to-length ratio of the NFET current source, and V_{THn} is the NFET threshold voltage. The square-root relation described in (4.7) shows that V_{BIAS} is not subject to large changes as I_{mirror} changes. To ensure that there is enough precision between the bias currents corresponding to consecutive digital control words, six bits are used to control each current mirror.

4.2.6 Digital Control Path

The digital control path of the equalizer allows manipulation of the digitally-controllable varactors described in Section 4.2.4 and current mirrors described in Section 4.2.5. Each of these digitally-controllable blocks are controlled by a separate register. Two 5-bit registers control the state of the input and output varactors, respectively. Seven 6-bit registers control the state of the preamplifier and equalizer taps: one of these registers controls the preamplifier; three of these registers control the positive path

for each of the three taps; three of these registers control the negative path for each of the three taps.

These nine registers are linked together within the circuit to form a 52-bit shift register. This shift register is controlled by a data input (DIN) and a clock input (CLK). Whenever a positive edge on the CLK input is detected, the bit on DIN is read into the first bit of the shift register, and the rest of the bits are shifted towards the end. This simple interface was necessitated by the lack of chip area for probe pads. No more than two pads were available for the digital control inputs of the equalizer.

A register map describing the layout of the internal control register is provided in Appendix B.

4.2.7 Noise and Linearity Considerations

The equalizer components have not specifically designed for low-noise or highly linear operation. However, noise and linearity have been considered.

The importance of low-noise operation is reduced by the fact that the equalizer follows a low-noise TIA front-end. While the equalizer was not specifically designed for low-noise operation, the entire equalizer exhibits a noise figure of less than 10 dB to 40 GHz.

The equalizer must be linear enough to enable accurate linear equalization of the data. However, since the output of the equalizer is a binary signal which will be limited and sliced, some nonlinearity is tolerable. The linearity of the equalizer is difficult to measure since it is a programmable circuit with many potential states. Therefore, the linearity is assessed by testing the ability of the equalizer to equalize inputs with both small and large peak-to-peak amplitudes.

Table 4.2: Definitions for nominal and worst-case conditions used in circuit simulations for the 90-nm equalizer design.

Condition	Temperature	V_{DD}	Process Corner	Termination Mismatch
Nominal	27 °C	1.0 V	Typical-Typical	0% (R_{term} = 50 Ω)
Worst-case	100 °C	0.9 V	Slow-Slow	20% (R_{term} = 40 Ω)

4.2.8 Circuit Layout

Die photos of the circuit layout are given in Figure 4.5. Labels are included on the second photo to identify the pad layout and the major circuit blocks. The overall dimensions of the equalizer IC are 600 μm x 500 μm.

4.3 Circuit Simulations

The equalizer design was simulated using Spectre to verify its performance. Circuit simulations were performed in two steps. First, the equalizer was simulated to obtain its S-parameter measurements. S-parameters were used to characterize the power gain and group delay through each of the equalizer taps, as well as the input and output matching. Time-domain simulations were then performed to verify the ability of the equalizer to equalize 40-Gb/s data streams corrupted by various PMD conditions.

Each of the simulations were performed for both nominal and worst-case conditions. The nominal and worst-case conditions are defined in Table 4.2. Worst-case corresponds to the case yielding the minimum gain performance. Note that the tap weight, preamplifier and varactor settings were optimized only once (for the nominal case) and used for all simulations. Therefore, because no tuning is performed for the worst-case simulations, the results of those simulations may be somewhat pessimistic.

The simulation testbench used for both the S-parameter and time-domain simulations is described in Appendix C.

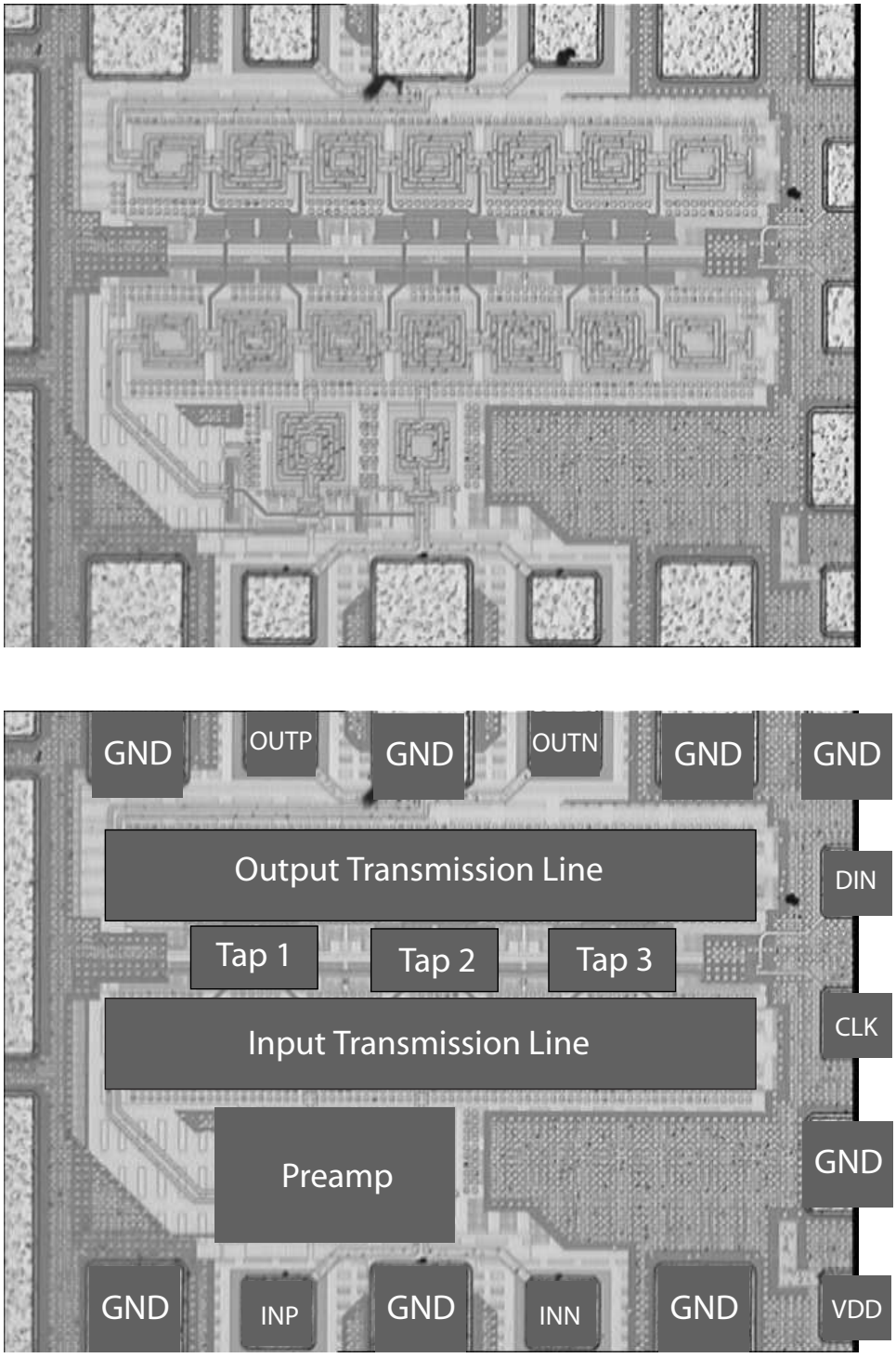


Figure 4.5: Die photos of 90-nm equalizer without and with labels.

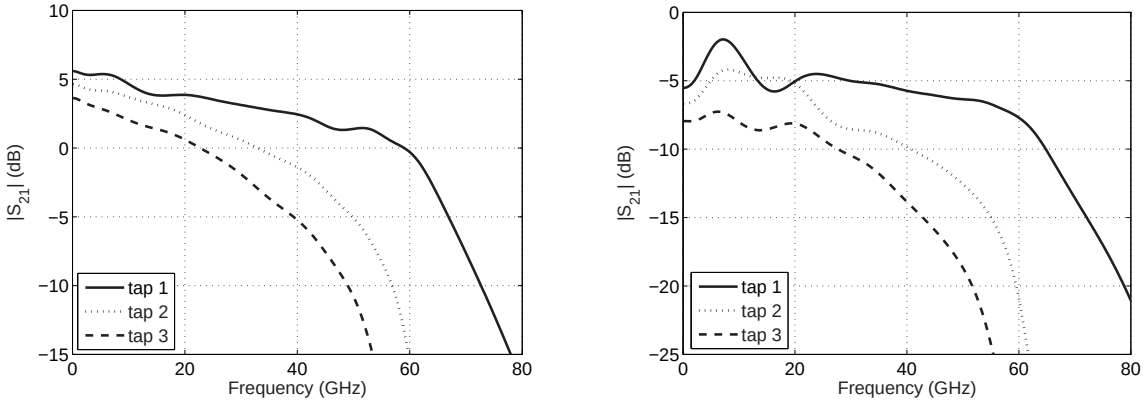


Figure 4.6: Plot of power gain through each of the three equalizer taps. a) Nominal conditions. b) Worst-case conditions.

4.3.1 S-Parameter Analysis

Plots of power gain (S_{21}) under nominal and worst-case conditions are given in Figure 4.6. The power gain through each tap was determined by setting the bias level for that tap to its maximum level and zeroing the bias level of the other two taps. Plots of group delay under nominal and worst-case conditions are given in Figure 4.7. Once again, the group delay through a particular tap was determined by turning on that tap and zeroing the other two taps.

Plots of input and output matching (S_{11} and S_{22}) under nominal and worst-case conditions are given in Figure 4.8.

S-Parameter Conclusions

The results of the S-parameter simulations are summarized in Table 4.3. These results demonstrate that the equalizer taps have sufficient bandwidth for 40-Gb/s operation and implement the desired tap spacing. They also demonstrate that the equalizer exhibits broadband input and output matching.

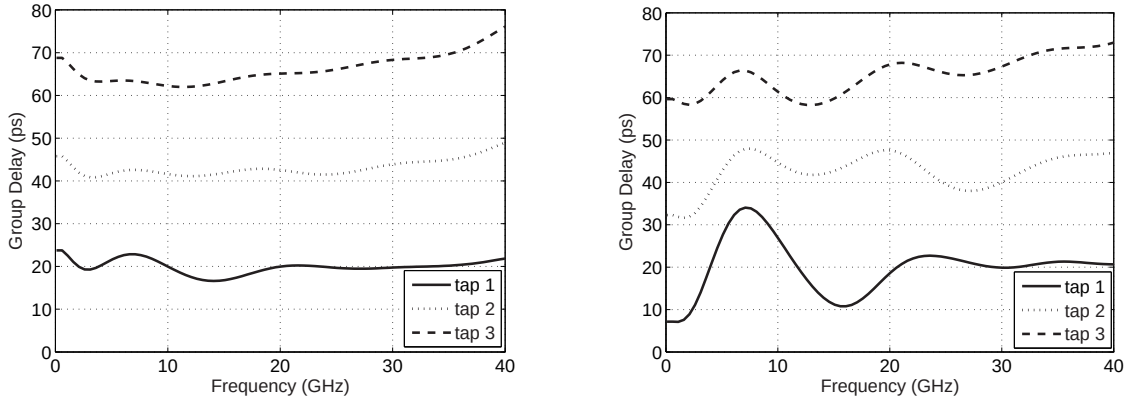


Figure 4.7: Plot of group delay through each of the three equalizer taps. a) Nominal conditions. b) Worst-case conditions.

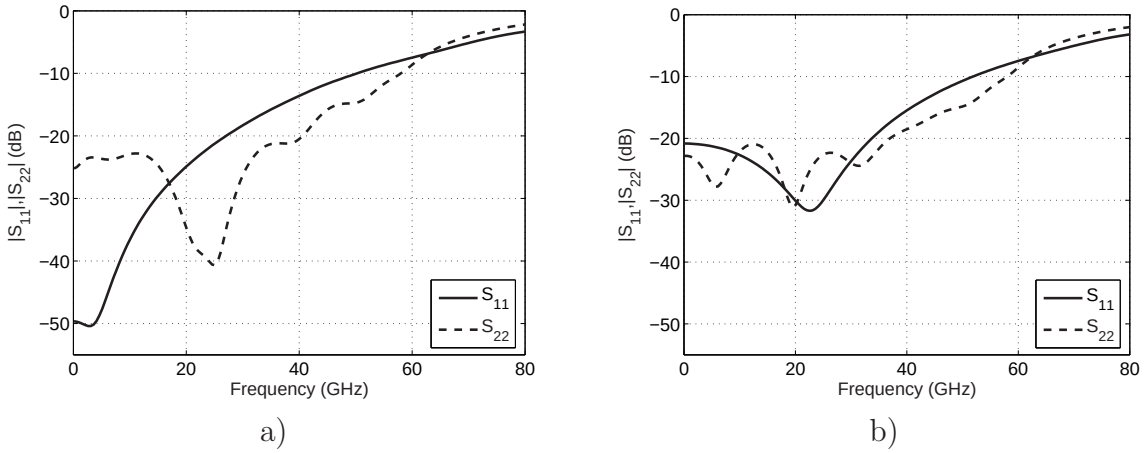


Figure 4.8: Input and output matching. a) Nominal conditions. b) Worst-case conditions.

4.3.2 Time-Domain Analysis

For the time-domain simulations, an input data stream was corrupted by PMD with various characteristics and applied to the equalizer. Equalizer tap weights were optimized manually. Figures 4.9 - 4.12 compare the eye diagrams of the data stream before and after equalization.

Time-domain Conclusions

These eye diagram plots imply that this equalizer design should perform well as a PMD compensator in a 40-Gb/s system. Figures 4.9 and 4.10 demonstrate that the equalizer is able to compensate for PMD with large and small γ values. Figure 4.11 shows that the equalizer has sufficient linearity to enable effective equalization even for large input signals. Finally, Figure 4.12 demonstrates the ability of the equalizer to compensate PMD with DGD that is not a multiple of the tap spacing.

4.3.3 Power Consumption

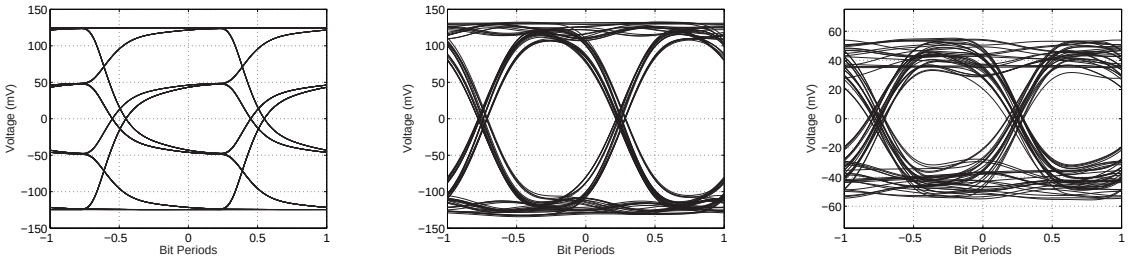
The power requirements of the equalizer are summarized in Table 4.4. The equalizer consumes approximately 23 mW from a 1-V supply. This is significantly lower than both of the 40-Gb/s FFEs reported (820 mW [11] and 750 mW [12]) and nearly all of the 10-Gb/s FFEs reported.

4.4 Measurement Results

The equalizer design was taped out in October 2003. Problems with certain processing steps have delayed receipt of a measurable die. A measurement test plan which mirrors the simulations has been formulated and will be carried out as soon as a die is received. The test setup and measurement objectives are given in Appendix C.

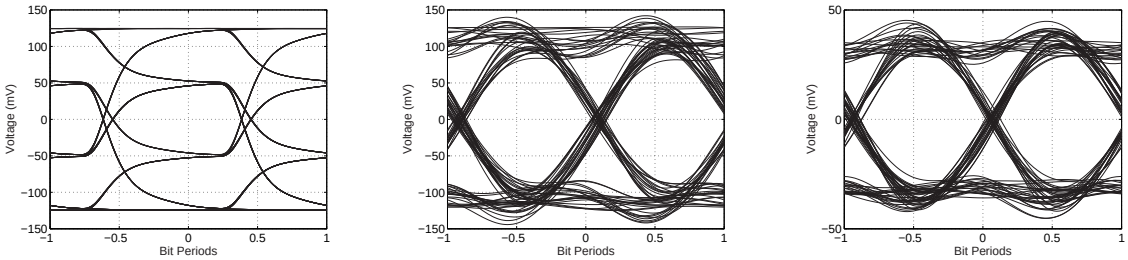
Table 4.3: Summary of S-parameter circuit simulations for the 90-nm equalizer design. Worst-case results are in parentheses.

Tap Characterization				
Tap #	Gain (dB)	Bandwidth (GHz)	Ripple (dB)	Group Delay (ps)
1	5.6 (-5.5)	38 (40)	0.05 (3)	20 (20)
2	4.6 (-6.7)	24 (24)	0 (2.5)	43 (42)
3	3.6 (-8.0)	20 (30)	0 (0.8)	67 (65)
Input/Output Matching				
S_{11}	better than -14 dB (-15 dB) up to 40 GHz			
S_{22}	better than -20 dB (-19 dB) up to 40 GHz			



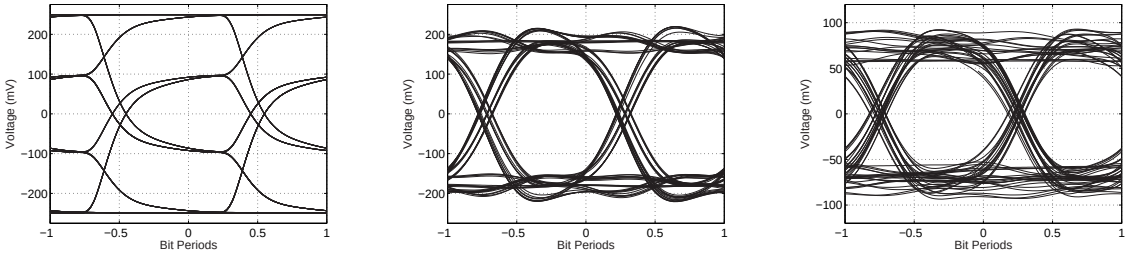
a) b) c)

Figure 4.9: Eye diagrams for PMD channel with $\gamma = 0.7$, $\Delta\tau = 25$ ps, $v_{\text{in}} = 250$ mV$_{p-p}$. a) Before equalization. b) After equalization (nominal conditions). c) After equalization (worst-case conditions).



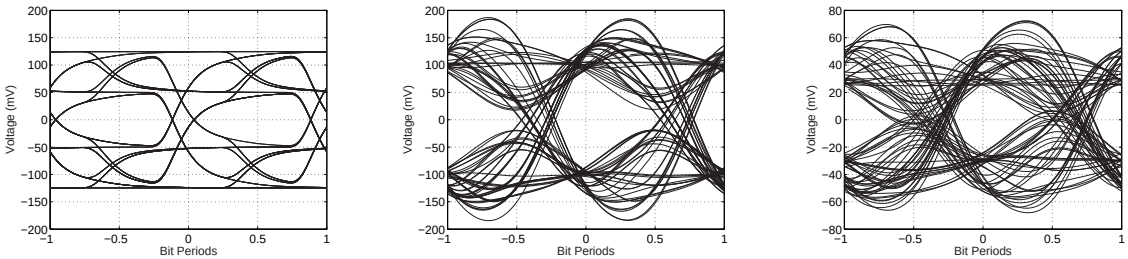
a) b) c)

Figure 4.10: Eye diagrams for PMD channel with $\gamma = 0.3$, $\Delta\tau = 25$ ps, $v_{\text{in}} = 250$ mV$_{p-p}$. a) Before equalization. b) After equalization (nominal conditions). c) After equalization (worst-case conditions).



a) b) c)

Figure 4.11: Eye diagrams for PMD channel with $\gamma = 0.7$, $\Delta\tau = 25$ ps, $v_{\text{in}} = 500$ mV$_{p-p}$. a) Before equalization. b) After equalization (nominal conditions). c) After equalization (worst-case conditions).



a) b) c)

Figure 4.12: Eye diagrams for PMD channel with $\gamma = 0.3$, $\Delta\tau = 37.5$ ps, $v_{\text{in}} = 250$ mV$_{p-p}$. a) Before equalization. b) After equalization (nominal conditions). c) After equalization (worst-case conditions).

Table 4.4: Summary of simulated power requirements for 90-nm equalizer IC.

Component	Power Consumption
Preamplifier	13 mW
Gain Cells	8 mW
Biasing	2 mW
Total	23 mW

4.5 Conclusion

In this chapter, a 40-Gb/s 3-tap equalizer has been described. The equalizer is fully-differential and digitally-controllable. The design of this equalizer has been documented with schematics and descriptions of design methodology. Simulation results have been provided which demonstrate the potential ability of the circuit to equalize 40-Gb/s data streams corrupted with PMD while consuming much less power than comparable implementations. This equalizer has been fabricated in the TSMC 90-nm CMOS IC process. Circuit measurements await receipt of fabricated dice.

Chapter 5

40-Gb/s 3-tap Equalizer in 0.18-μm CMOS

5.1 Introduction

This section describes a 40-Gb/s equalizer which has been designed for and fabricated in the TSMC 0.18-μm CMOS process. It is a fully-differential, 3-tap equalizer designed with the folded-cascade TWF topology. The equalizer has been designed to perform the function of an FFE in a high-speed optical or chip-to-chip communications system, and to test the suitability of the folded-cascade TWF topology.

Section 5.2 provides a description of the equalizer design. Section 5.3 outlines the performance of the equalizer as determined through simulations. Section 5.4 describes circuit measurement results and conclusions are drawn in Section 5.5.

5.2 Circuit Description

5.2.1 Circuit Topology

The topology used for this equalizer IC is the folded-cascade TWF topology introduced in Section 3.3.3. This equalizer has been designed in part to test the suitability of this circuit architecture. The main benefit of this architecture is that it allows the level of distribution of the transmission lines to be chosen independently of the number of equalizer taps. A block diagram of the equalizer topology is given in Figure 5.1. As described in Section 3.3.3 each tap is composed of a cascade of two DAs. It can be verified that the delay through a particular tap is identical regardless of the path taken from input to output. This equalizer does not have a lumped preamplifier stage because lumped circuits in the 0.18-μm technology do not have sufficient bandwidth for 40-Gb/s operation.

The supply voltage used for the equalizer is 1.8 V. Three analog control voltages control the gain for each of the taps. A fourth control voltage controls the common-mode voltage of the far end of the input transmission line, as shown in Figure 5.1. By setting this voltage to be equal to the input common-mode voltage, no DC current flows through the input transmission line, resulting in more constant bias voltages along the length of the transmission line.

5.2.2 Gain Cell

The gain cell used in this equalizer is a differential pair, as shown in Figure 5.2. Six of these differential pairs make up each of the three equalizer taps. Because 40-Gb/s operation is only possible in the 0.18-μm technology when distributed circuit techniques are used, more complicated structures such as cascodes were not available to this design. Cascode structures have a circuit node that is not connected to one of

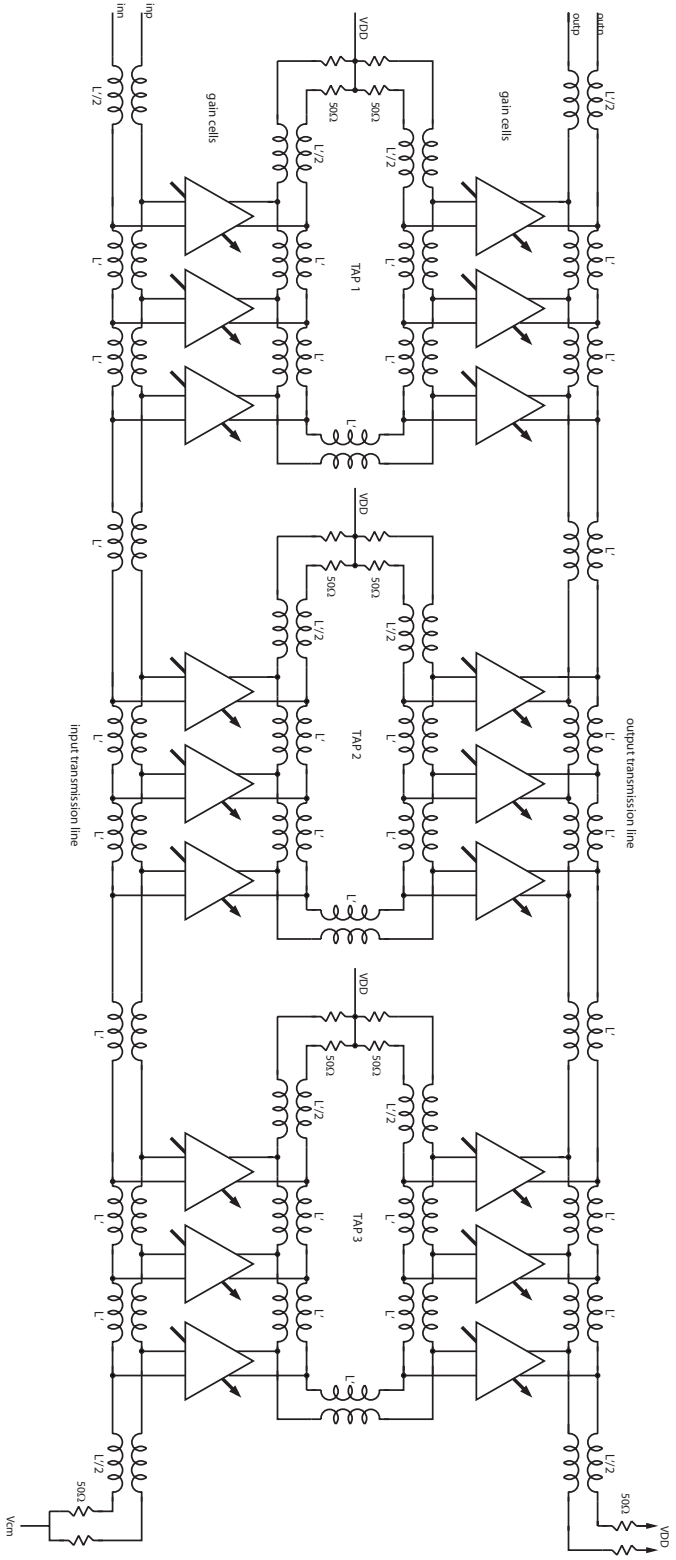


Figure 5.1: Symbolic top-level circuit schematic for 0.18-μm equalizer IC.

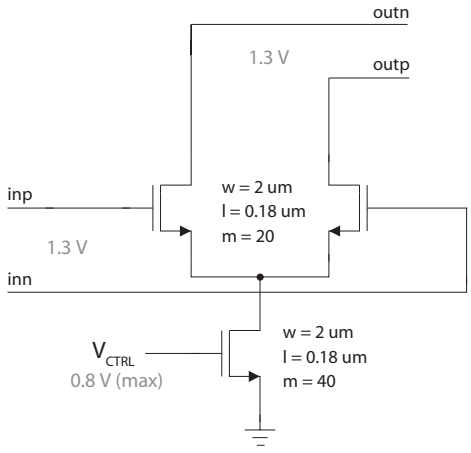


Figure 5.2: Schematic of equalizer gain cell. Six of these cells are used in each tap of the equalizer.

the transmission lines. This node would limit the speed for this application.

Each of the three taps has a fixed polarity. The first tap is positive, the second is negative, and the third is positive. These polarities correspond to a high-pass response, which would be the typical response of such an equalizer when used with most chip-to-chip or PMD channels. The polarities were fixed to maintain a reasonable level of gain through each equalizer tap. A Gilbert cell mixer for implementing signed tap weights is not possible for the reasons described in the discussion of the cascode structure above. Therefore, positive and negative tap weights would have to be implemented with two gain cells connected with opposite polarity, as described in Section 4.2.3. Since the capacitances are fixed, the size of the gain cell must be halved, resulting in a halving of the gain. For the 0.18-μm technology this would result in maximum tap gains of approximately -2 dB. When tested single-endedly, a further decrease of 6 dB in tap gain is experienced, to -8 dB. Fixing the polarities allows a 6 dB increase in the maximum tap gains, to nearly 4 dB (-2 dB single-endedly). This increased tap gain will simplify the measurement of the equalizer and the verification of the folded-cascade TWF topology.

The size of the gain cells was chosen such that the device capacitances, when added to the inductor parasitic capacitances, make up the transmission line capacitances, C'. No variable capacitance was added for tuning so that the maximum possible gain could be achieved. To achieve the same gain per tap in the 0.18-μm technology as was achieved in the 90-nm technology, the device capacitances must make up a much larger percentage of the node capacitance C'.

The gain of each of the gain cells is controlled by an analog control voltage (V_{CTRL}) that is provided off-chip. There are three control voltages, one for each tap. The control voltage for a given tap is connected to the gates of the current source transistors of each of the six differential pairs making up the tap. By varying V_{CTRL}, the currents through the differential pairs are varied, allowing control of the gain, as described in Section 4.2.2.

The maximum total current through the output stage of all three taps combined is limited to 20 mA. This is due to the restriction that the output common-mode voltage must not drop any lower than approximately 1.3 V for all transistors to remain in saturation while allowing differential signal swings in excess of 1 V_{p-p}.

5.2.3 Transmission Lines

A total of five lumped differential transmission lines are used in the design of this equalizer: one at the input, one at the output, and one internal to each of the three taps.

The values for the inductance L' and capacitance C' of each transmission line section are determined using (3.6) and (3.7), respectively. These equations require specification of the characteristic impedance Z_0 and delay τ. The characteristic impedance is 50 Ω. The delay τ of each transmission line section can be determined by referring to Figure 5.1. The input-to-output delay through tap 1 is equal to the delay of six sections, or 6τ. The input-to-output delay through tap 2 is equal to 12τ. The desired

inter-tap spacing is 25 ps (one bit period at 40 Gb/s). Therefore, τ is equal to one sixth of a bit period, or 4.17 ps. The resulting values of L' and C' are 208.5 pH and 83.4 fF, respectively.

The input transmission line is designed to have a characteristic impedance of 50 Ω per side for matching to a 100-Ω (differential) system impedance. The inductors composing each path of this differential transmission line are isolated as much as possible from one another, such that the coupling between the two paths is minimized. This is done in anticipation of single-ended stimulation of this circuit, which is necessary due to testing considerations. If strongly coupled differential inductors were used to implement this input transmission line, the single-ended characteristic impedance would be less than 50 Ω. This would result in poor input matching for unbalanced inputs. Using a separate, isolated inductor for each path ensures that each path sees a characteristic impedance of 50 Ω for both unbalanced and balanced stimuli.

The other four transmission lines are made up of differential inductors which minimize both area and series loss. Differential inductors can be used for these lines even if the input is driven single-endedly because each of these lines is driven by at least one stage of differential pairs, which convert the unbalanced input into a balanced output.

The inductors were again designed using the ASITIC modelling software. The layouts, models and characterizations of these inductors are given in Appendix A.

For this design, unlike the 90-nm equalizer design, no capacitors or varactors were added to the nodes of the transmission line. Because of the larger devices in the 0.18-μm technology, the device capacitances (in combination with the inductor parasitics) make up the entire node capacitance.

5.2.4 Noise and Linearity Considerations

Once again, this equalizer was not designed specifically for low-noise or highly linear operation. The discussion provided in Section 4.2.7 for the 90-nm equalizer design applies to this design as well. This equalizer exhibits a noise figure of less than 8 dB up to 40 GHz.

5.2.5 Circuit Layout

Unlabelled and labelled die photos of the circuit layout are given in Figure 5.3. The overall dimensions of the equalizer IC are 1 mm x 1 mm.

5.3 Circuit Simulations

The equalizer design was simulated using Spectre to verify its performance. Like the equalizer described in Chapter 4, both S-parameter and time-domain simulations were performed.

Each of the simulations were performed for both nominal and worst-case conditions. The nominal and worst-case conditions are defined in Table 5.1.

Table 5.1: Definitions for nominal and worst-case conditions used in circuit simulations for the 0.18-μm equalizer design.

Condition	Temperature	V_{DD}	Process Corner	Termination Mismatch
Nominal	27 °C	1.8 V	Typical-Typical	0% (R_{term} = 50 Ω)
Worst-case	100 °C	1.6 V	Slow-Slow	20% (R_{term} = 40 Ω)

The simulation testbench used for both the S-parameter and time-domain simulations is described in Appendix C.

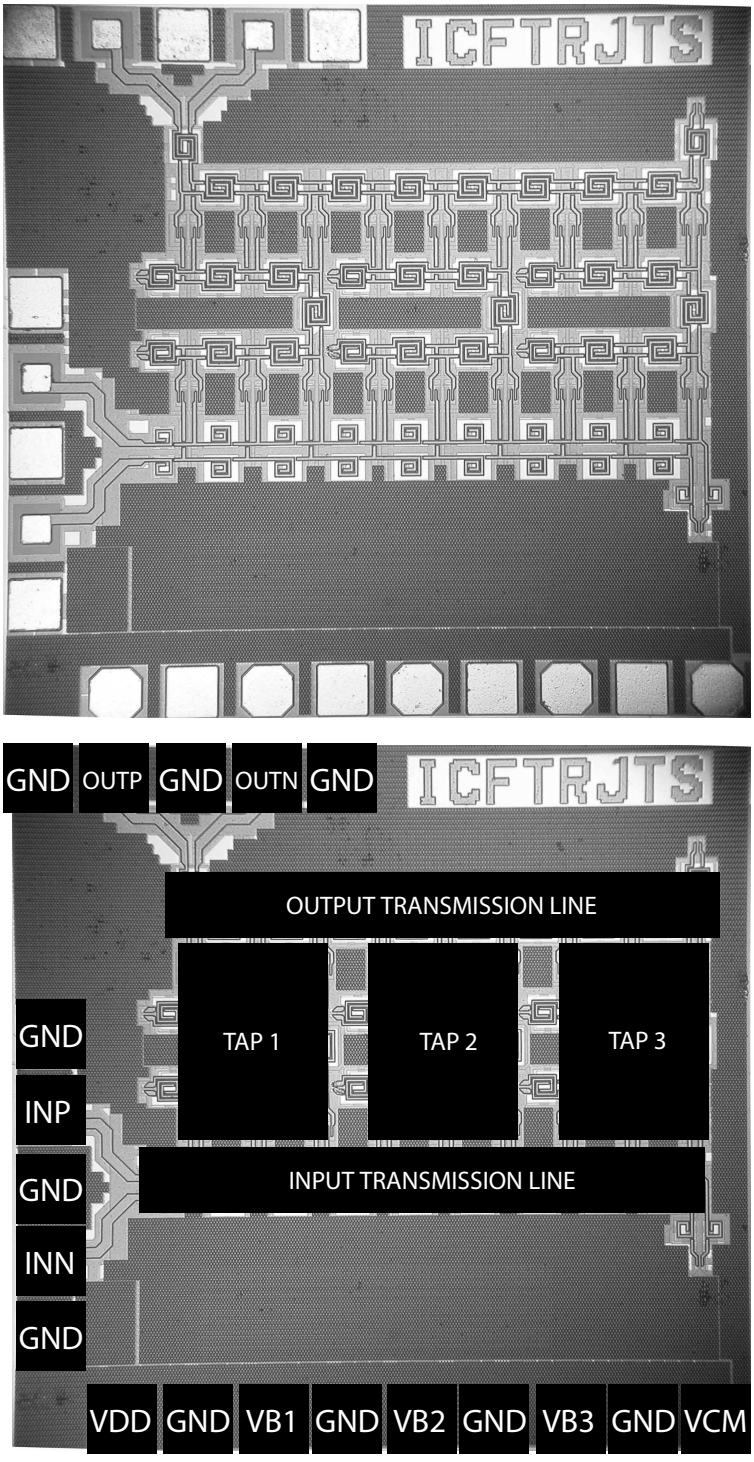


Figure 5.3: Die photos of 0.18-μm equalizer without and with labels.

5.3.1 S-parameter Analysis

Plots of power gain (S_{21}) for each tap under nominal and worst-case conditions are given in Figure 5.4. Plots of group delay under nominal and worst-case conditions are given in Figure 5.5. For both power gain and group delay simulations, only one tap was activated at any given time, with the other two taps turned off. Plots of input and output matching (S_{11} and S_{22}) under nominal and worst-case conditions are given in Figure 5.6.

S-parameter Conclusions

The results of the S-parameter simulations are summarized in Table 5.2. The first two taps have sufficient bandwidth although the first tap exhibits up to 3 dB of gain ripple. The third tap has a relatively small 3-dB bandwidth (17 GHz), although the gain rolloff is not severe, with the gain at 40 GHz only 5 dB less than at DC. While these results show that this circuit will perform the basic function of equalization, they are inconclusive in predicting the quality of its performance based on the gain ripple and bandwidth concerns.

5.3.2 Time-domain Analysis

A time-domain analysis was performed by applying a 40-Gb/s data stream corrupted by PMD with various characteristics to the equalizer. Equalizer tap weights were optimized manually. Figures 5.7 - 5.10 compare the eye diagrams of the data stream before and after equalization.

Time-domain Conclusions

These plots demonstrate that this circuit is able to effectively equalize a 40-Gb/s data stream for all PMD configurations. The ripple that was observed in the S-parameter

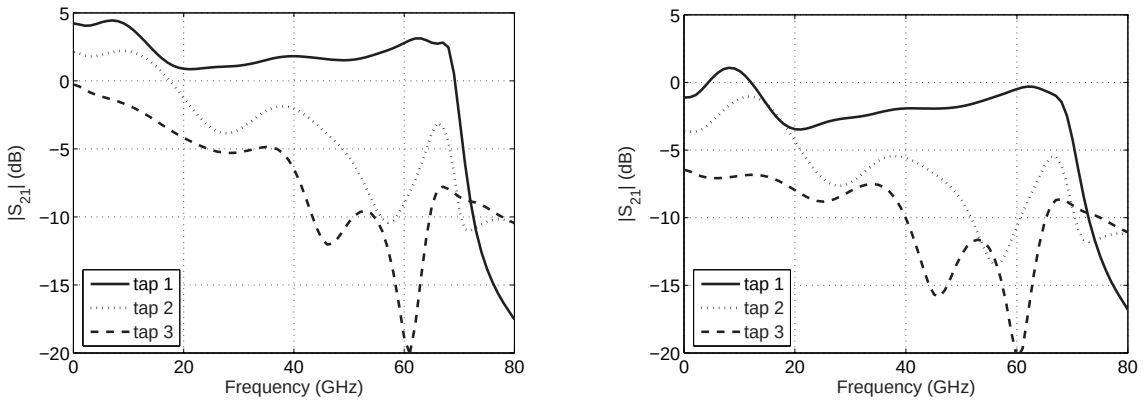


Figure 5.4: Plot of power gain through each of the three equalizer taps. a) Nominal conditions. b) Worst-case conditions.

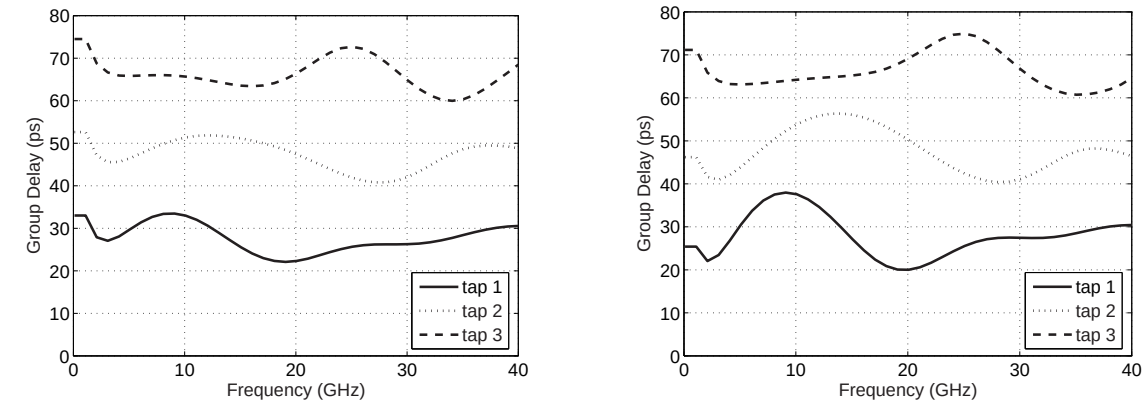


Figure 5.5: Plot of group delay through each of the three equalizer taps. a) Nominal conditions. b) Worst-case conditions.

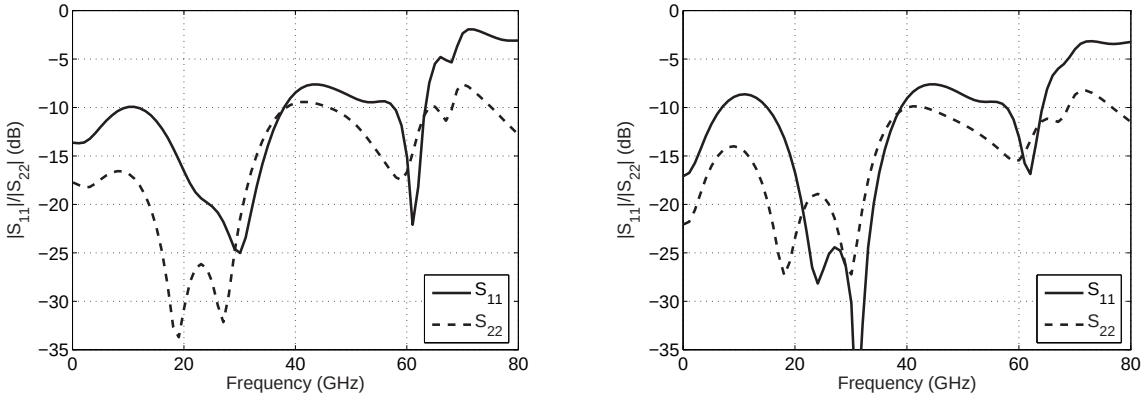
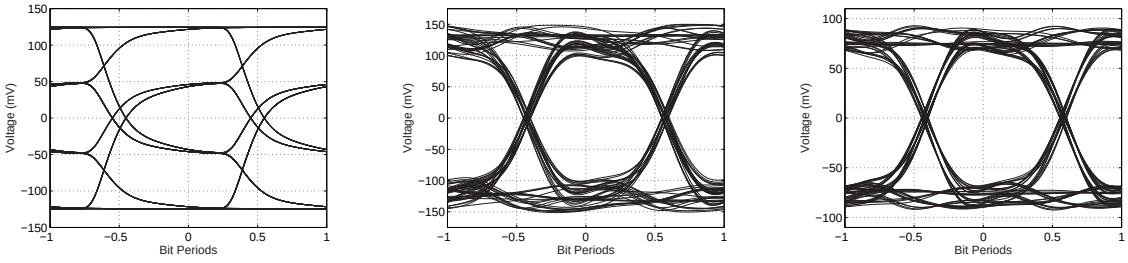


Figure 5.6: Input and output matching. a) Nominal conditions. b) Worst-case conditions.

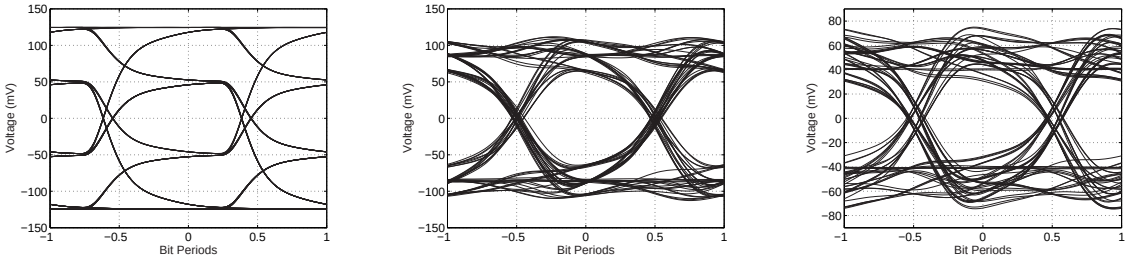
Table 5.2: Summary of S-parameter circuit simulations for the 0.18-μm equalizer design. Worst-case results are in parentheses.

Tap Characterization				
Tap #	Gain (dB)	Bandwidth (GHz)	Ripple (dB)	Group Delay (ps)
1	4.2 (-1.1)	60 (60)	3 (4)	27 (25)
2	2.1 (-3.6)	22 (24)	0.2 (2.5)	50 (50)
3	-0.3 (-6.4)	17 (40)	0 (1.2)	70 (70)
Input/Output Matching				
S_{11}	better than -8.6 dB (-8.6 dB) up to 40 GHz			
S_{22}	better than -10 dB (-9.5 dB) up to 40 GHz			



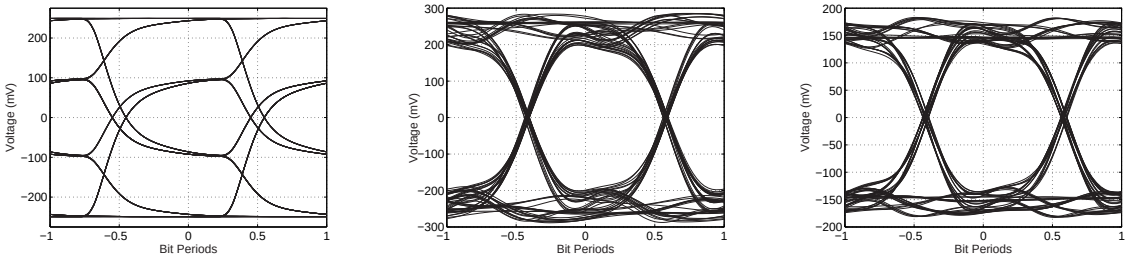
a) b) c)

Figure 5.7: Eye diagrams for PMD channel with $\gamma = 0.7$, $\Delta\tau = 25$ ps, $v_{\text{in}} = 250$ mV$_{p-p}$. a) Before equalization. b) After equalization (nominal conditions). c) After equalization (worst-case conditions).



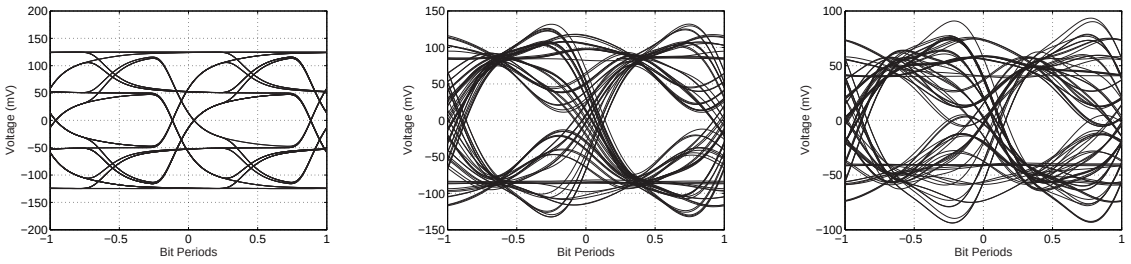
a) b) c)

Figure 5.8: Eye diagrams for PMD channel with $\gamma = 0.3$, $\Delta\tau = 25$ ps, $v_{\text{in}} = 250$ mV$_{p-p}$. a) Before equalization. b) After equalization (nominal conditions). c) After equalization (worst-case conditions).



a) b) c)

Figure 5.9: Eye diagrams for PMD channel with $\gamma = 0.7$, $\Delta\tau = 25$ ps, $v_{\text{in}} = 500$ mV$_{p-p}$. a) Before equalization. b) After equalization (nominal conditions). c) After equalization (worst-case conditions).



a) b) c)

Figure 5.10: Eye diagrams for PMD channel with $\gamma = 0.3$, $\Delta\tau = 37.5$ ps, $v_{\text{in}} = 250$ mV$_{p-p}$. a) Before equalization. b) After equalization (nominal conditions). c) After equalization (worst-case conditions).

measurements does not contribute to a degradation in equalizer performance, demonstrating the robustness of the architecture. The ability of the equalizer to handle PMD with large and small values of γ is shown by the eye diagrams in Figures 5.7 and 5.8. The linearity of the equalizer is shown by the scaled but otherwise identical responses of Figures 5.7 and 5.9 for input voltages of 250 and 500 mV$_{p-p}$, respectively. Finally, Figure 5.10 shows that the equalizer can compensate PMD with DGD that is not aligned with the tap spacing.

5.3.3 Power Consumption

The equalizer consumes approximately 72 mW from a 1.8-V supply when the maximum current is being drawn by the gain cells. This is somewhat higher than the 90-nm equalizer described in Chapter 4, but significantly lower than almost all other 10- and 40-Gb/s FFE implementations.

5.4 Circuit Measurements

The measurement setup and a brief overview of the measurement test plan for both the 90-nm and 0.18-μm equalizer designs are given in Appendix C.

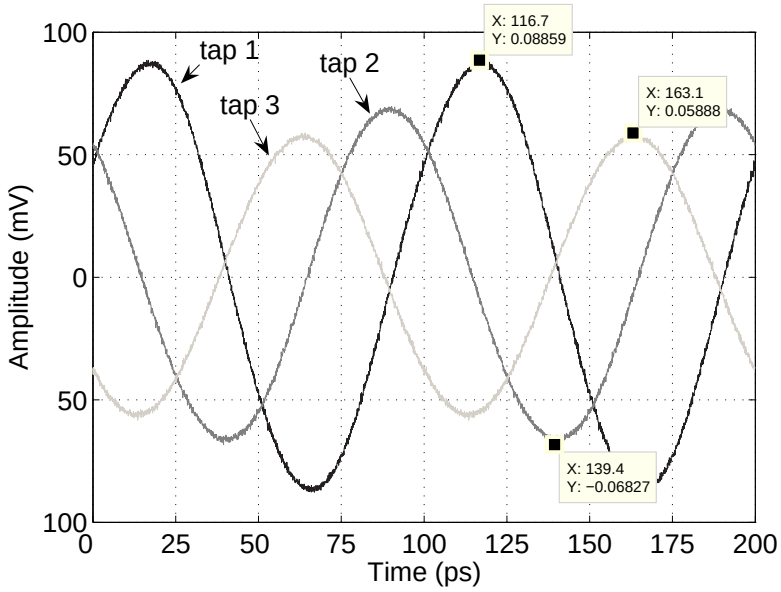


Figure 5.11: Measurement of tap delays for 0.18-μm equalizer IC using stimulation by a 10-GHz sinusoid. Each tap was measured separately and the three curves were superimposed. Note that the second tap has opposite polarity from the first and third taps.

The tap spacing of this equalizer was measured by applying a 10-GHz sinusoid to the input and measuring the output with only one of the equalizer taps activated at a given time. The sinusoid was generated using an HP 83650B Swept Signal Generator and the outputs were captured using an Agilent 86100B Oscilloscope with 86118A remote sampling modules. The resulting outputs are given in Figure 5.11. This plot demonstrates that the equalizer accurately implements the proper tap spacing. The delay between the first and second tap is 22.7 ps, while the delay between the second and third tap is 23.7 ps.

Figure 5.12 shows the normalized gain through the first tap of the equalizer versus the tap control voltage. This plot shows that the equalizer can be tuned to provide a wide range of tap gains by varying the bias voltage over a 300 mV range.

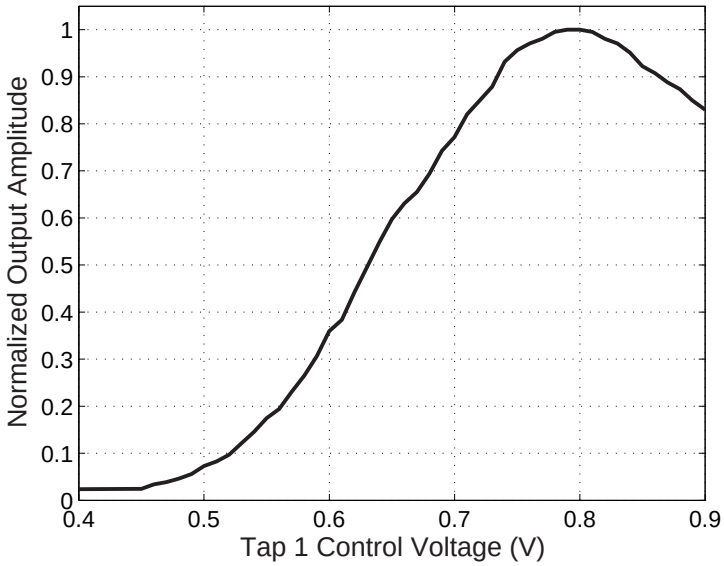


Figure 5.12: Measurement of normalized tap gain versus tap control voltage.

S-parameter measurements await the receipt of software that allows network analyzer calibration for probes that are oriented at 90° to one another. Equalization measurements on a 40-Gb/s data stream await the availability of a 40-Gb/s data source.

5.5 Conclusion

This chapter has described the design, simulation and measurement of an equalizer IC fabricated in the TSMC 0.18-μm CMOS process. This equalizer makes use of distributed circuit techniques to allow 40-Gb/s operation in a less advanced technology than is generally possible for 40-Gb/s circuits. The performance of the equalizer has been demonstrated through simulation. Circuit measurements have verified the tap spacing of the equalizer and are still ongoing.

Chapter 6

Conclusion

6.1 Summary

Electronic equalization of PMD in 40-Gb/s optical systems has been investigated through system analysis and the design of two CMOS IC equalizers.

Chapter 2 described the results of a system-level analysis of first-order PMD effects in a 40-Gb/s optical system. A DFE with a 3-tap FFE and a 1-tap FBE was identified as a potential implementation of a PMD compensator. This DFE was shown to allow an increase in the useful length of a PMD-limited optical system of more than eight times.

FFE architectures were discussed in Chapter 3. The TWF topology was shown to be superior to the TF topology. The basic design considerations for a TWF were described, including the use of artificial L-C transmission lines. Two new TWF topologies were introduced: the crossover TWF topology and the folded-cascade TWF topology. These topologies allow decoupling of tap spacing and bandwidth in TWF designs, allowing more flexibility for equalizer specification.

Chapter 4 described the design and simulation of a fully-differential, 3-tap 40-Gb/s equalizer IC in TSMC 90-nm CMOS. Chapter 5 described the design, simulation and

measurement of a fully-differential, 3-tap 40-Gb/s equalizer IC in TSMC 0.18-μm CMOS. These equalizers are designed as FFEs for incorporation into an electronic PMD compensation scheme. They consume much less power than comparable implementations in other technologies and would represent the first CMOS 40-Gb/s equalizers.

6.2 Future Work

In terms of this project, circuit measurements for both equalizer ICs must be completed. The adaptation circuitry for these equalizers was not implemented, and could be included in subsequent designs. Also, the equalizers have been designed to implement the FFE component of a DFE-based PMD compensation scheme. Implementation of an FBE and integration of the FFE and FBE into an integrated PMD compensator remain as future projects. Also remaining is the integration in CMOS of an entire receiver (TIA, PMD compensator, limiting amplifier and decision circuitry).

In more general terms, significant work remains in the field of electronic PMD compensation. While analog PMD compensation holds a temporary advantage over the DSP approach at 40-Gb/s, DSP solutions will eventually gain favour as improvements in IC technology enable the availability of high-speed ADCs. Digital PMD compensation would enable the use of maximum-likelihood sequence detection (MLSD), which has been shown to provide the best performance of any electronic scheme [29]. Analog compensation will then be applied to higher speeds.

Appendix A

Characterization of Inductors

This appendix contains layout and modelling information for each of the eight inductor designs used in the implementations of the 40-Gb/s equalizers described in Chapters 4 and 5.

A.1 Inductor Models and Layouts

The eight unique spirals used in the equalizer ICs described in Chapters 4 and 5 can be categorized into three types: single-ended inductors, three-terminal inductors and transformers. This section describes each inductor type, including circuit models and layouts.

A.1.1 Single-Ended Inductors

Single-ended inductors are the basic 2-port spirals common in high-speed and radio-frequency (RF) IC design.

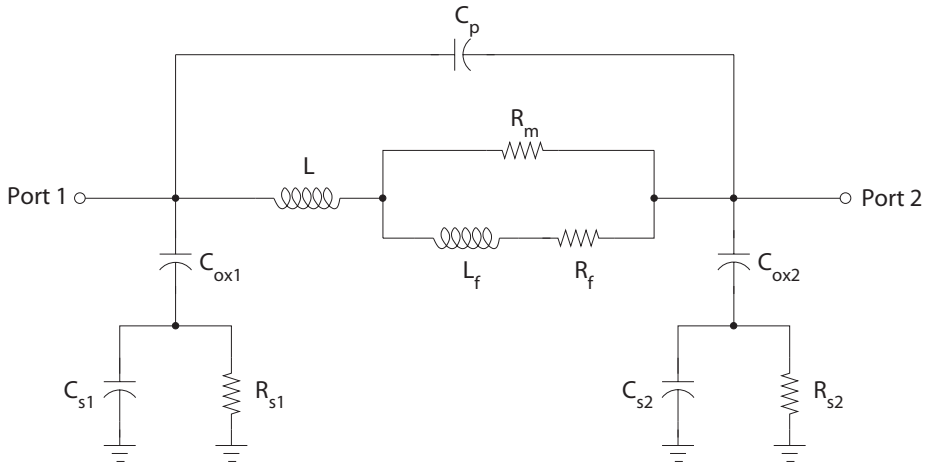


Figure A.1: Single-ended inductor circuit model.

Circuit Model

The lumped circuit model given in Figure A.1 was used to model inductors [37].

Layouts

The only single-ended inductor layout used in this project, the multi-level inductor (MLI) layout, is shown in Figure A.2. Multiple metallization layers are used to increase the inductance per unit area.

A.1.2 Three-Terminal Inductors

The three-terminal inductor is a 3-port spiral and is used in this design for differential inductors when the inductors are connected at a common node (e.g. when one node of each inductor is connected to V_{DD}).

Circuit Model

The circuit model given in Figure A.3 was used to model three-terminal inductors [37].

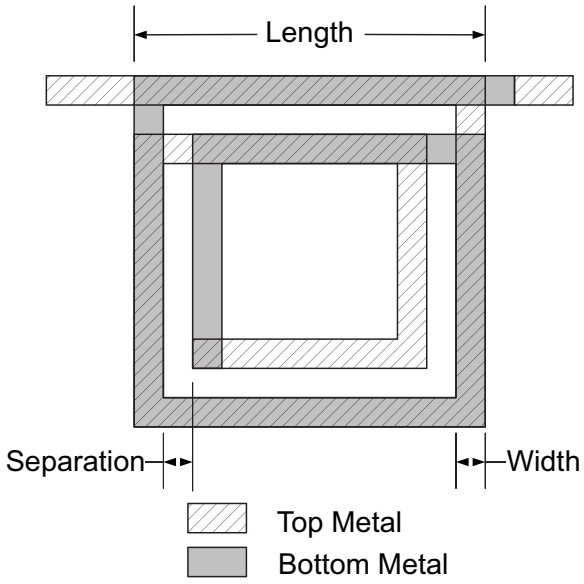


Figure A.2: Multi-level inductor (MLI) layout.

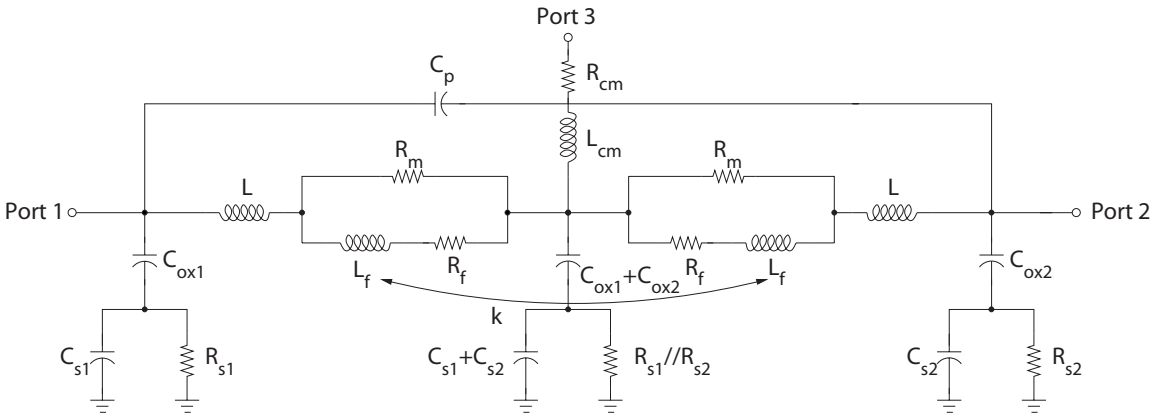


Figure A.3: Three-terminal inductor circuit model.

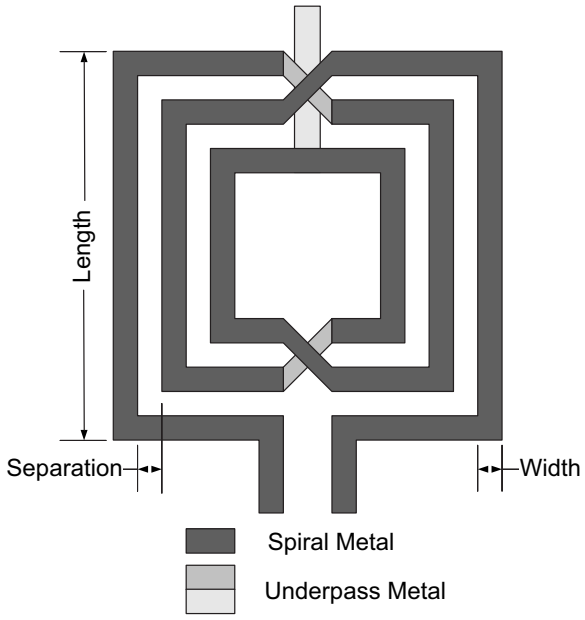


Figure A.4: Three-terminal inductor (3TI) layout.

Layout

The three-terminal inductor (3TI) layout used in this project is given in Figure A.4.

A.1.3 Transformers

Transformers are 4-port spirals that consist of two interwound spirals. Transformers are used in this project to implement inductances for both sides of a differential transmission line. Since the transformer is driven differentially, its per-side inductance is increased by an amount equal to the mutual inductance between the two spirals. Thus, a transformer can achieve a larger per-area inductance than two isolated spirals.

Circuit Model

The circuit model given in Figure A.5 was used to model transformers [38].

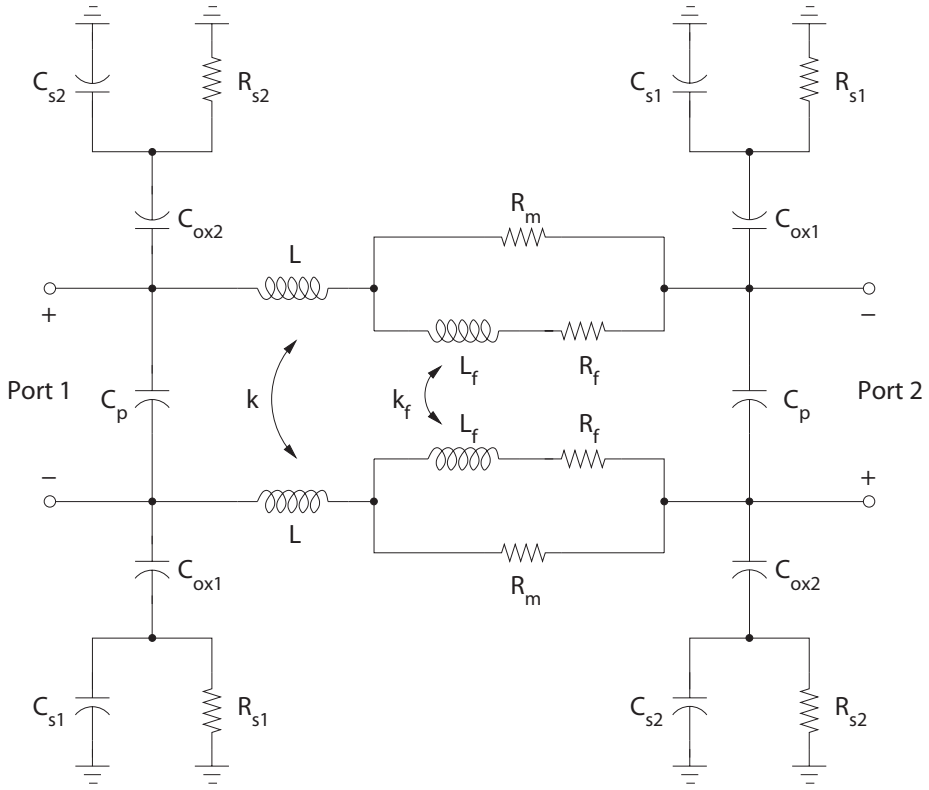


Figure A.5: Transformer circuit model.

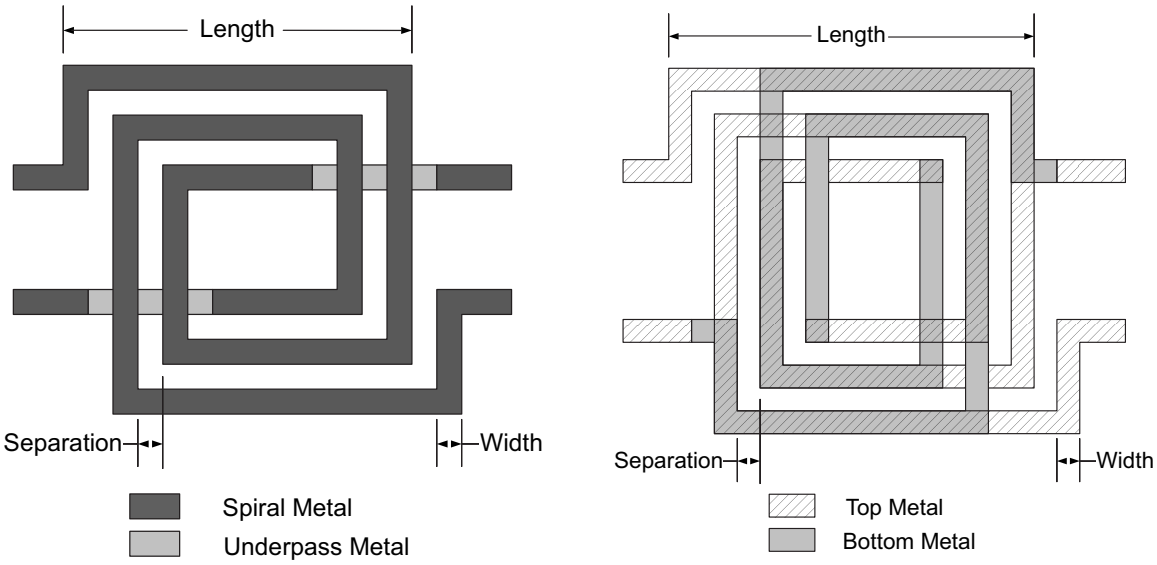


Figure A.6: Transformer layouts. a) Basic transformer (BT) layout. b) Multi-level transformer (MLT) layout.

Layouts

The two transformer layouts used in this project, the basic transformer (BT) and multi-level transformer (MLT) layouts are given in Figure A.6.

A.2 Inductor Characterization

The characterization of each of the inductors is given in this section. Tables A.1 and A.2 provide layout and modelling parameters for the inductors used in the 90-nm and 0.18-μm equalizers, respectively.

Figure A.7 provides plots of simulated (by ASITIC) versus modelled (using circuit model) inductance and quality factor for each of the inductor designs used in the 90-nm equalizer design. Figure A.8 provides these plots for the inductors used in the 0.18-μm equalizer design.

Table A.1: Table of inductor layout and modelling parameters for 90-nm equalizer.

Value	156.25 pH	312.5 pH	150 pH	350 pH
Type	Trans.	Trans.	3-Term Ind.	3-Term Ind.
Layout	BT	BT	3TI	3TI
Top Metal	M8-M9	M8-M9	M9	M9
Bottom Metal	M6-M7	M6-M7	M7,M8	M7,M8
Length (μm)	41	47	36.5	46
Turns	1.25	2.25	1.5	2.5
Width (μm)	2	2	2	2
Separation (μm)	2	2	2	2
L (pH)	110	193	102.8	214
R_m (Ω)	1.8	3.26	3.05	5.94
R_f (Ω)	2.6	3.26	3.7	5.94
L_f (pH)	65	90	40	80
C_{ox1} (fF)	5.65	7.28	3.94	6.41
C_{ox2} (fF)	6.02	8.41	3.65	5.52
C_{s1} (fF)	1	1	1.2	1
C_{s2} (fF)	1	1	1.2	1
R_{s1} (Ω)	4000	6000	8500	10500
R_{s2} (Ω)	4000	6000	8500	10500
C_p (fF)	0.2	0.8	0	1.3
k	0.40	0.48	0.40	0.53
k_f	0	0	-	-
L_{cm} (pH)	-	-	5	5
R_{cm} (Ω)	-	-	0.1	0.1

Table A.2: Table of inductor layout and modelling parameters for 0.18-μm equalizer. SE represents single-ended inductors, Diff. represents differential inductors.

Value	105 pH (SE)	105 pH (Diff.)	210 pH (SE)	210 pH (Diff.)
Type	Ind.	Trans.	Ind.	Trans.
Layout	MLI	BT	MLI	MLT
Top Metal	M6	M5-M6	M6	M6
Bottom Metal	M4-M5	M3-M4	M4-M5	M4-M5
Length (μm)	22	38	26	43
Turns	2.25	1.25	3.25	2.25
Width (μm)	4	3	4	4
Separation (μm)	2	2	2	2
L (pH)	100	91	191	139
R_m (Ω)	5.0	2.8	9.9	10.0
R_f (Ω)	2.7	3.0	4.0	3.3
L_f (pH)	31	50	66	51
C_{ox1} (fF)	2.77	4.53	3.42	5.63
C_{ox2} (fF)	3.85	4.46	6.27	4.94
C_{s1} (fF)	0.82	1.04	0.67	1.12
C_{s2} (fF)	1.13	1.00	1.34	0.94
R_{s1} (Ω)	12250	9741	15100	9040
R_{s2} (Ω)	8936	10040	7500	10740
C_p (fF)	1.75	0	4	2.5
k	-	0.11	-	0.38
k_f	-	0.10	-	0.20

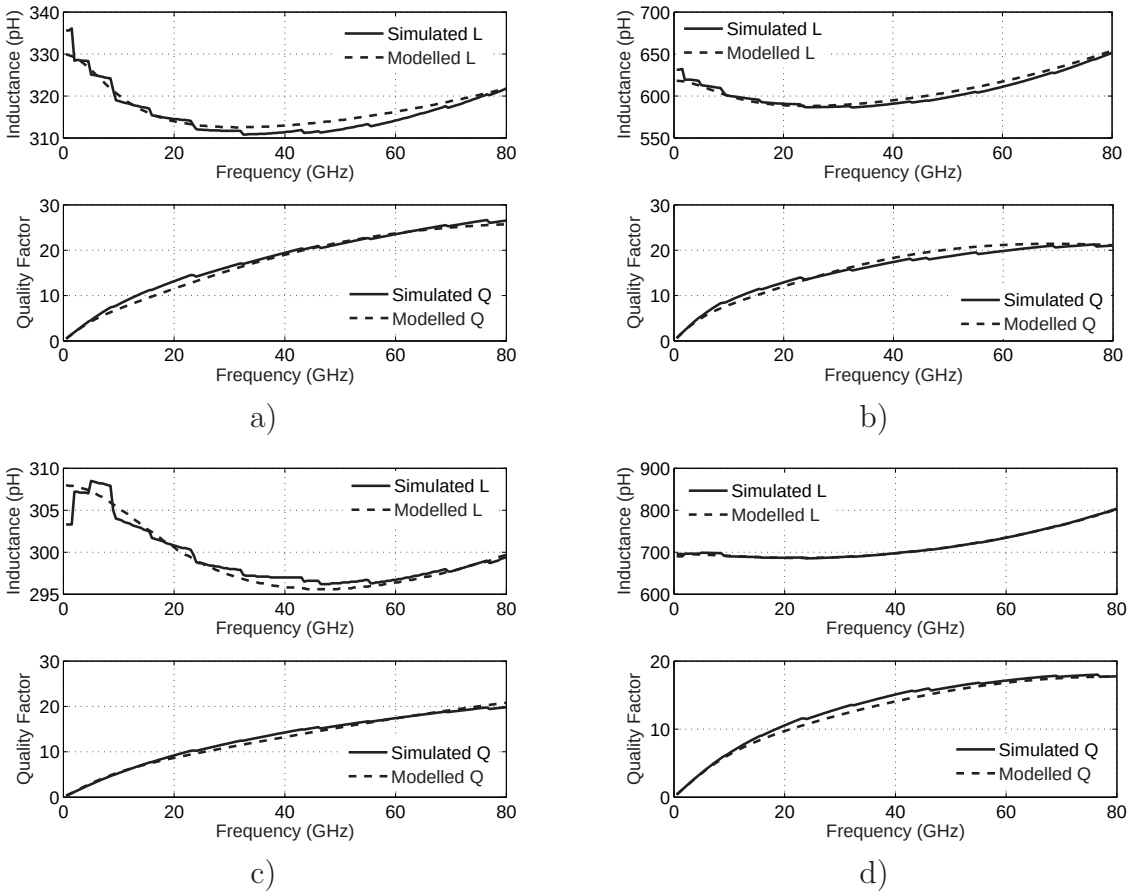


Figure A.7: Simulated vs. modelled inductance and quality factor for inductors used in the 90-nm equalizer design. a) 156.25 pH transformer. b) 312.5 pH transformer. c) 150 pH three-terminal inductor. d) 350 pH three-terminal inductor.

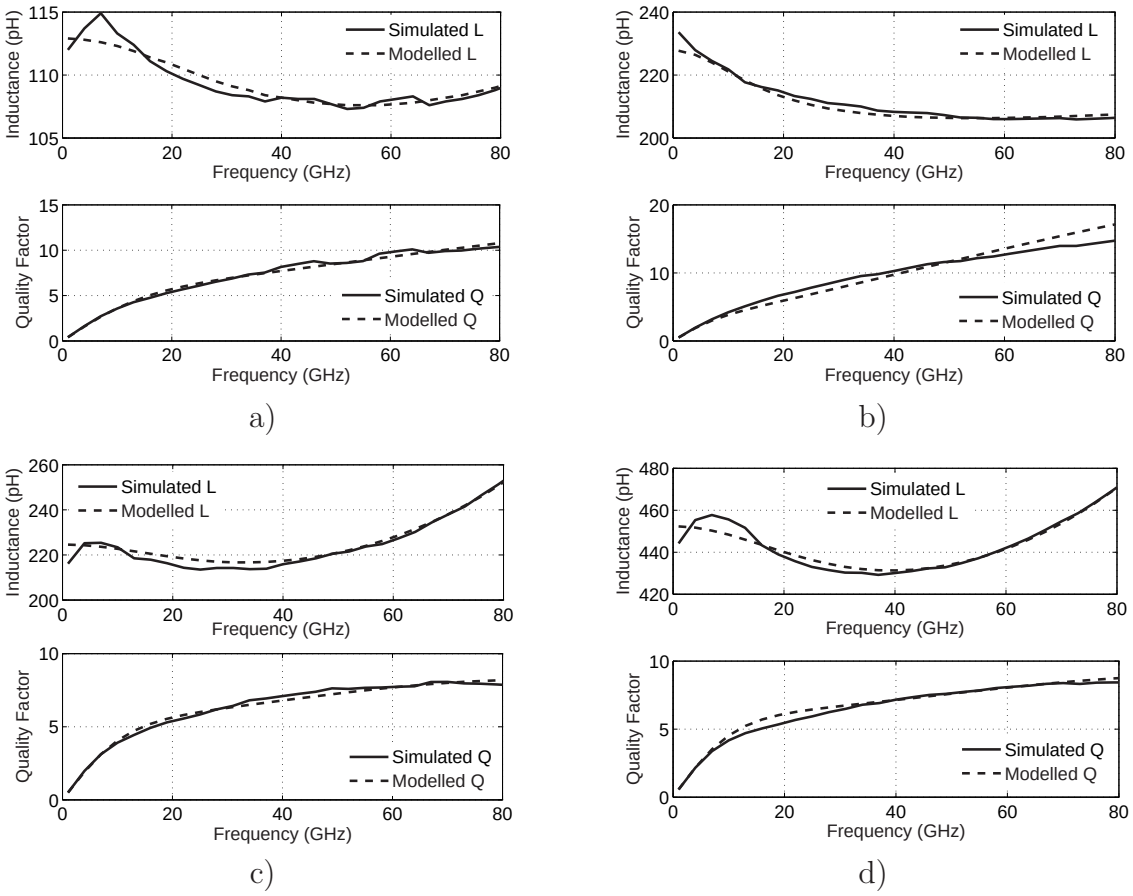


Figure A.8: Simulated vs. modelled inductance and quality factor for inductors used in the 0.18-μm equalizer design. a) 105 pH single-ended inductor. b) 105 pH transformer. c) 210 pH single-ended inductor. d) 210 pH transformer.

Appendix B

90-nm Equalizer Digital Control Register Map

Table B.1 provides a map of the internal digital control register for the 90-nm equalizer IC. This register can be loaded using the DIN and CLK inputs to the equalizer. Each time a rising edge on the CLK input is detected, the value of DIN is read into bit b_{51} of the control register. The existing bits are shifted toward the end of the register. Thus, the bits should be loaded in the order shown, from b_0 to b_{51}. While the register is loaded, the state of the equalizer changes, rendering the equalizer unusable until all control bits have been loaded.

Table B.1: 90-nm equalizer - Digital control register map. *Bit* refers to the register location; *Name* refers to the function of the control bit. Note that some of the control bits use negative logic.

Bit	Name		Bit	Name		Bit	Name	
b_0	$\overline{pa\_ctrl\_b0}$	Preamp	b_{17}	$\overline{tap1p\_b5}$	Tap 1 (+ve)	b_{35}	$\overline{tap3n\_b0}$	Tap 3 (-ve)
b_1	$\overline{pa\_ctrl\_b1}$		b_{18}	$\overline{tap1p\_b4}$		b_{36}	$\overline{tap3n\_b1}$	
b_2	$\overline{pa\_ctrl\_b2}$		b_{19}	$\overline{tap1p\_b3}$		b_{37}	$\overline{tap3n\_b2}$	
b_3	$\overline{pa\_ctrl\_b3}$		b_{20}	$\overline{tap1p\_b2}$		b_{38}	$\overline{tap3n\_b3}$	
b_4	$\overline{pa\_ctrl\_b4}$		b_{21}	$\overline{tap1p\_b1}$		b_{39}	$\overline{tap3n\_b4}$	
b_5	$\overline{pa\_ctrl\_b5}$		b_{22}	$\overline{tap1p\_b0}$		b_{40}	$\overline{tap3n\_b5}$	
b_6	out_cap_b4	Out Cap.	b_{23}	$\overline{tap2n\_b0}$	Tap 2 (-ve)	b_{41}	$\overline{tap3p\_b5}$	Tap 3 (+ve)
b_7	out_cap_b3		b_{24}	$\overline{tap2n\_b1}$		b_{42}	$\overline{tap3p\_b4}$	
b_8	out_cap_b2		b_{25}	$\overline{tap2n\_b2}$		b_{43}	$\overline{tap3p\_b3}$	
b_9	out_cap_b1		b_{26}	$\overline{tap2n\_b3}$		b_{44}	$\overline{tap3p\_b2}$	
b_{10}	out_cap_b0		b_{27}	$\overline{tap2n\_b4}$		b_{45}	$\overline{tap3p\_b1}$	
b_{11}	$\overline{tap1n\_b0}$	Tap 1 (-ve)	b_{28}	$\overline{tap2n\_b5}$		b_{46}	$\overline{tap3p\_b0}$	
b_{12}	$\overline{tap1n\_b1}$		b_{29}	$\overline{tap2p\_b5}$	Tap 2 (+ve)	b_{47}	in_cap_b0	Input Cap.
b_{13}	$\overline{tap1n\_b2}$		b_{30}	$\overline{tap2p\_b4}$		b_{48}	in_cap_b1	
b_{14}	$\overline{tap1n\_b3}$		b_{31}	$\overline{tap2p\_b3}$		b_{49}	in_cap_b2	
b_{15}	$\overline{tap1n\_b4}$		b_{32}	$\overline{tap2p\_b2}$		b_{50}	in_cap_b3	
b_{16}	$\overline{tap1n\_b5}$		b_{33}	$\overline{tap2p\_b1}$		b_{51}	in_cap_b4	
			b_{34}	$\overline{tap2p\_b0}$				

Appendix C

Testbenches and Test Setup

This appendix provides schematics of the testbench and test setups used in the simulation and measurement of the two equalizer designs. Circuit measurement objectives are also briefly described.

C.1 Simulation Testbench

Figure C.1 gives a schematic of the testbench used for circuit simulations. The input of the equalizer is biased using bias-tees. Bias-tees are also used at the output to provide DC current. Using the setup shown, the equalizer sees 50 Ω externally at the output for both DC and AC frequencies. This more accurately represents the intended operation of the equalizer, as it can be directly coupled to a subsequent current-mode logic (CML) stage without a DC block. For S-parameter simulations, ports 1 and 2 are connected to 100-Ω ports. For time-domain simulations, the output is simply terminated in 50-Ω loads, and the input is driven using the circuit shown in Figure C.2. This circuit generates random data and corrupts it with PMD before driving the input of the equalizer with a 100-Ω (differential) output impedance.

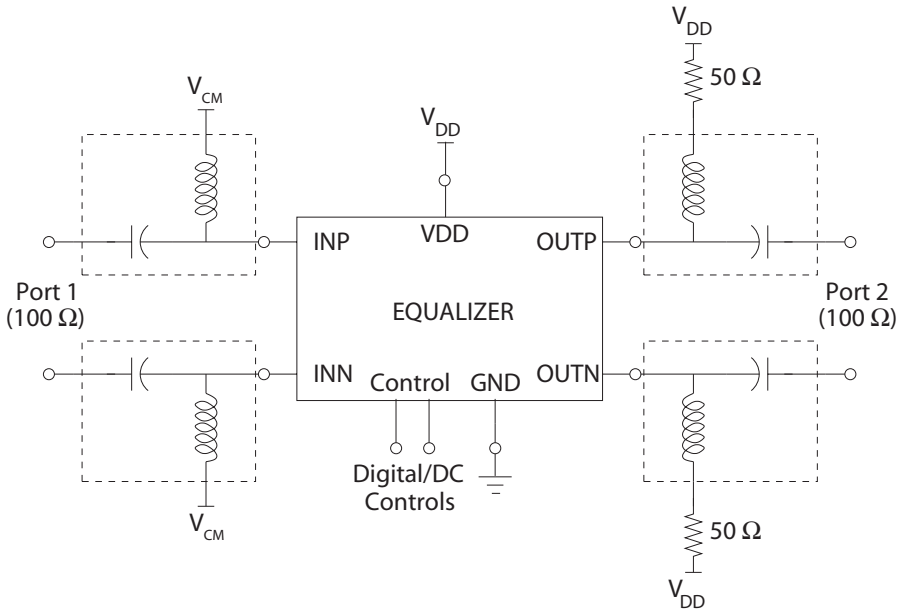


Figure C.1: Schematic of simulation testbench used for both 90-nm and 0.18-μm equalizer designs.

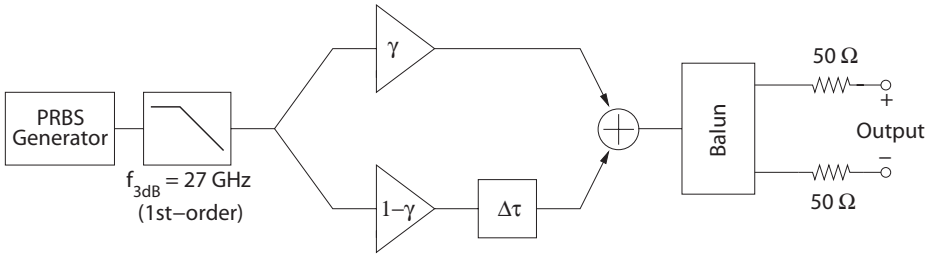


Figure C.2: Schematic of PMD emulator used as the source for time-domain simulation of both the 90-nm and 0.18-μm equalizer designs.

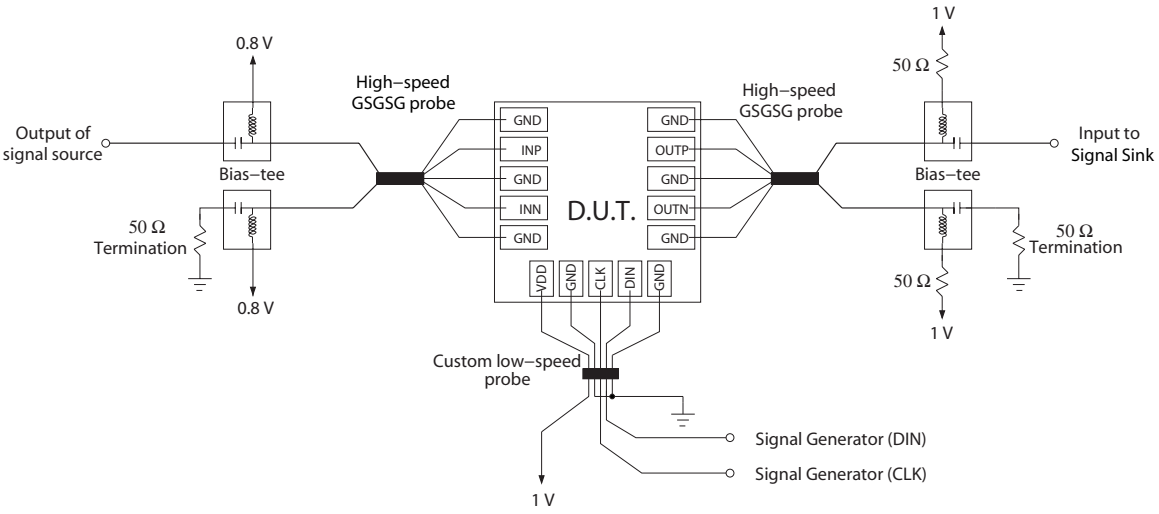


Figure C.3: Test setup for measurement of the 90-nm equalizer IC.

C.2 Test Setup and Objectives

This section describes the test setup and the main objectives for the measurement of the two equalizer designs. The measurements closely parallel the simulations, with both S-parameter and time-domain analyses to be performed.

C.2.1 Test Setup

The test setups to be used for the measurement of the 90-nm and 0.18-μm equalizer ICs are given in Figures C.3 and C.4. Note that single-ended measurement is required due to the difficulty in properly accounting for the skew between differential signals at high speeds. The signal source and sink could be the ports of a network analyzer or a data source and an oscilloscope, depending on the particular measurement.

C.2.2 S-parameter Measurement Objectives

Using a network analyzer, the equalizers will be characterized in terms of their S-parameters. S_{11} and S_{22} will be measured to determine the accuracy of the input and

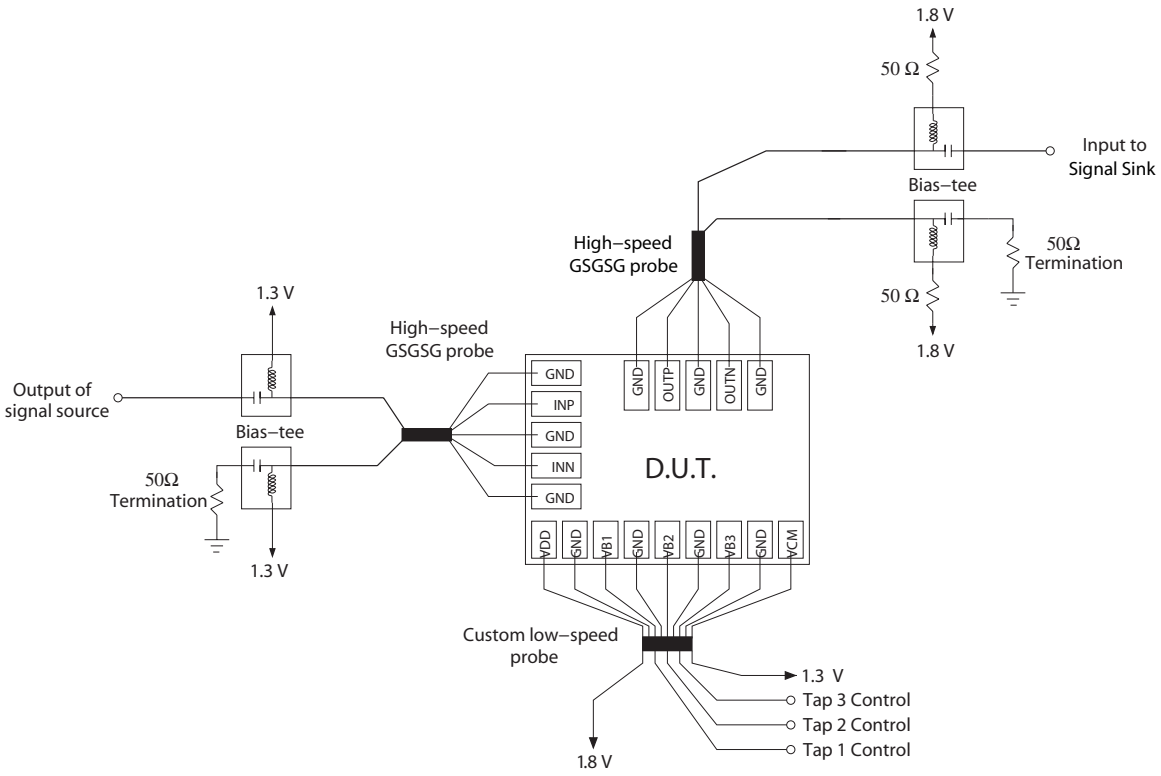


Figure C.4: Test setup for measurement of the 0.18-μm equalizer IC.

output matching. S_{21} will be measured for each of the equalizer taps to determine tap gain, bandwidth and delay.

C.2.3 Time-domain Measurement Objectives

Initial time-domain measurements will consist of providing a sinusoidal input and measuring the difference in delay through each of the three equalizer taps. Ultimately, however, the time-domain measurements are meant to verify the ability of the equalizer to perform equalization of a 40-Gb/s data stream. A 40-Gb/s data stream from a PRBS generator will be corrupted with ISI by an electronically emulated PMD channel. The equalizer taps will be optimized and the improvement in eye opening achieved due to equalization will be determined.

References

[1] J. Hecht, *City of Light: The Story of Fiber Optics*. New York: Oxford University Press, 1999.

[2] K. Azadet, E. F. Haratsch, H. Kim, F. Saibi, J. H. Saunders, M. Shaffer, L. Song, and M. L. Yu, "Equalization and FEC techniques for optical transceivers," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 3, pp. 317–327, Mar. 2002.

[3] H. Bülow, "Polarisation mode dispersion (PMD) sensitivity of a 10 Gbit/s transmission system," in *Optical Communication, 1996. ECOC '96. 22nd European Conference on*, vol. 2, 1996, pp. 211–214.

[4] ——, "PMD mitigation techniques and their effectiveness in installed fiber," in *Optical Fiber Communication Conference, 2000*, vol. 3, 2000, pp. 110–112.

[5] H. Bülow, W. Baumert, H. Schmuck, F. Mohr, T. Schulz, F. Kuppers, and W. Weiershausen, "Measurement of the maximum speed of PMD fluctuation in installed field fiber," in *Optical Fiber Communication Conference, 1999, and the International Conference on Integrated Optics and Optical Fiber Communication. OFC/IOOC '99. Technical Digest*, vol. 2, 1999, pp. 83–85.

[6] H. Bülow, F. Buchali, W. Baumert, R. Ballentin, and T. Wehren, "PMD mitigation at 10 Gbit/s using linear and nonlinear integrated electronic equaliser circuits," *Electronics Letters*, vol. 36, no. 2, pp. 163–164, 2000.

[7] L. Möller, S. Thiede, S. Chandrasekhar, W. Benz, M. Lang, T. Jakobus, and M. Schlechtweg, "ISI mitigation using decision feedback loop demonstrated with PMD distorted 10Gbit/s signals," *Electronic Letters*, vol. 35, no. 24, pp. 2092–2093, 1999.

[8] G. Kanter, P. Capofreddi, S. Behtash, and A. Gandhi, "Electronic equalization for extending the reach of electro-absoption modulator based transponders," in *Optical Fiber Communication Conference and Exhibit, 2003. OFC 2003*, vol. 2, 2003, pp. 476–477.

[9] H. Wu, J. A. Tierno, P. Pepeljugoski, J. Schaub, S. Gowda, J. A. Kash, and A. Hajimiri, "Integrated transversal equalizers in high-speed fiber-optic systems," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 12, pp. 2131–2137, Dec. 2003.

[10] C. Pelard, E. Gebara, A. J. Kim, M. G. Vrazel, F. Bien, Y. Hur, M. Maeng, S. Chandramouli, C. Chun, S. Bajekal, S. E. Ralph, B. Schmukler, V. M. Hietala, and J. Laskar, "Realization of multigigabit channel equalization and crosstalk cancellation integrated circuits," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 10, pp. 1659–1670, Oct. 2004.

[11] M. Nakamura, H. Nosaka, M. Ida, K. Kurishima, and M. Tokumitsu, "Electrical PMD equalizer ICs for a 40-Gbit/s transmission," in *Optical Fiber Communication Conference and Exhibit, 2004. OFC 2004*, vol. TuG4, 2004.

[12] A. Hazneci and S. P. Voinigescu, "A 49-Gb/s, 7-tap transversal filter in 0.18μm SiGe BiCMOS for backplane equalization," in *IEEE Compound Semiconductor Integrated Circuits Symposium*, Monterey, CA, Oct. 2004.

[13] J. J. Refi, "Optical fibers for optical networking," *Bell Labs Technical Journal*, pp. 246–261, Jan.-Mar. 1999.

[14] B. Razavi, *Design of Integrated Circuits for Optical Communications.* New York: McGraw-Hill, 2003.

[15] C. D. Poole, R. W. Tkach, A. R. Chraplyvy, and D. A. Fishman, "Fading in lightwave systems due to polarization-mode dispersion," *IEEE Photonics Technology Letters*, vol. 3, no. 1, pp. 68–70, Jan. 1991.

[16] H. Bülow, "Operation of digital optical transmission system with minimal degradation due to polarisation mode dispersion," *Electronic Letters*, vol. 31, no. 3, pp. 214–215, 1995.

[17] G. J. Foschini and C. D. Poole, "Statistical-theory of polarization dispersion in single-mode fibers," *IEEE/OSA Journal of Lightwave Technology*, vol. 9, no. 11, pp. 1439–1456, Nov. 1991.

[18] N. Gisin, R. Passy, J. C. Bishoff, and B. Perny, "Experimental investigations of the statistical properties of polarization mode dispersion in single mode fibers," *IEEE Photonics Technology Letters*, vol. 5, no. 7, pp. 819–821, July 1993.

[19] R. Ramaswami and K. N. Sivarajan, *Optical Networks - A Practical Perspective, Second Edition.* Morgan Kaufmann Publishers, 2002.

[20] F. Buchali and H. Bülow, "Adaptive PMD compensation by electrical and optical techniques," *IEEE/OSA Journal of Lightwave Technology*, vol. 22, no. 4, pp. 1116–1126, Apr. 2004.

[21] B. Wedding and C. N. Haslach, "Enhanced PMD mitigation by polarization scrambling and forward error correction," in *Optical Fiber Communication Conference and Exhibit, 2001. OFC 2001*, vol. 3, 2001, pp. WAA1–1–WAA1–3.

[22] L. Song, M.-L. Yu, and M. S. Shaffer, "10- and 40-Gb/s forward error correction devices for optical communications," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 11, pp. 1565–1573, Nov. 2002.

[23] D. Penninckx, S. Lanne, and H. Bülow, "WDM redundancy to counteract PMD effects in optical systems," in *Optical Communication, 2001. ECOC '01. 27th European Conference on*, vol. 3, 2001, pp. 444–445.

[24] H. F. Haunstein, W. Sauer-Greff, A. Dittrich, K. Sticht, and R. Urbansky, "Principles for electronic equalization of polarization-mode dispersion," *IEEE/OSA Journal of Lightwave Technology*, vol. 22, no. 4, pp. 1169–1182, Apr. 2004.

[25] H. Sunnerud, M. Karlsson, C. J. Xie, and P. A. Andrekson, "Polarization-mode dispersion in high-speed fiber-optic transmission systems," *IEEE/OSA Journal of Lightwave Technology*, vol. 20, no. 12, pp. 2204–2219, Dec. 2002.

[26] H. Sunnerud, M. Westlund, J. Li, J. Hansryd, M. Karlsson, P.-O. Hedekvist, and P. A. Andrekson, "Long-term 160 Gb/s-TDM, RZ transmission with automatic PMD compensation and system monitoring using an optical sampling system," in *Optical Communication, 2001. ECOC '01. 27th European Conference on*, vol. 6, 2001, pp. 18–19.

[27] C. Francia, J.-P. Bruyère, F. Thiéry, and D. Penninckx, "Simple dynamic polarisation mode dispersion compensator," *Electronics Letters*, vol. 35, no. 5, pp. 414–415, 1999.

[28] H. Sunnerud, C. J. Xie, M. Karlsson, R. Samuelsson, and P. A. Andrekson, "A comparison between different PMD compensation techniques," *IEEE/OSA Journal of Lightwave Technology*, vol. 20, no. 3, pp. 368–378, Mar. 2002.

[29] H. Bülow and G. Thielecke, "Electronic PMD mitigation - from linear equalization to maximum-likelihood detection," in *Optical Fiber Communication Conference and Exhibit, 2001. OFC 2001*, vol. 3, 2001, pp. WAA3–1–WAA3–3.

[30] G. Zhang, P. Chaudhari, and M. Green, "26.7 - a BiCMOS 10Gb/s adaptive cable equalizer," in *Solid-State Circuits Conference, 2004. Digest of Technical Papers. ISSCC. 2004 IEEE International*, 2004, pp. 482–491.

[31] R. S. Kajley, P. J. Hurst, and J. E. C. Brown, "A mixed-signal decision-feedback equalizer that uses a look-ahead architecture," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 3, pp. 450–459, Mar. 1997.

[32] P. Pepeljugoski, S. E. Golowich, A. J. Ritger, P. Kolesar, and A. Risteski, "Modeling and simulation of next-generation multimode fiber links," *IEEE/OSA Journal of Lightwave Technology*, vol. 21, no. 5, pp. 1242–1255, May 2003.

[33] J. Lee, P. Roux, U.-V. Koc, T. Link, Y. Baeyens, and Y.-K. Chen, "A 5-b 10-GSample/s A/D converter for 10-Gb/s optical receivers," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 10, pp. 1671–1679, Oct. 2004.

[34] S. Pavan, "Continuous-time integrated FIR filters at microwave frequencies," *IEEE Transactions on Circuits and Systems—Part II: Analog and Digital Signal Processing*, vol. 51, no. 1, pp. 15–20, Jan. 2004.

[35] C. Rauscher, "Microwave active filters based on transversal and recursive principles," *IEEE Transactions on Microwave Theory and Techniques*, vol. MTT-33, no. 12, pp. 1350–1360, Dec. 1985.

[36] A. S. Sedra and K. C. Smith, *Microelectronic Circuits - Fourth Edition.* New York: Oxford University Press, 1998.

[37] K. B. Ashby, I. A. Koullias, W. C. Finley, J. J. Bastek, and S. Moinian, "High Q inductors for wireless applications in a complementary silicon bipolar process," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 1, pp. 4–9, Jan. 1996.

[38] J. R. Long and M. Danesh, "A uniform compact model for planar RF/MMIC interconnect, inductors and transformers," in *Bipolar/BiCMOS Circuits and Technology Meeting, Proceedings of the 2001*, 2001, pp. 167–170.