Algorithmic Design Methodologies and Design Porting of Wireline Transceiver IC Building Blocks Between Technology Nodes

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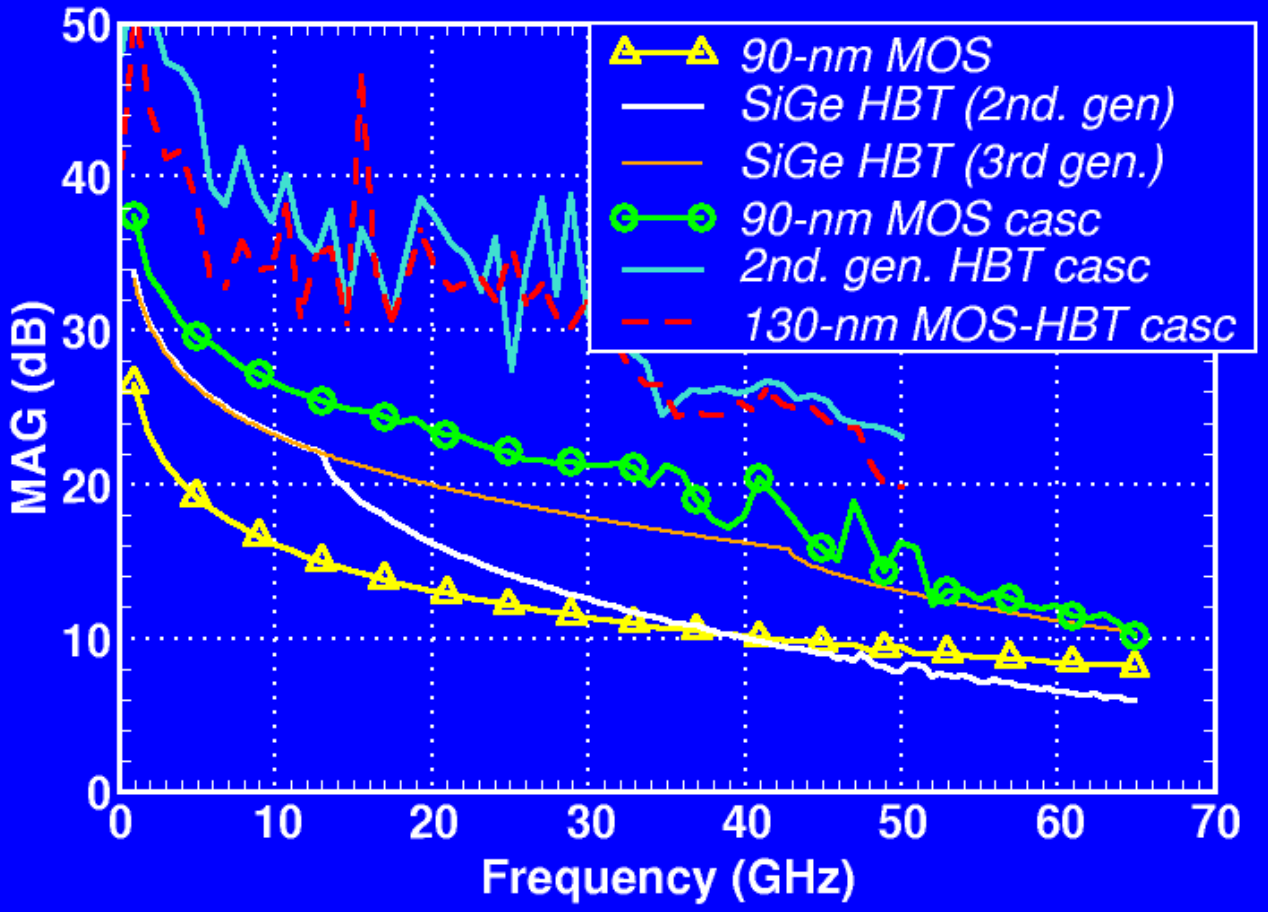
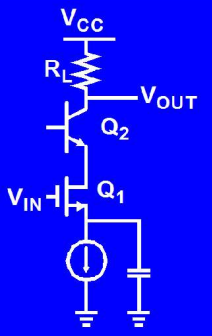
Outline

- Introduction
- Low-noise broadband input comparators
- Mm-wave VCOs
- High-speed logic gates
- Circuits beyond 40 Gb/s
- Summary

Si(Ge Bi)CMOS speed is free ... if you can afford the mask costs!

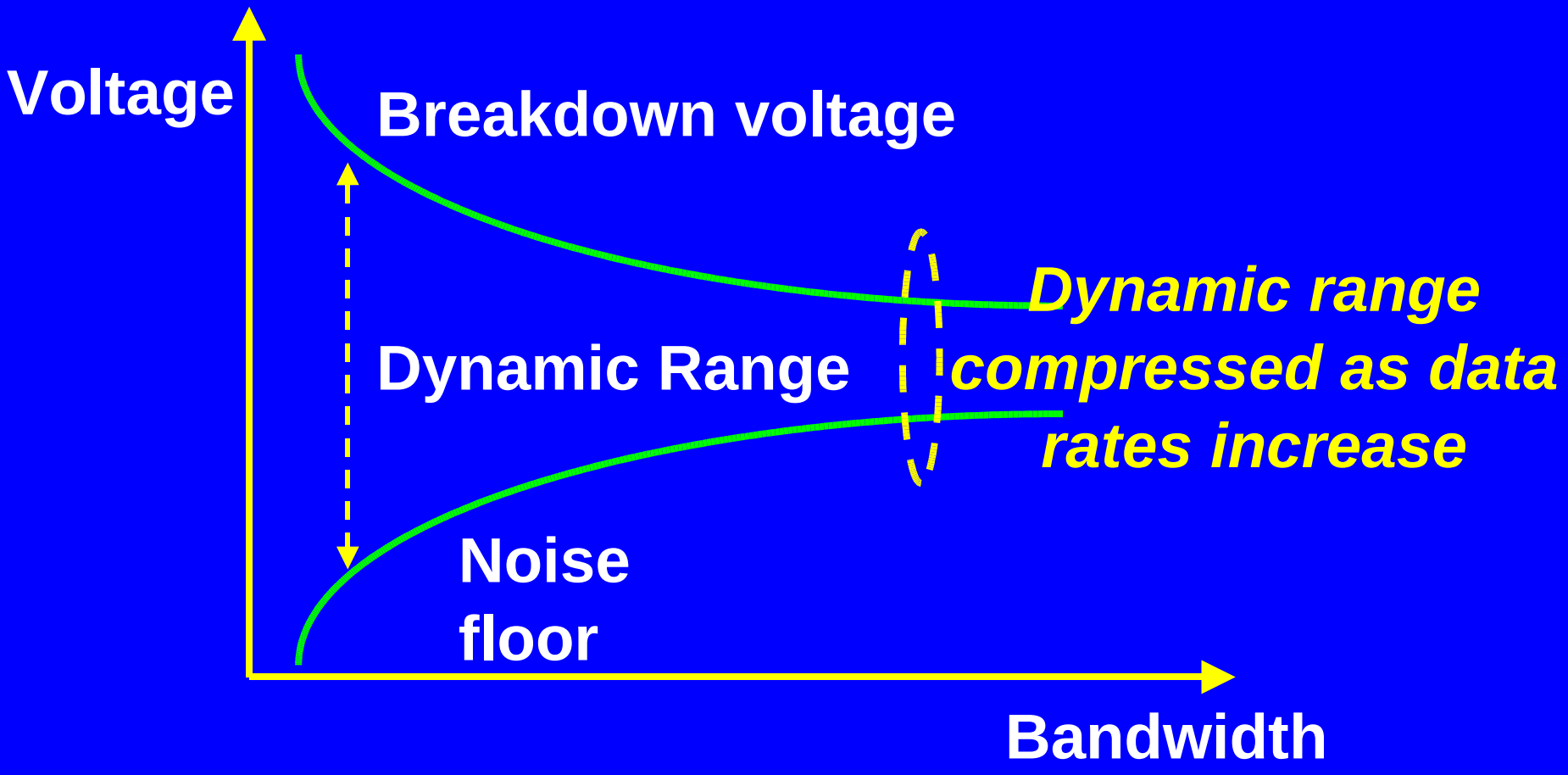




MOS-HBT (BiCMOS) Cascode

- MAG > 8 dB @ 65 GHz in HBTs and MOSFETs
- HBT-based cascodes have highest gain
- Benefits of the MOS cascode questionable at 65 GHz

Fundamental limitations of dynamic range



Emphasizes need for low-noise design methodologies

Power dissipation a major limitation in circuits beyond 40 Gb/s

- Bipolar only implementations suffer from
  - V_{cc} >= 3.3V
  - 40 GHz latch consumes more than 50 mW
- CMOS has lower supply voltage and lower power dissipation but
  - 40 GHz latch has yet to be demonstrated
  - must design in 90/65 nm with first pass success

Emphasizes need for new low-voltage, high-speed logic topologies and robust design methodologies

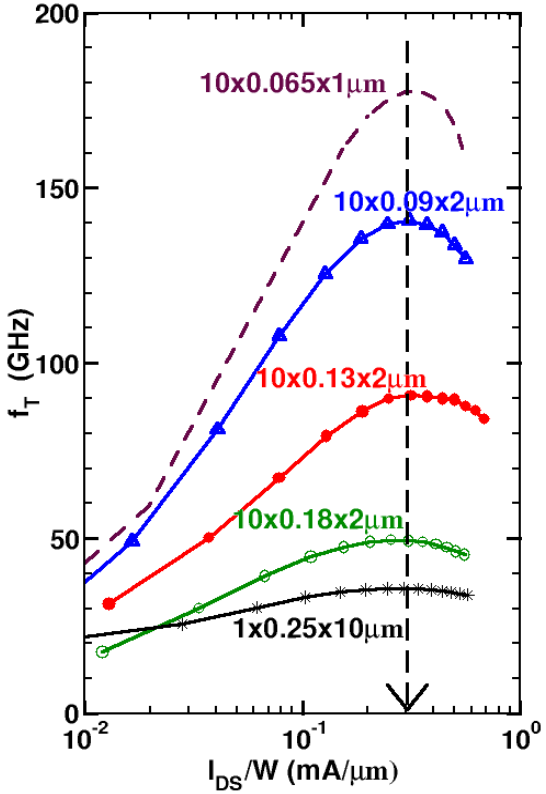
Goal of this presentation

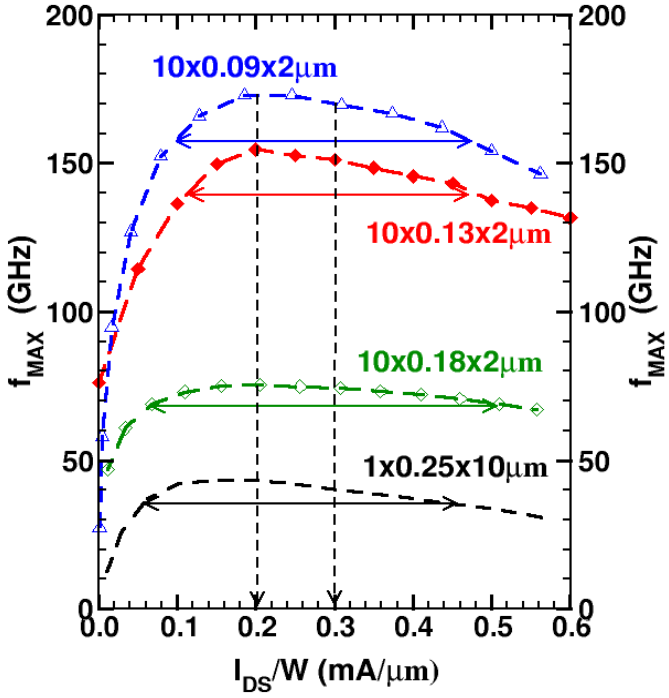
- Prove that algorithmic design methodologies exist for optimal solutions for all wireline building blocks
  - Broadband input amplifiers
  - VCOs
  - (Bi)MOS-CML logic gates
- Prove that CMOS implementations are portable between technology nodes and foundries

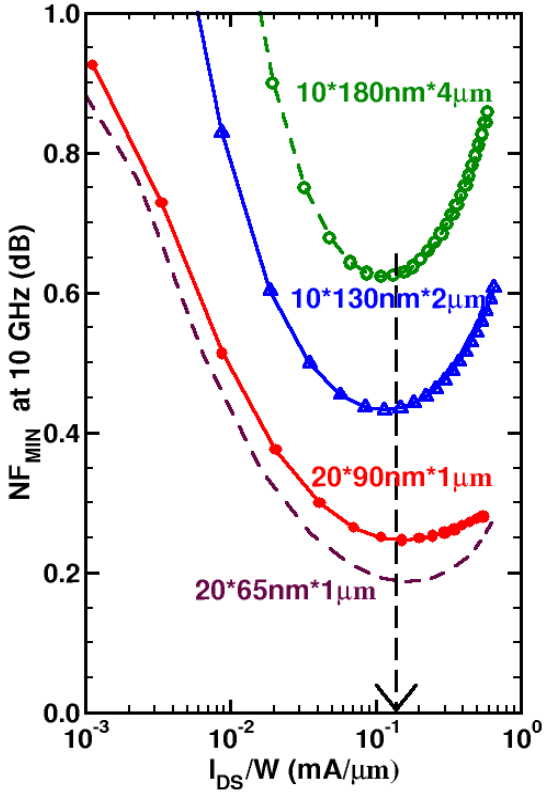
Key enablers

- Invariance of characteristic current densities in MOSFETs
- Low-noise broadband matching, biasing, and sizing
- Low-voltage (Bi)CMOS topologies
- Small footprint (less than 20 μm per side) inductors with SRF> 100 GHz

MOSFET characteristic current densities invariant across nodes & foundries







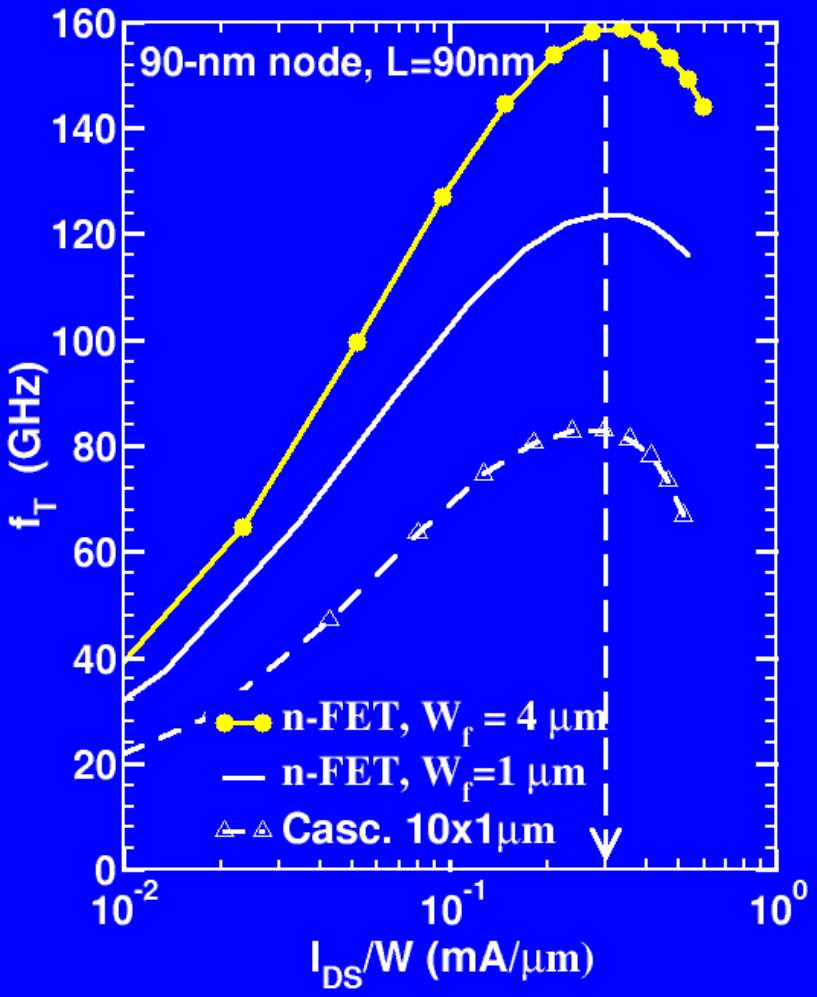
Peak f_T @ 0.3 mA/μm

Peak f_{MAX} @ 0.2 mA/μm

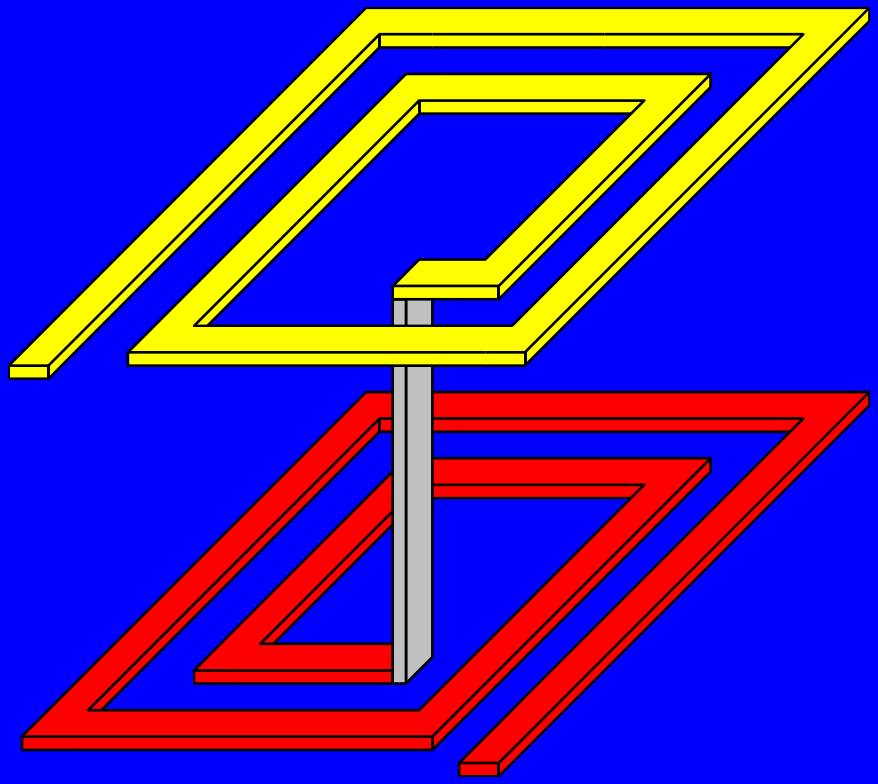
NF_{MIN} @ 0.15 mA/μm

Characteristic MOSFET current densities invariant over CS and cascode topologies

- The peak f_T current density of a MOSFET cascode stage remains 0.3 mA/μm
- Cascode stage can be treated as a composite transistor in circuit design (f_T, f_{MAX}, NF_{MIN})
- f_T of MOSFET cascode is < 60% of MOSFET f_T



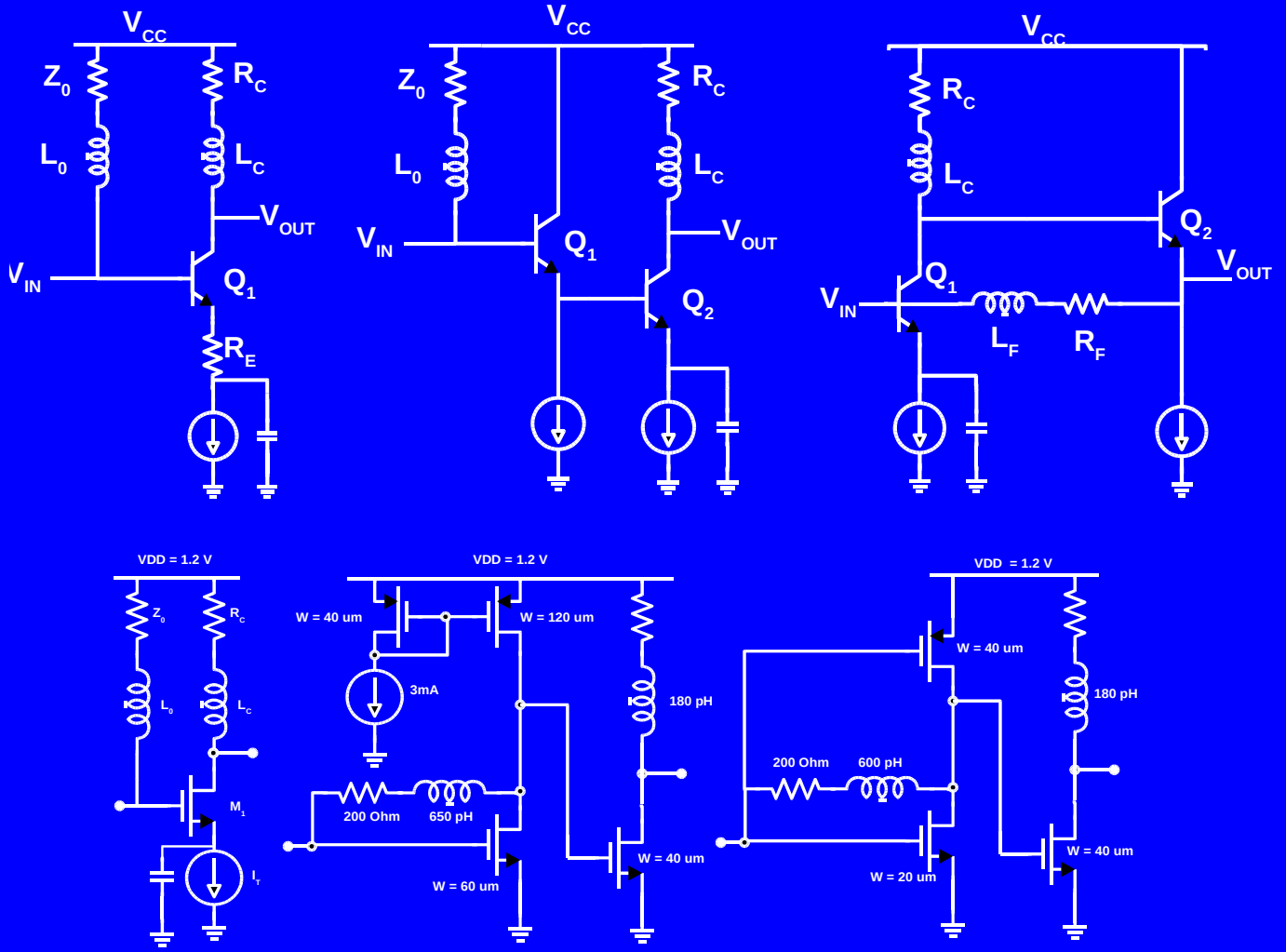
Vertically stacked, multi-metal inductors for CML logic



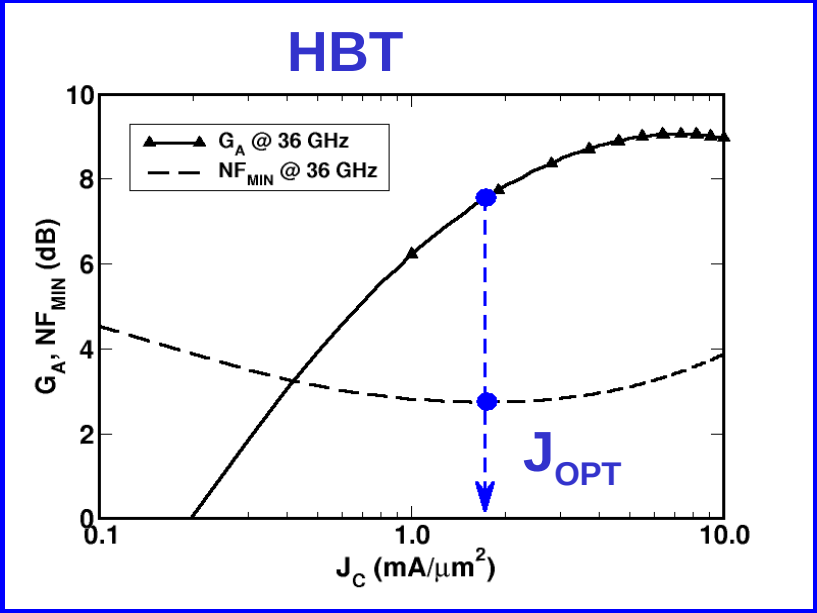
- Q is not important
- Size is important
- Maximize *L*SRF* to trade-off tail current for bandwidth
- Use 3-7 metals

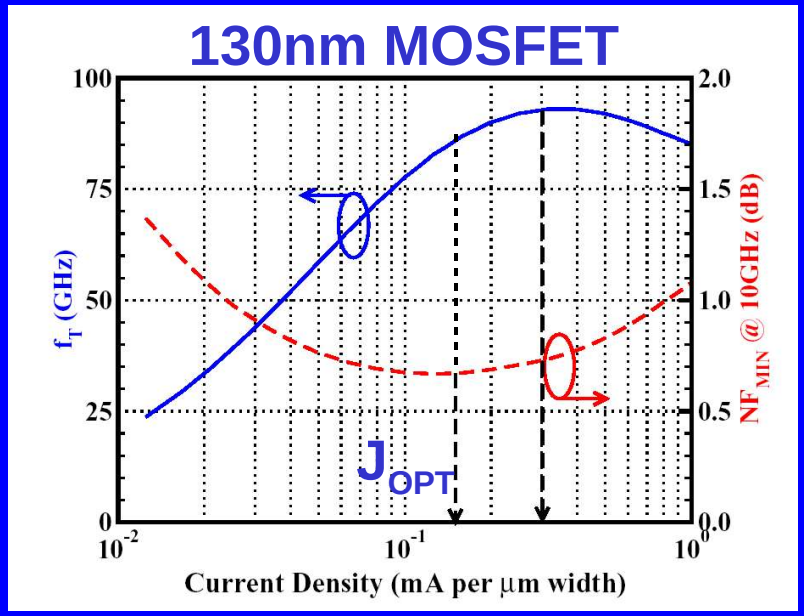
T. Dickson et al. IMS-2004

Low-noise broadband amplifiers



Transistor low-noise design
(S. Voinigescu et al., BCTM 1996)





Lowest noise achieved when transistor biased at J_{OPT} (0.15mA/μm).

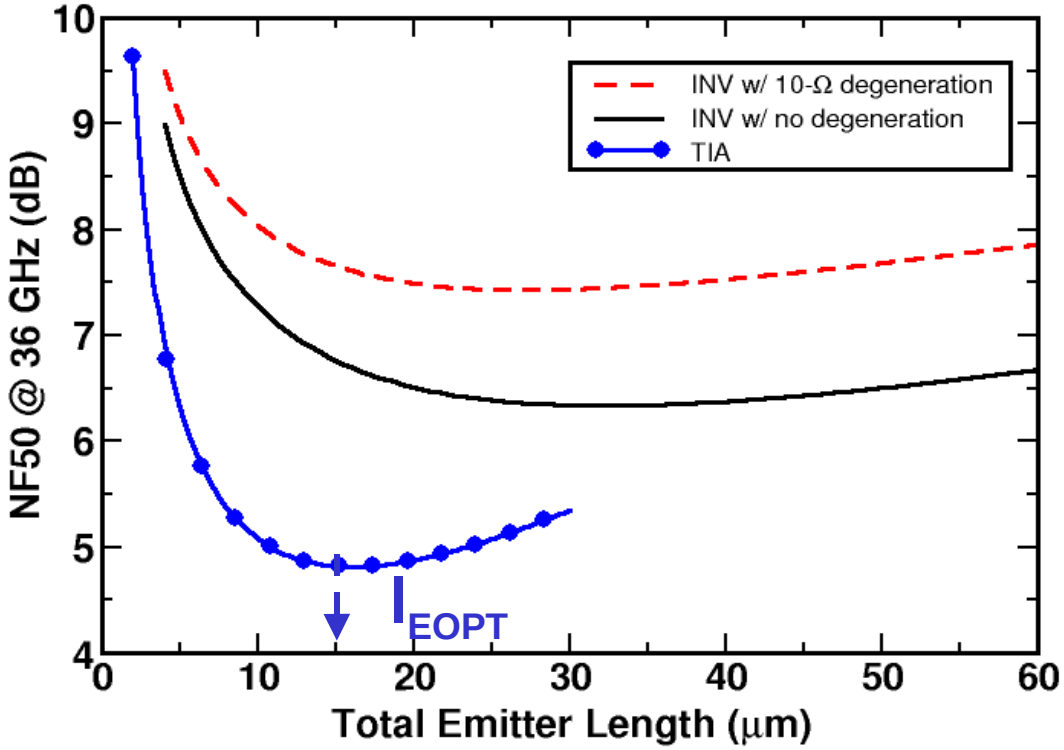
Transistor noise parameters scale with emitter length/ gate width.

$R_N = R/L_E$ $G_N = G\omega^2 L_E$ $G_{COR} = G_C\omega^2 L_E$ $B_{COR} = B\omega L_E$

$R_N = R/W$ $G_N = G\omega^2 W$ $G_{COR} = G_C\omega^2 W$ $B_{COR} = B\omega W$

Optimal biasing and sizing of transistor @ BW3dB is key to low noise design.

Sizing SiGe HBT TIA & INV designs for noise matching



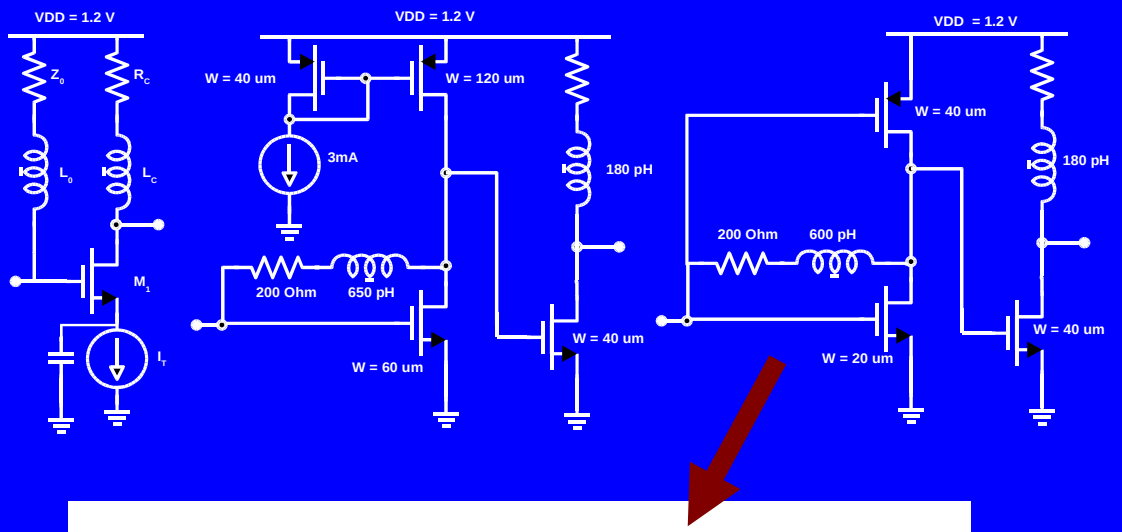
TIA requires much smaller transistor size:

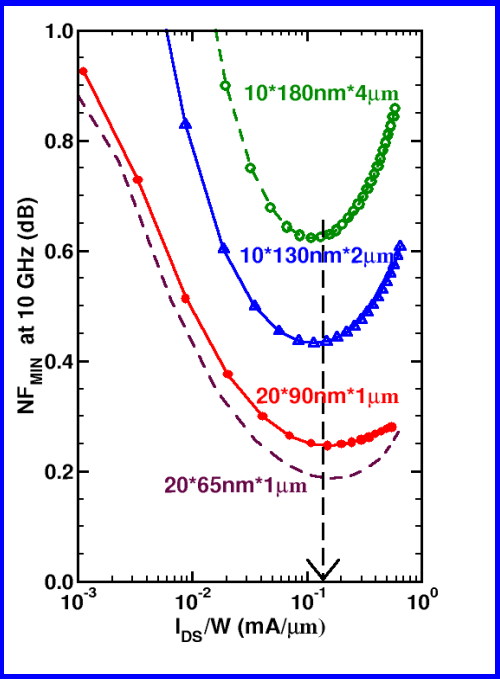
Higher bandwidth

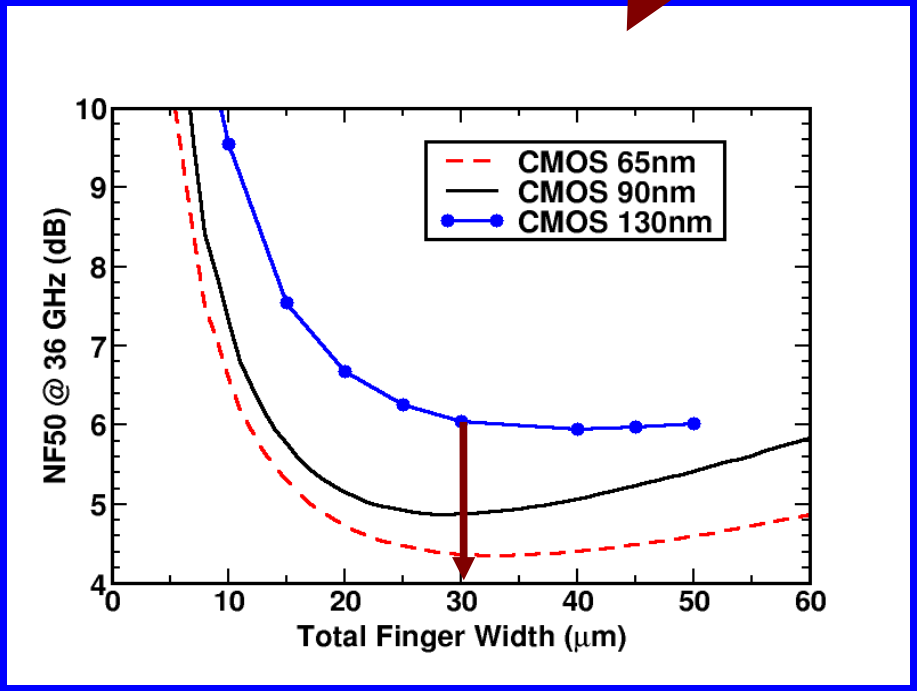
Broadband input match

Lower power consumption

Broadband CMOS LNA topology scaling







- Biased at 0.15 mA/μm
- *W*, I_{DS} do not change with nodes
- *NF50* and BW_{3dB} improve as technology scales

Algorithmic design methodology for broadband low-noise TIAs

1. Bias HBT(MOSFET) at optimal noise current density J_{OPT} (0.15 mA/μm) at 3dB frequency

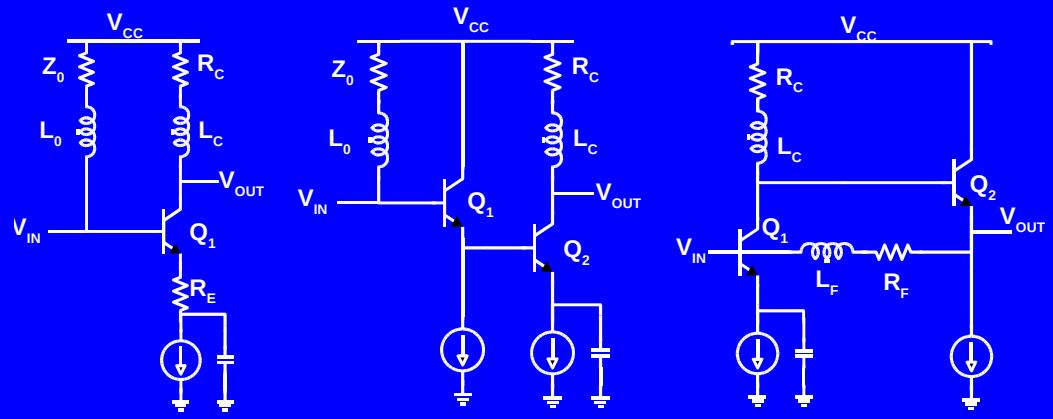
2. Choose the DC voltage drop across R_C for linearity requirements. This fixes the loop gain $T = g_m R_C$ ($=g_m * r_o$)

3. Set the feedback resistance R_F for 50Ω input match.

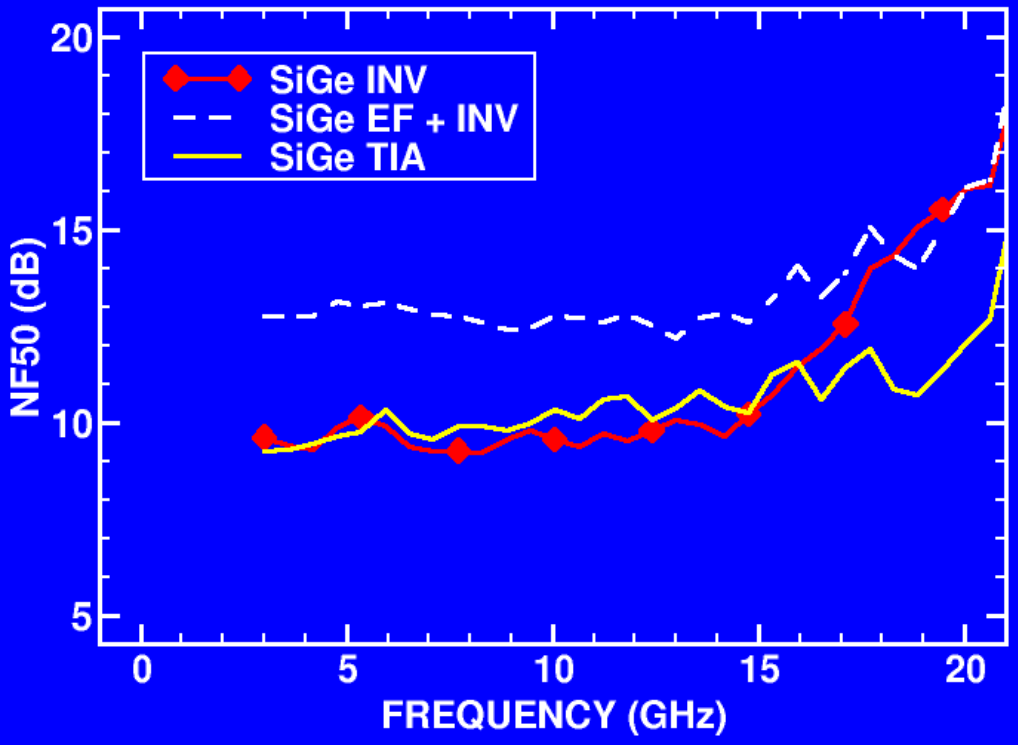
4. Size the emitter length (gate width) of Q1 for low-noise, such that the TIA noise impedance is 50Ω .

5. Add inductors to extend bandwidth and filter high-frequency noise.

Measured single-ended 50-Ohm noise figure



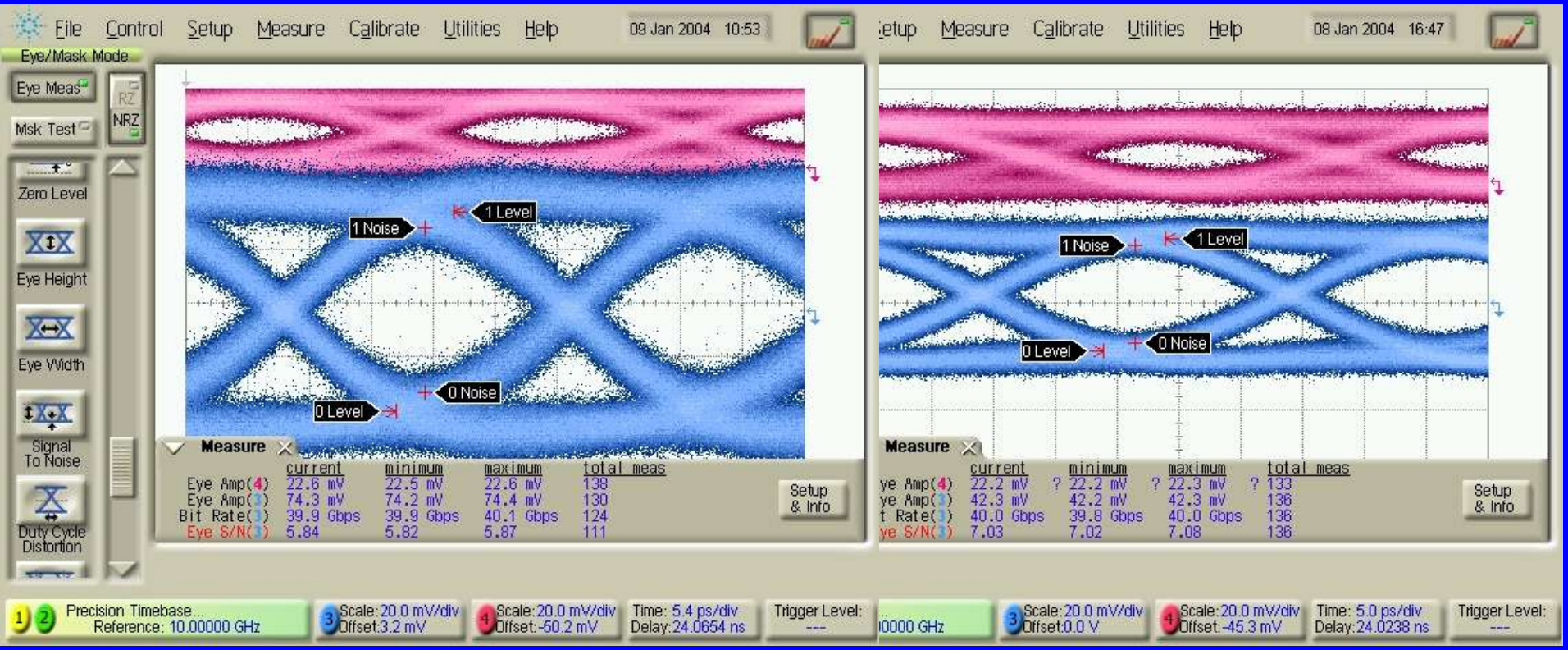
- Differential versions of three circuits implemented
- Measured single-ended noise figure in 50 Ohm



TIA has low noise over entire measured bandwidth

40-Gb/s eye diagrams

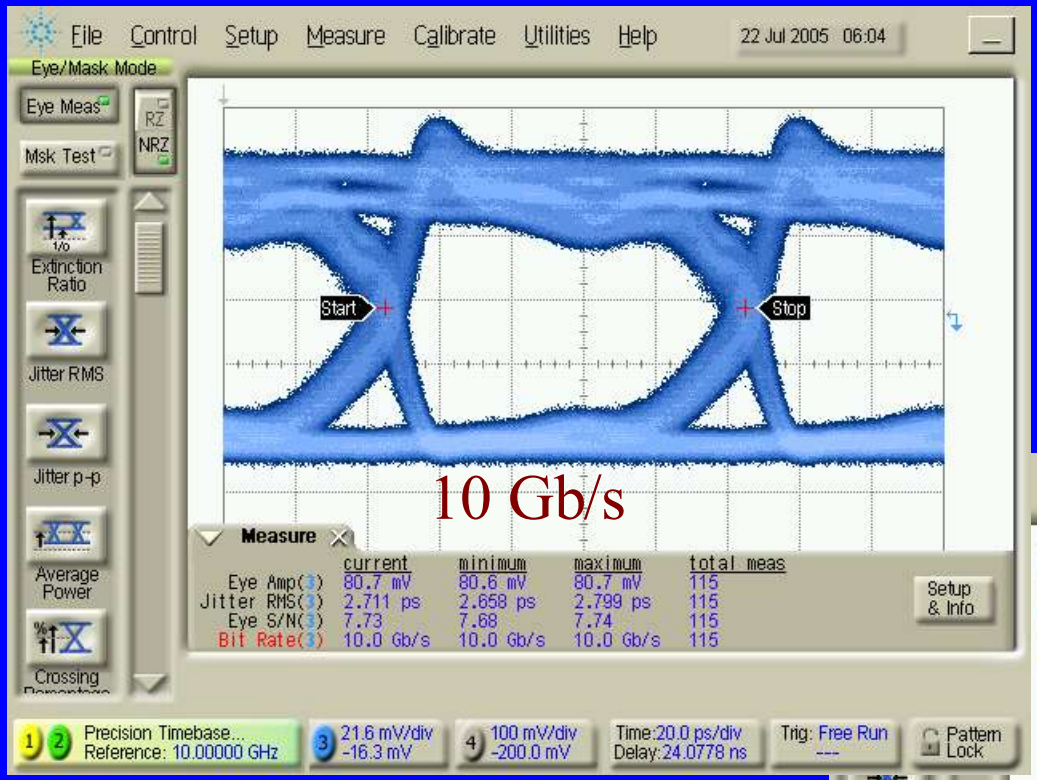
20-mV single-ended input (10-mV per side)

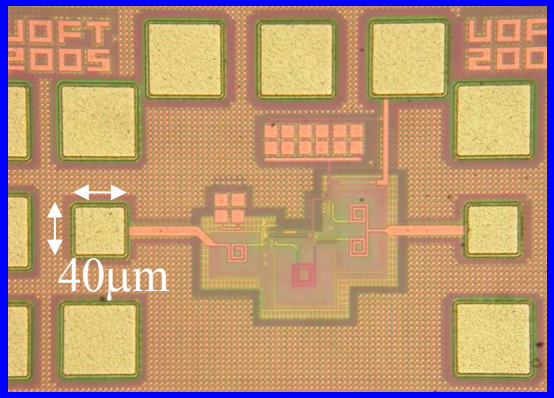


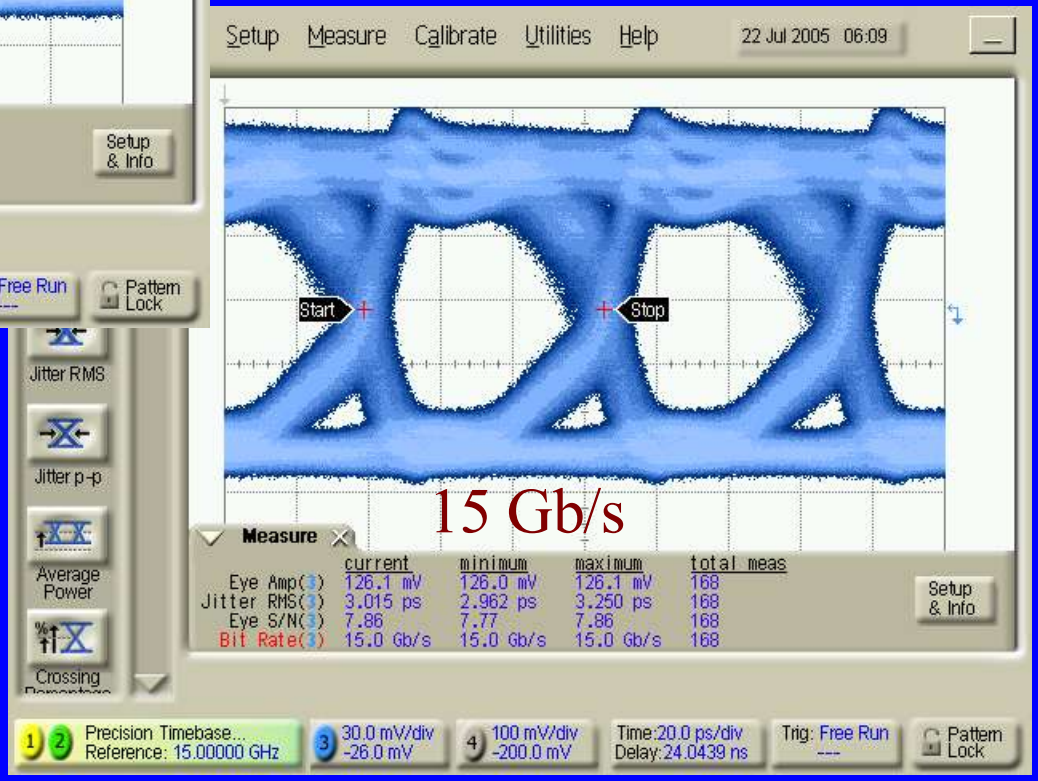
EF-INV **TIA**

Eye quality better for TIA (7.0) than EF-INV (5.8)

90-nm SOI TIA







- 8-dB noise figure
- 1V supply
- 6 mW
- p-MOS load

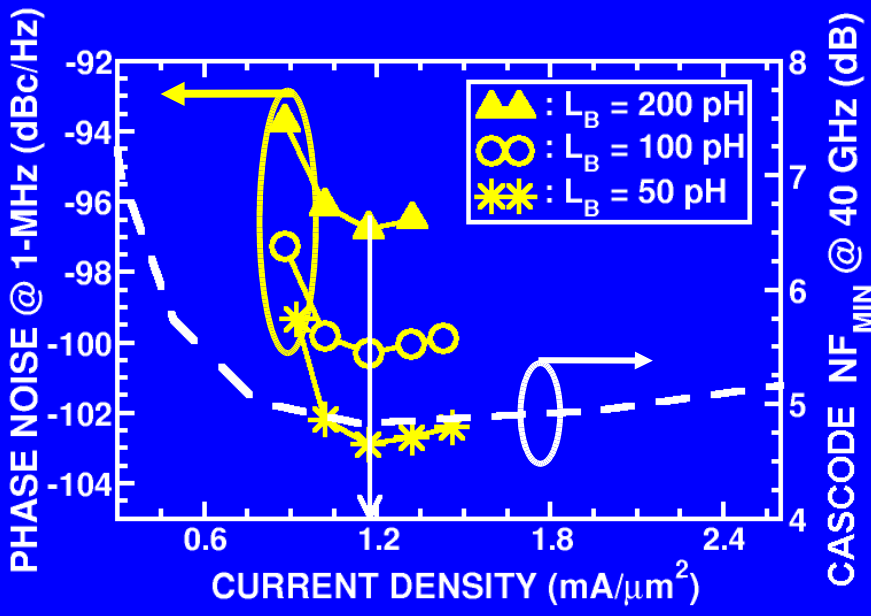
VCOs

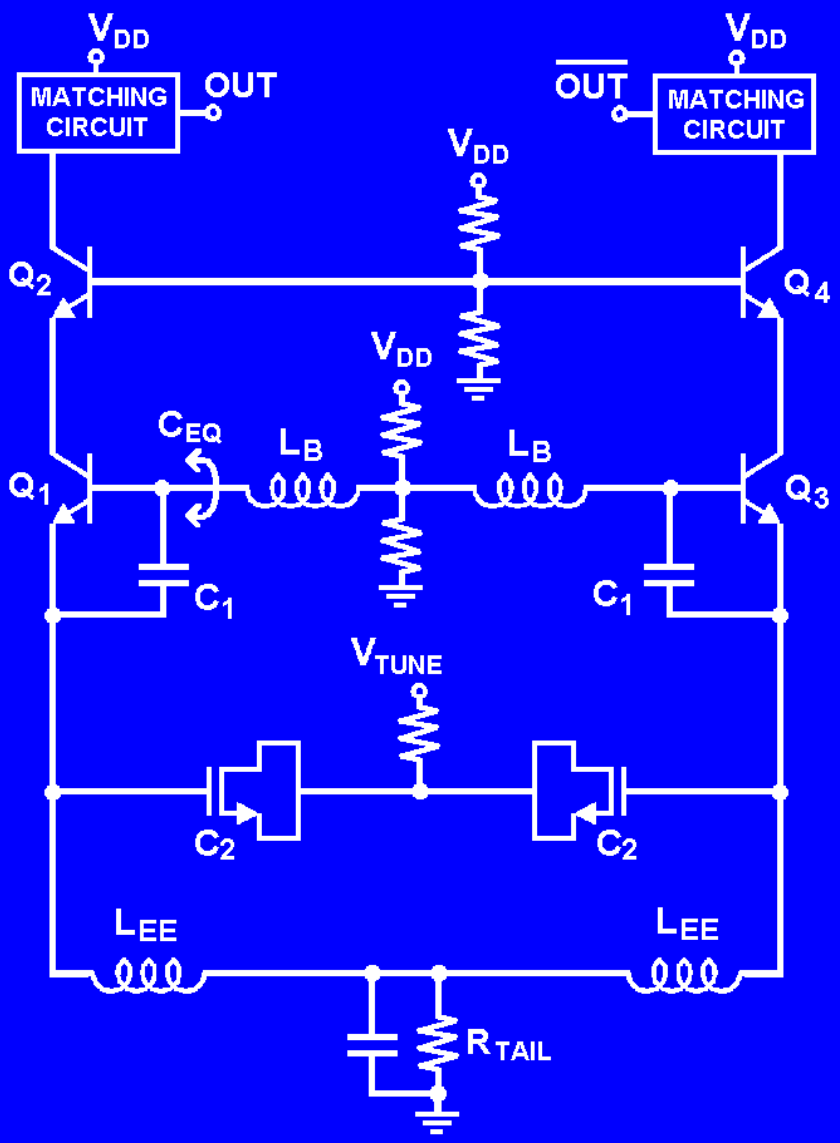
HBT VCOs

- Differential Colpitts topology

$$\text{Neg. Res.} = R_b - \frac{g_m}{\omega^2 C_1 C_2}$$

$$f_{osc} = \frac{1}{2\pi\sqrt{L_B C_{EQ}}}, \quad C_{EQ} = \frac{C_1 C_2}{C_1 + C_2}$$

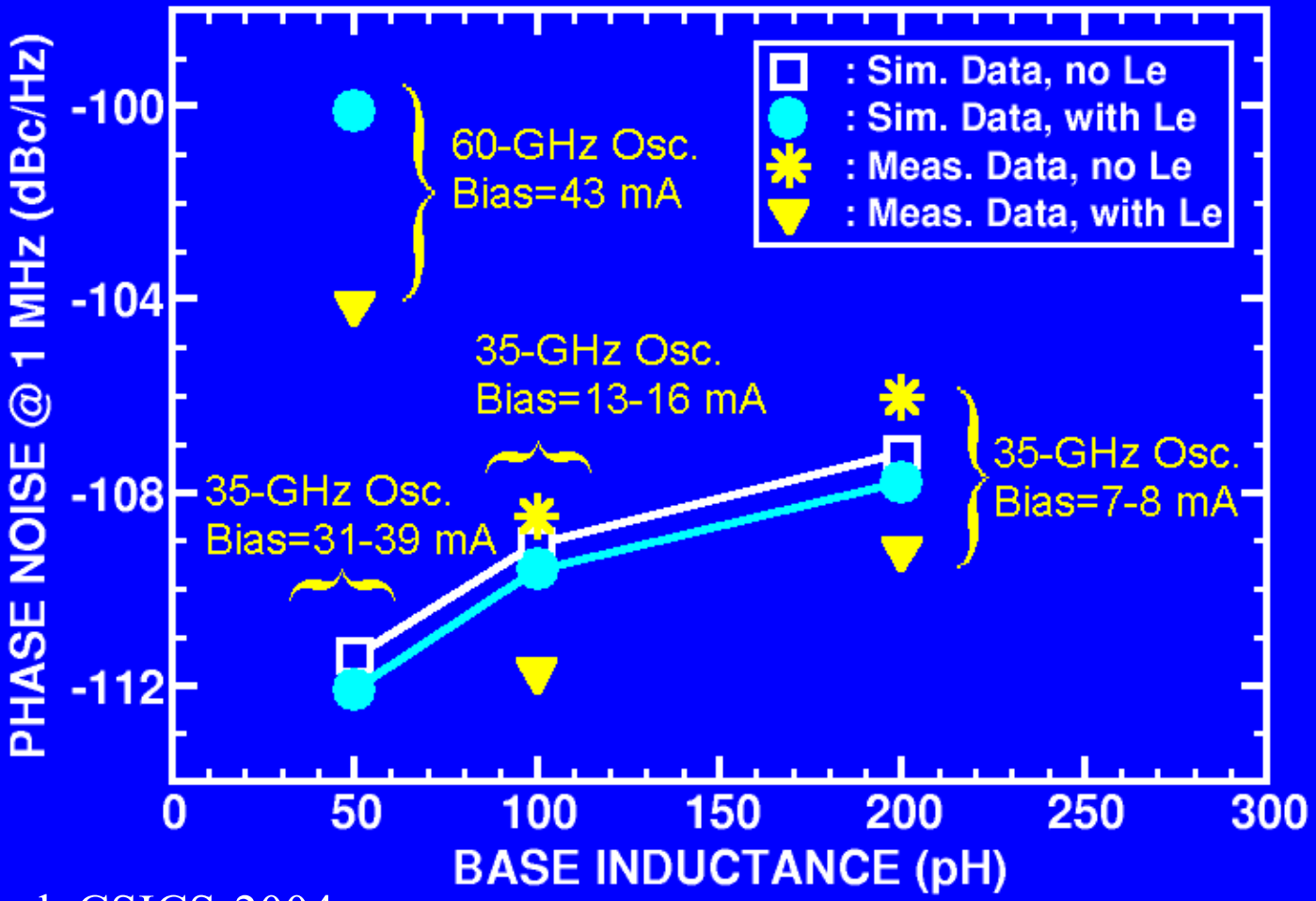




SiGe HBT oscillator measurements

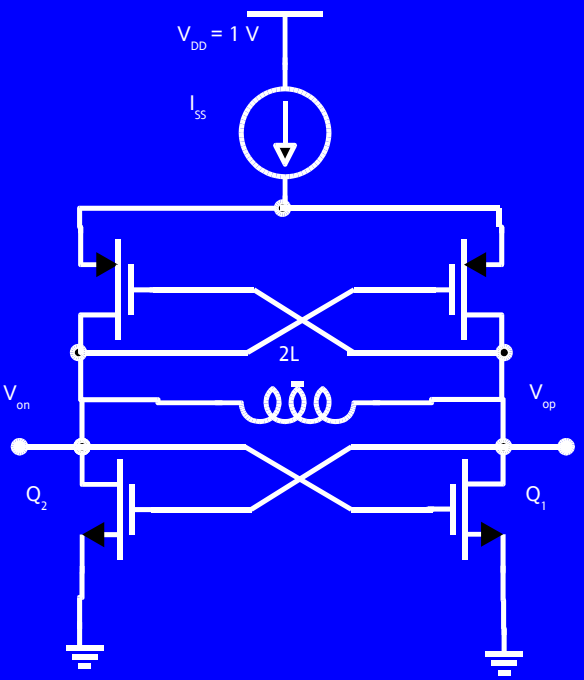
Impact of: 1. base (tank) inductor

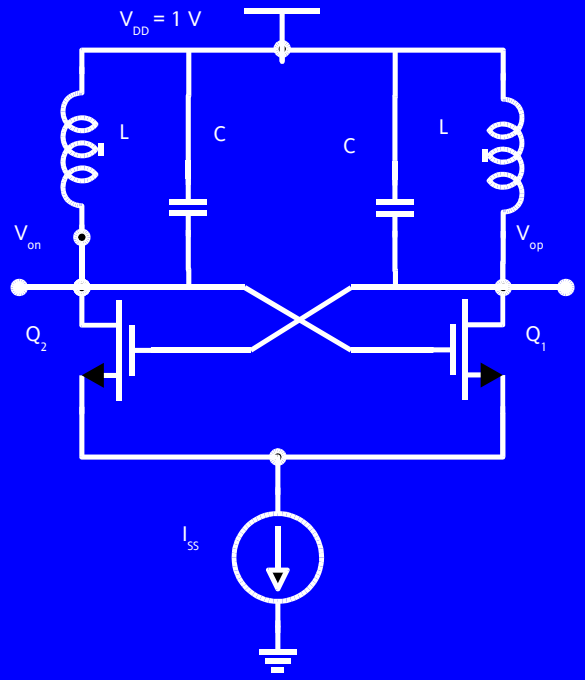
2. inductive emitter degeneration (L_E)



C. Lee et al. CSICS-2004

CMOS VCOs



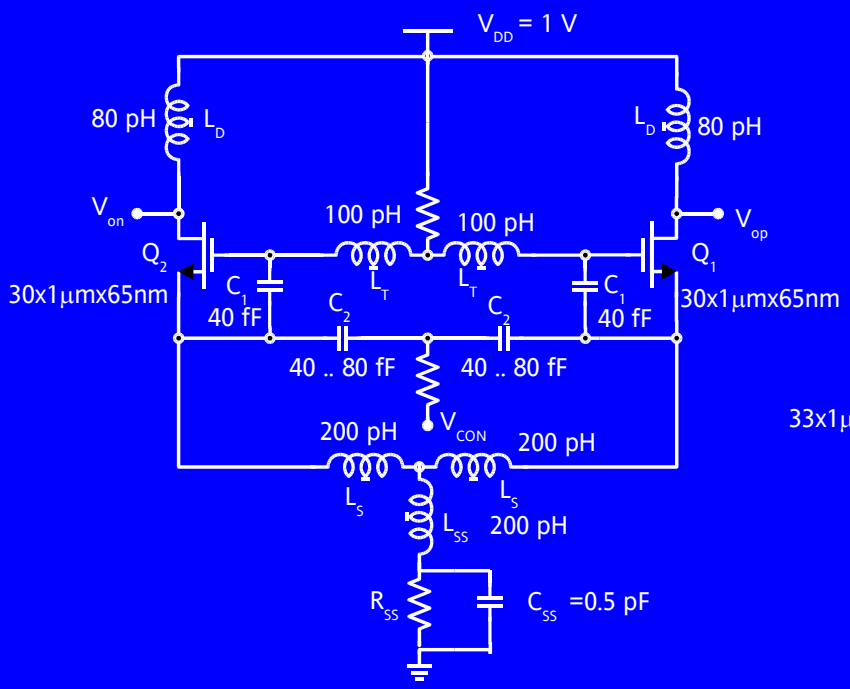


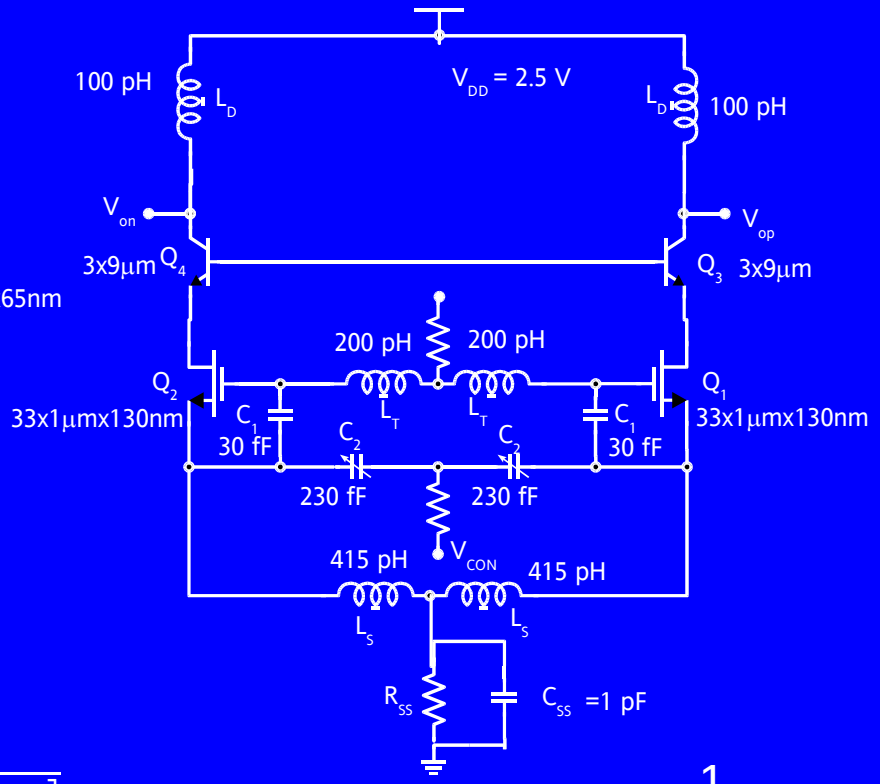
$$\omega_{osc,CMOS} \leq \frac{2}{3} \frac{g'_m Q_{eff}}{C'_{gs} + 4C'_{gd} + C'_{db} + \frac{C_L}{W}}$$

$$\omega_{osc,n-MOS} \leq \frac{g'_m Q_{eff}}{C'_{gs} + 4C'_{gd} + C'_{db} + \frac{C_L}{W}}$$

$$W_{n-MOS,cross} \leq \frac{1}{\omega_{osc}^2 L \left[C'_{gs} + 4C'_{gd} + C'_{db} \right]}$$

Colpitts CMOS/BiCMOS VCOs



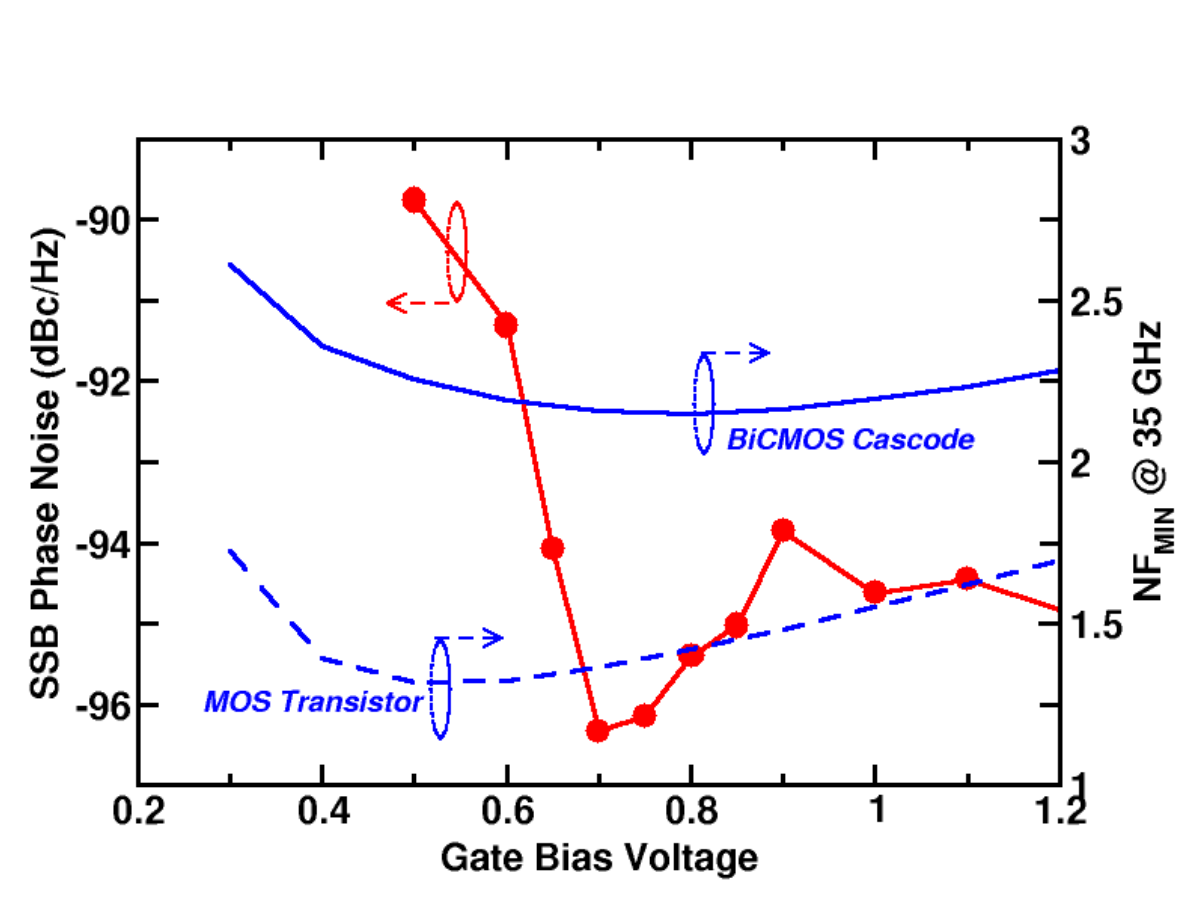


$$W_{n-MOS,\,Colpitts} \leq \frac{1}{\omega_{osc}^2 L \left[\frac{C'_{gs} C'_{sb}}{C'_{gs} + C'_{sb}} + k C'_{gd} \right]}$$

$$A_{E,\,HBT,\,Colpitts} \leq \frac{1}{\omega_{osc}^2 L \left[\frac{C_{jbA} \frac{C_{var}}{A_E}}{C'_{jbA} + \frac{C_{var}}{A_E}} + k C_{jcA} \right]}$$

Colpitts has higher f_{OSC} and built-in buffering over X-coupled

BiCMOS cascode oscillator measurements

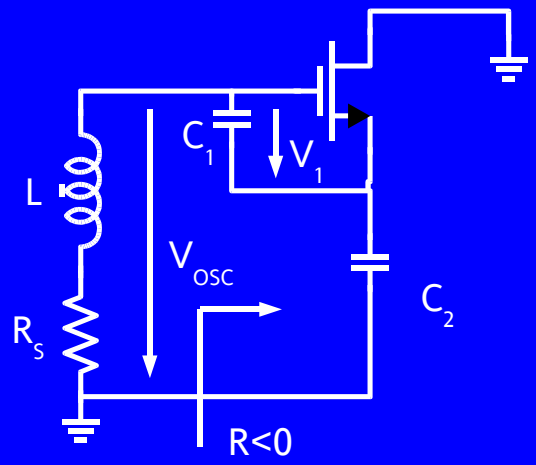


- Measured phase noise at 35 GHz and simulated NF_{MIN} of SiGe MOS-HBT cascode stage as a function of gate voltage

VCO design methodology

VCOs treated as LNAs matched to the "source" impedance R_p. This is generally not possible in cross-coupled VCOs!

- VCO topology (CS/CE or cascode) biased at optimum NF_{MIN} current density (0.15 mA/μm in FETs)
- V_{osc} must be set close to V_{MAX} to minimize phase noise
- Lower inductance, higher bias current, better L(f_m)
  - HBT-VCOs have 6..10 dB better phase noise due to larger V_{MAX}



$$L(f_m) = \frac{|I_n|^2}{V_{osc}^2} \times \frac{1}{f_m^2} \times \frac{1}{C_1^2\left(\frac{C_1}{C_2}+1\right)^2}$$

High-Speed Logic

Logic families

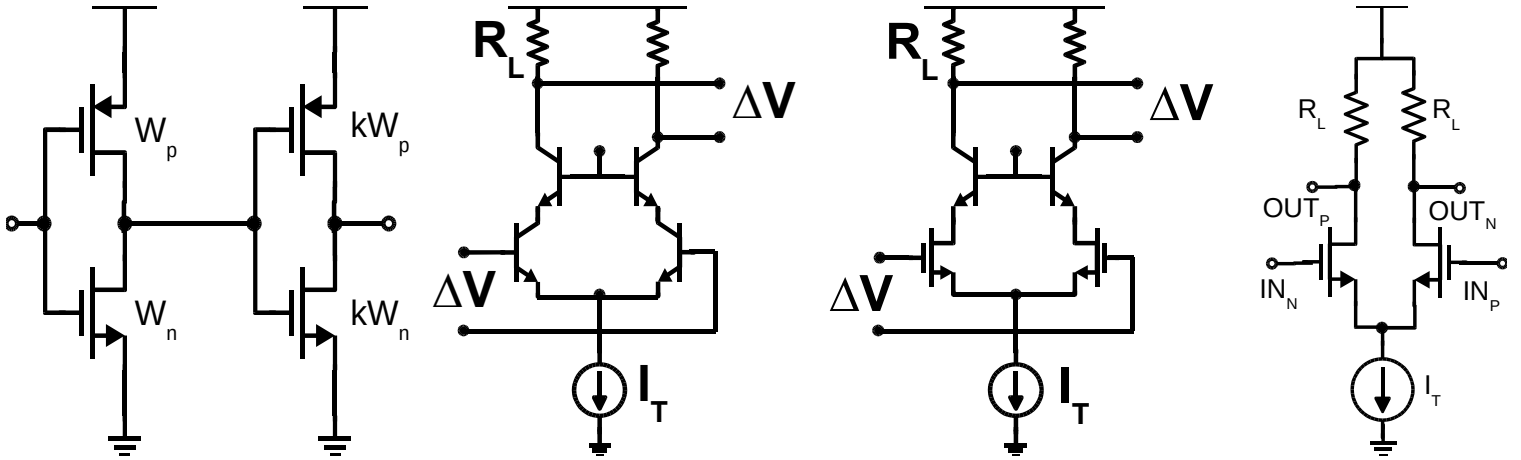
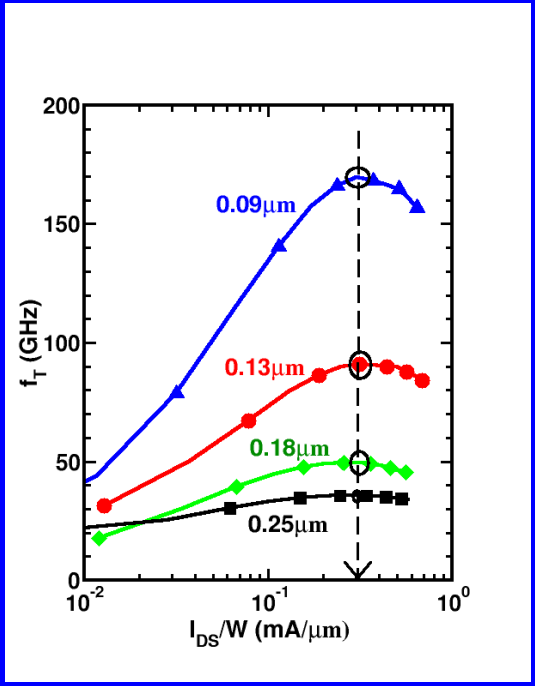
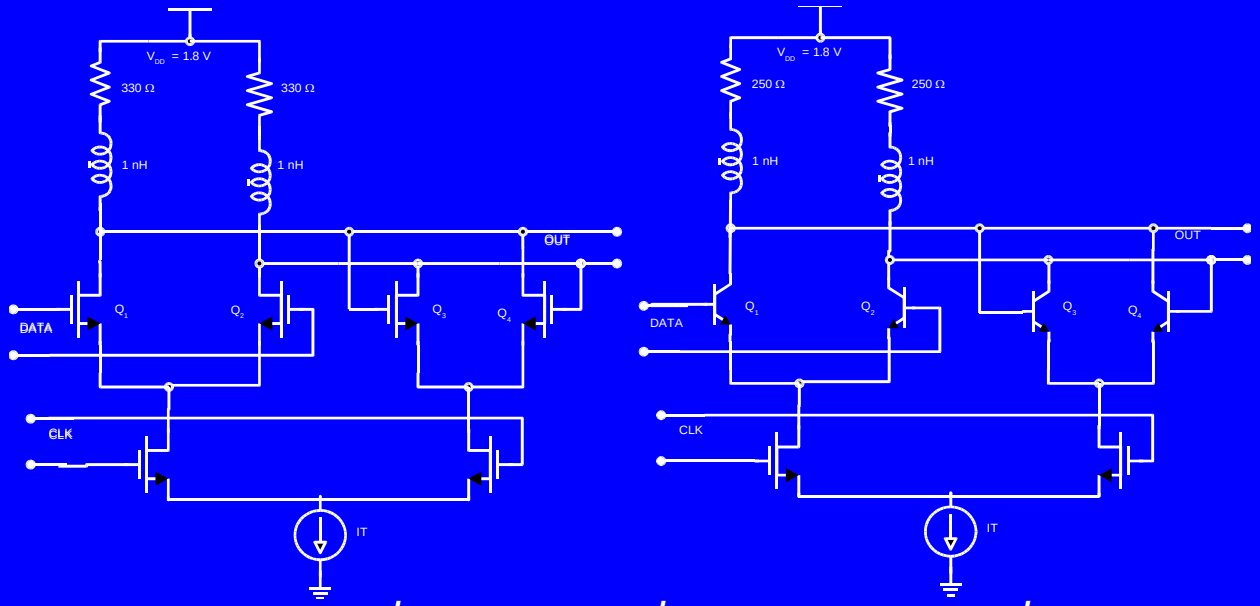


Fig. 9. Inverters in various CMOS and SiGe BiCMOS logic families.

- Unlike conventional CMOS, gate & subthreshold leakage is not a problem in MOS-CML
- In MOS-CML *low-*V_T is desirable
- MOS-CML with peaking is > 3x faster than CMOS

MOS/BiCMOS CML device sizing & biasing





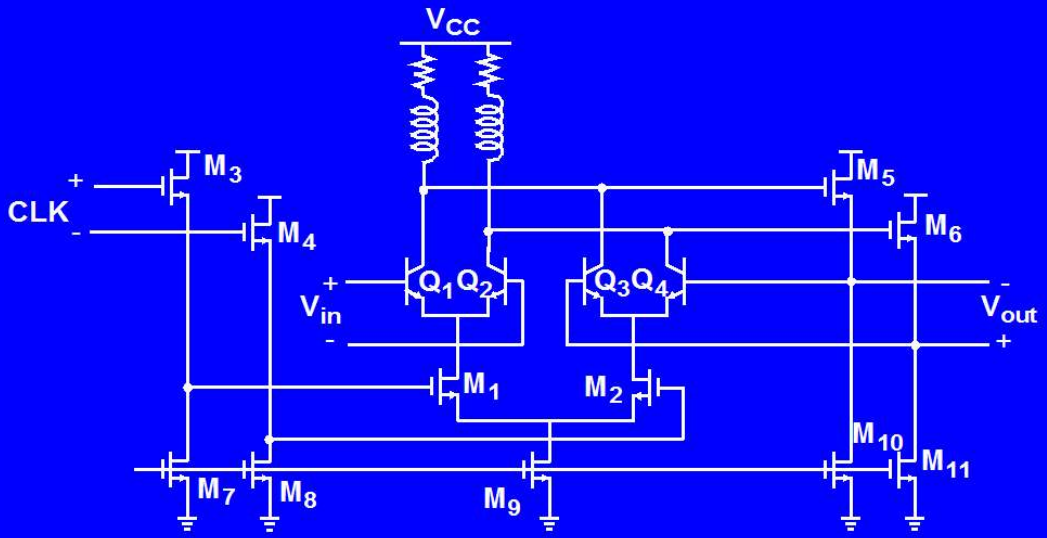
$\sqrt{2}V_{eff} \le \Delta V \le 2V_{eff}$ scales with L

$$W = \frac{I_T}{1.5J_{peakfMAX}} = \frac{I_T}{0.3mA/\mu m}; \quad A_E = \frac{I_T}{1.5J_{peakfMAX}}$$

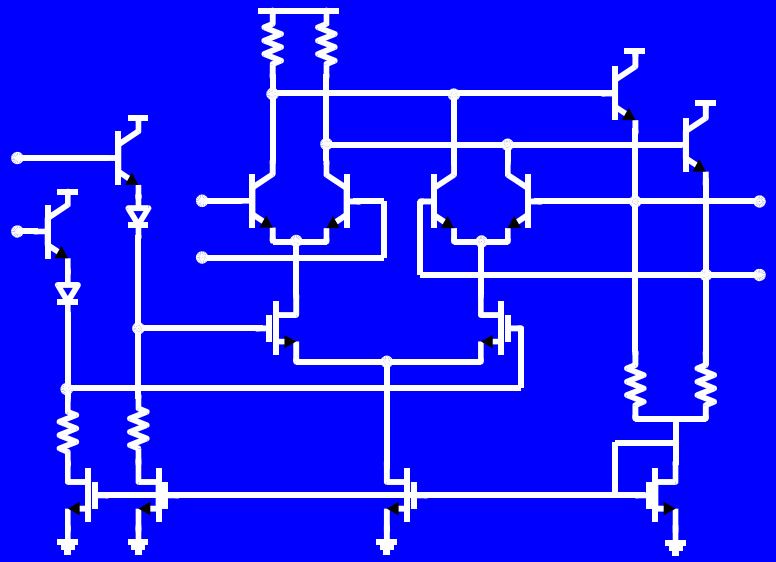
$$L_p = \frac{C_L R_L^2}{3.1} \qquad L_p = \frac{C_L}{3.1}\frac{\Delta V^2}{I_T^2} \qquad BW_{3dB} = \frac{1.6 \times I_T}{2\pi \Delta V C_L} \qquad I_{Tmin} = \Delta V \sqrt{\frac{C_L}{3.1 L_{pmax}}}$$

- For a given speed and technology there is a maximum realizable L_{pmax}
- Speed improvement as CMOS scales is due solely to V_{eff} (ΔV) scaling.

BiCMOS ECL latches (> 49 GHz)



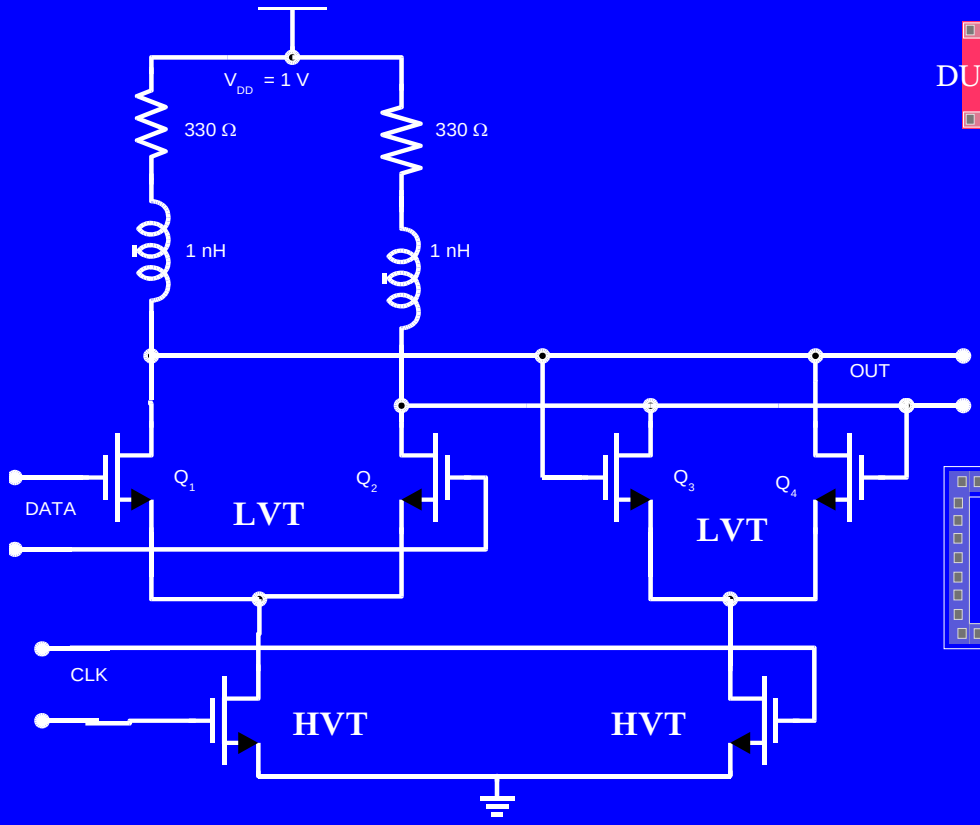
2.5 V supply, I_T=2 .. 4mA

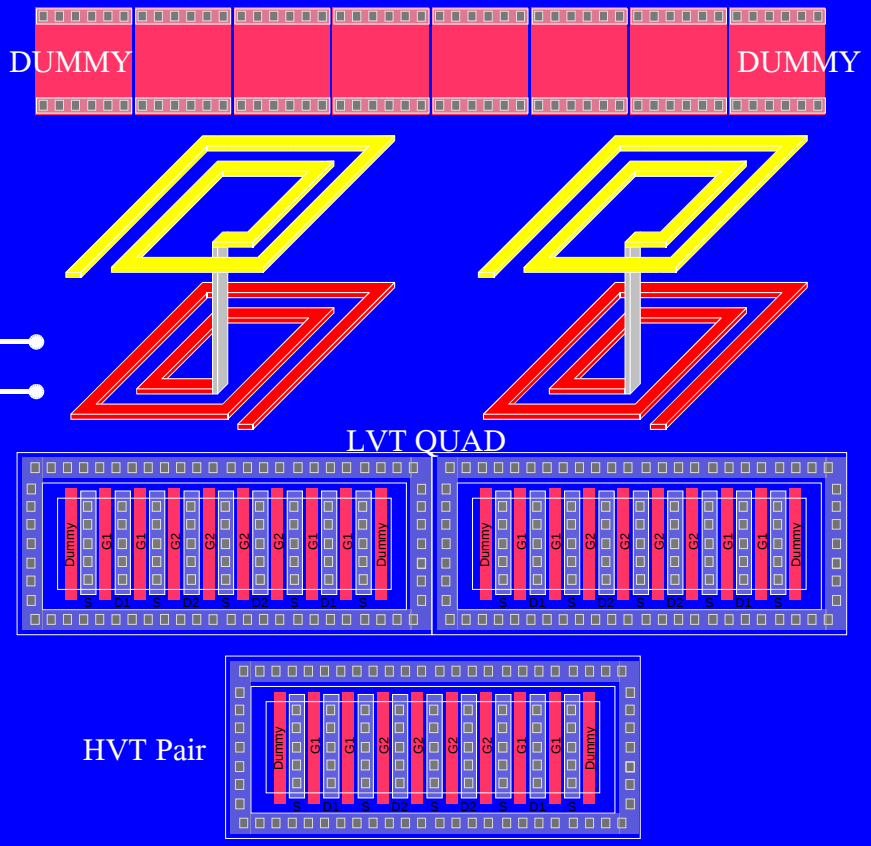


3.3 V supply, I_T=2 .. 4mA

- BiCMOS cascode with EF (SF)
- EF vs. SF:
  - higher gain, lower E-S capacitance
  - $V_{BE} > V_{GS}$

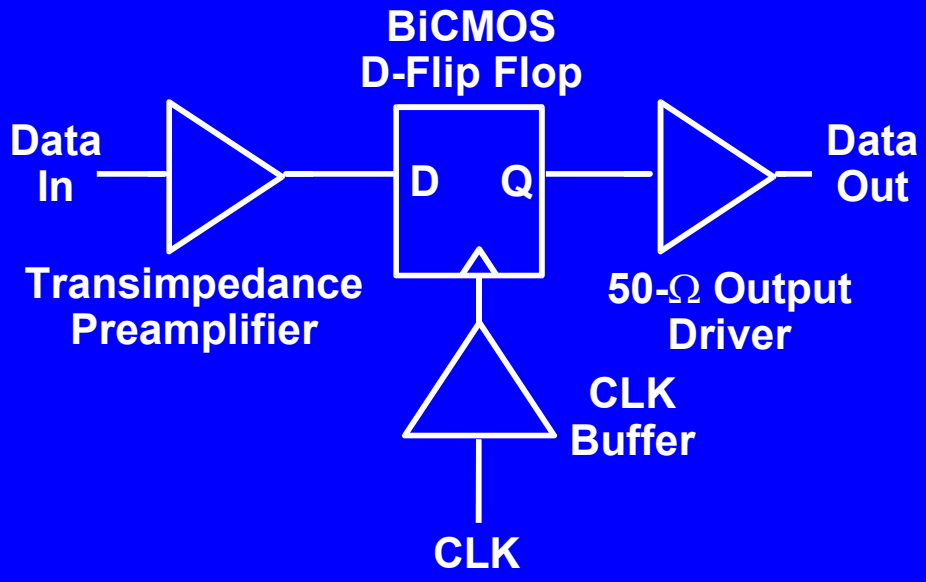
Evolution to 1-V, 40-GHz latch

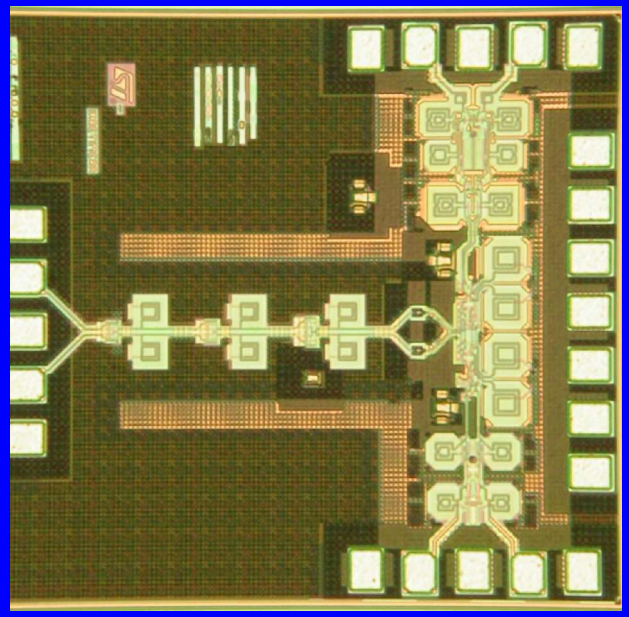


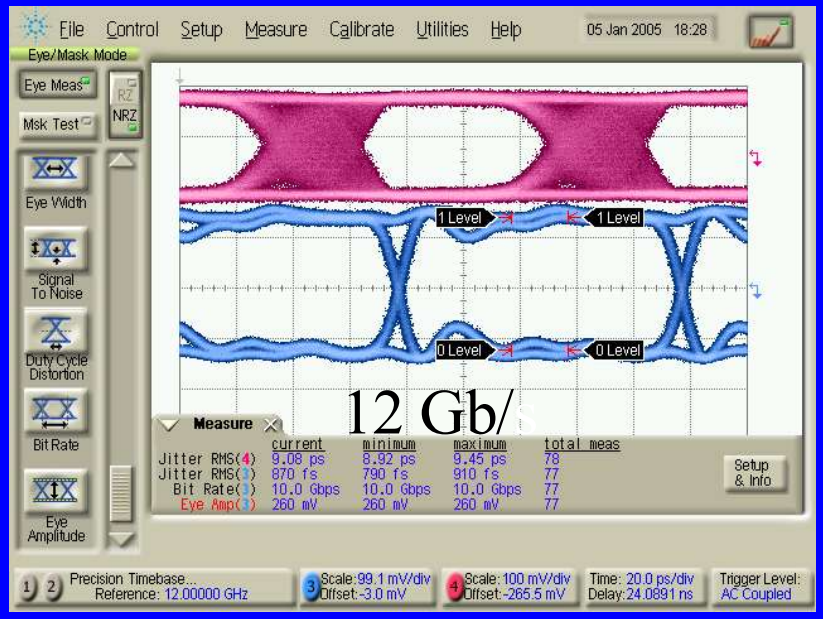


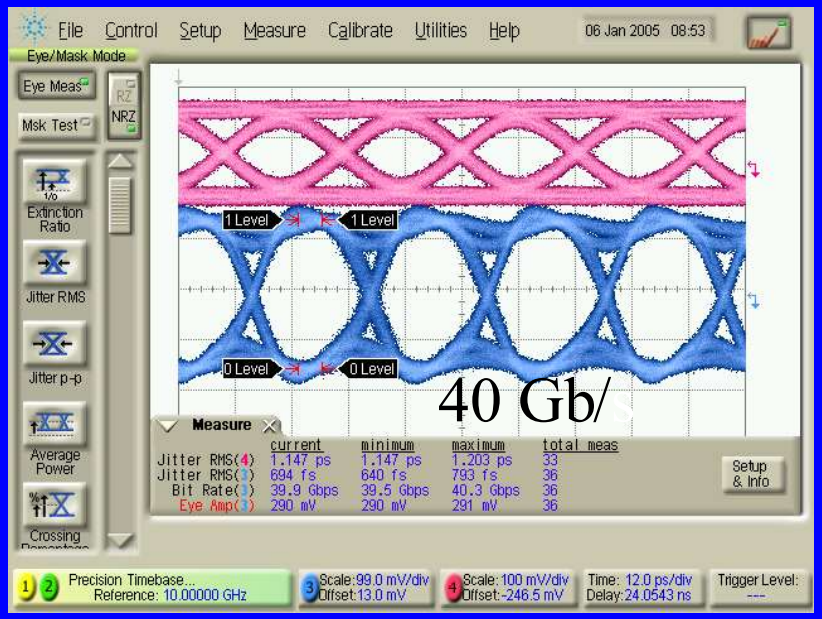
Wireline circuits beyond 40 Gb/s

2.5-V, Broadband 49-GHz MS DFF

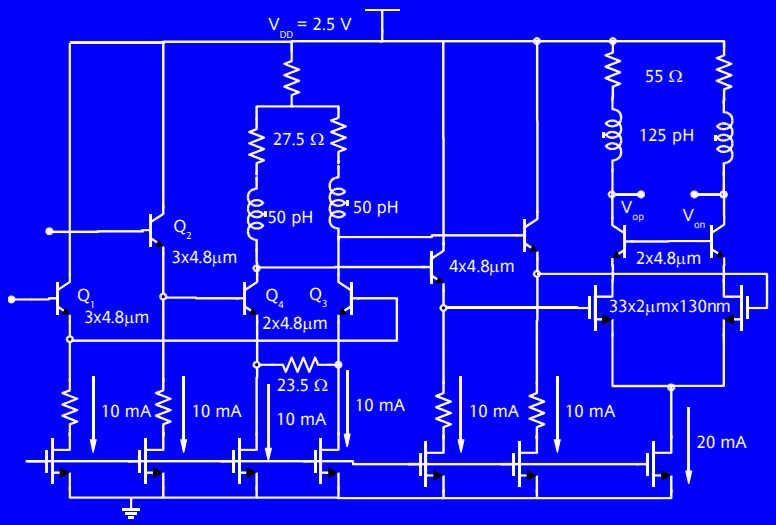




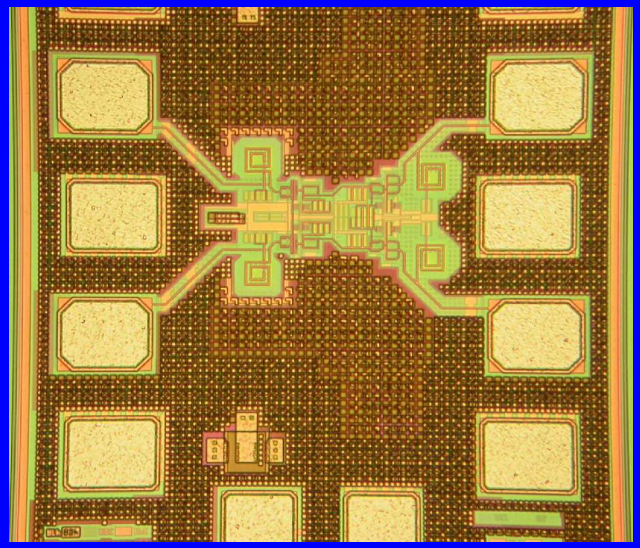


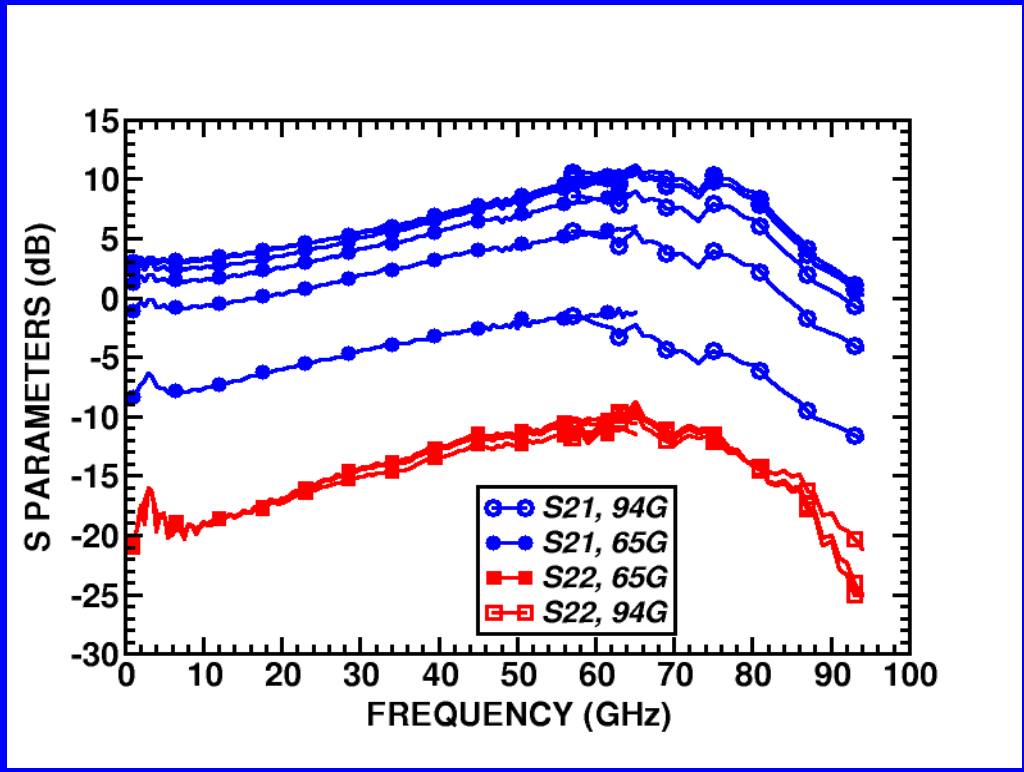


2.5-V, 80-GHz driver with pre-emphasis and gain control

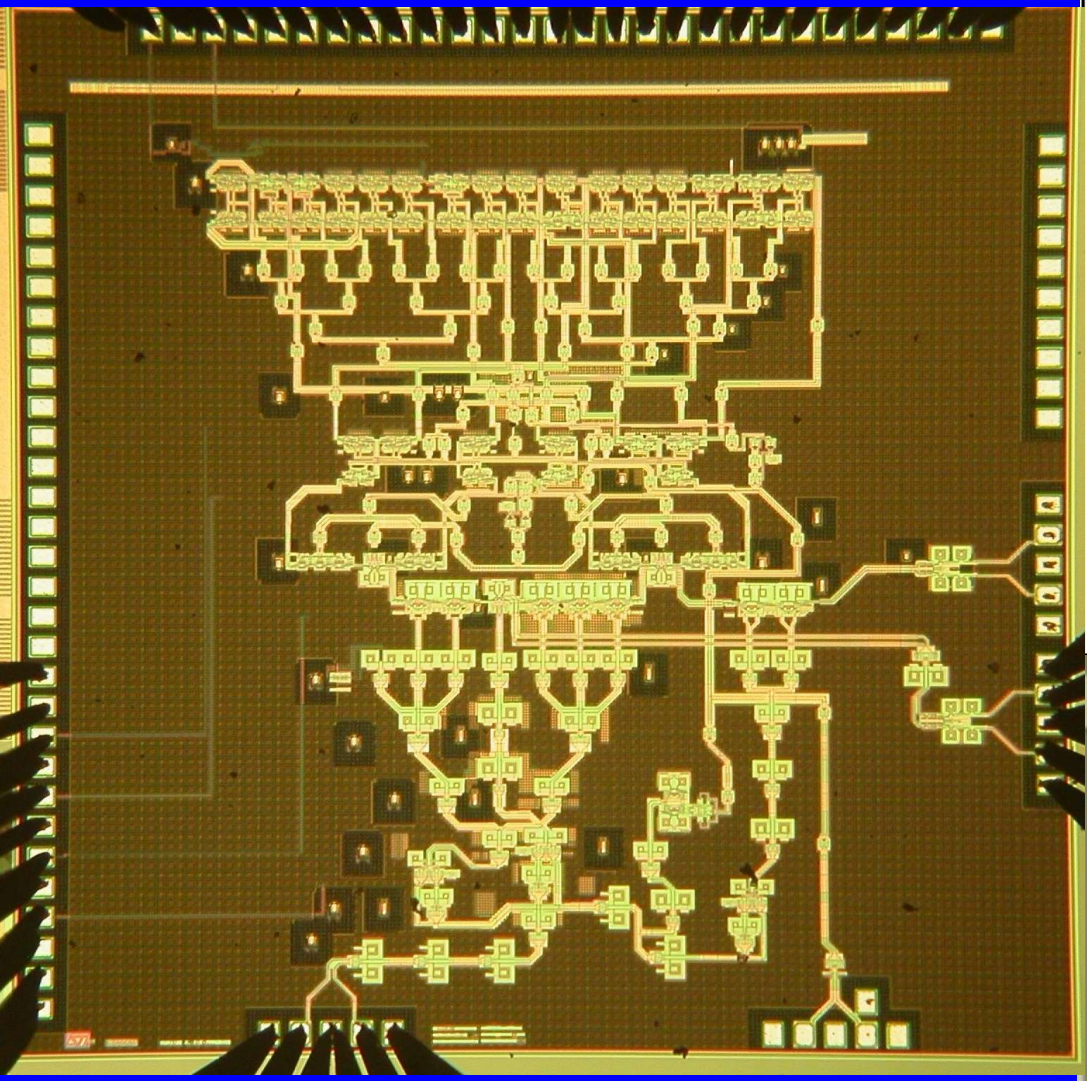


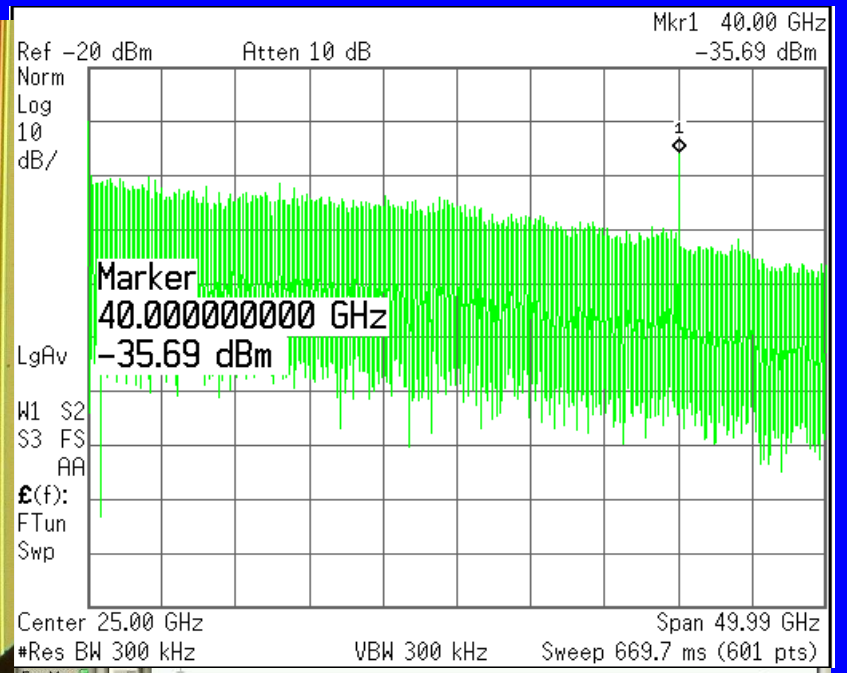
- Adjustable gain with peaking
- Gain > 0 dB @ 94 GHz
- S_{22}<-12 dB up to 94 GHz
- 130-nm MOS-HBT cascode

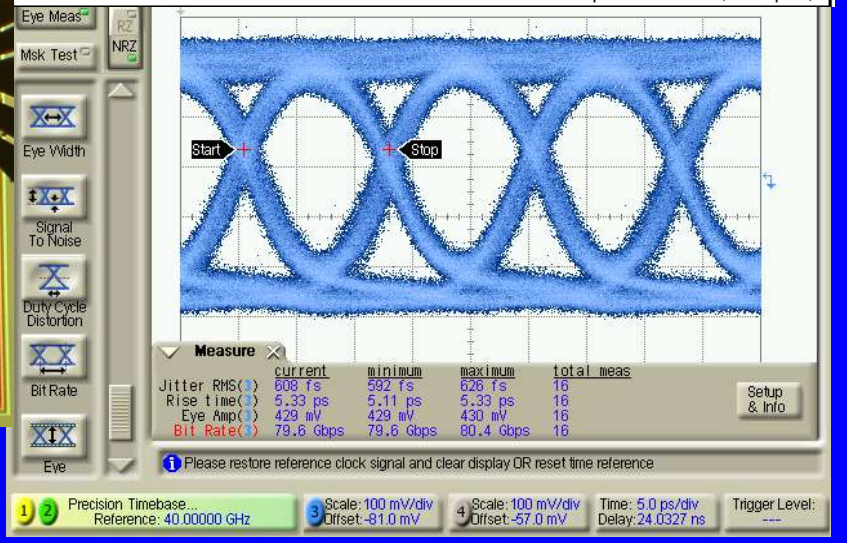




80-Gbs SiGe BiCMOS 2^{31}-1 PRBS Generator

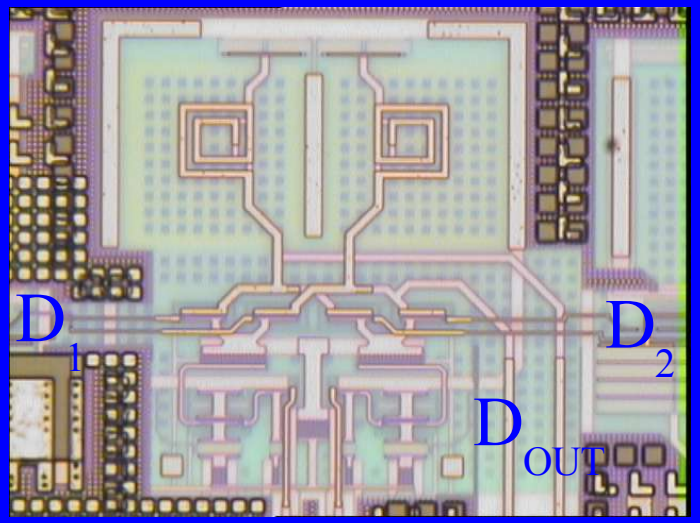




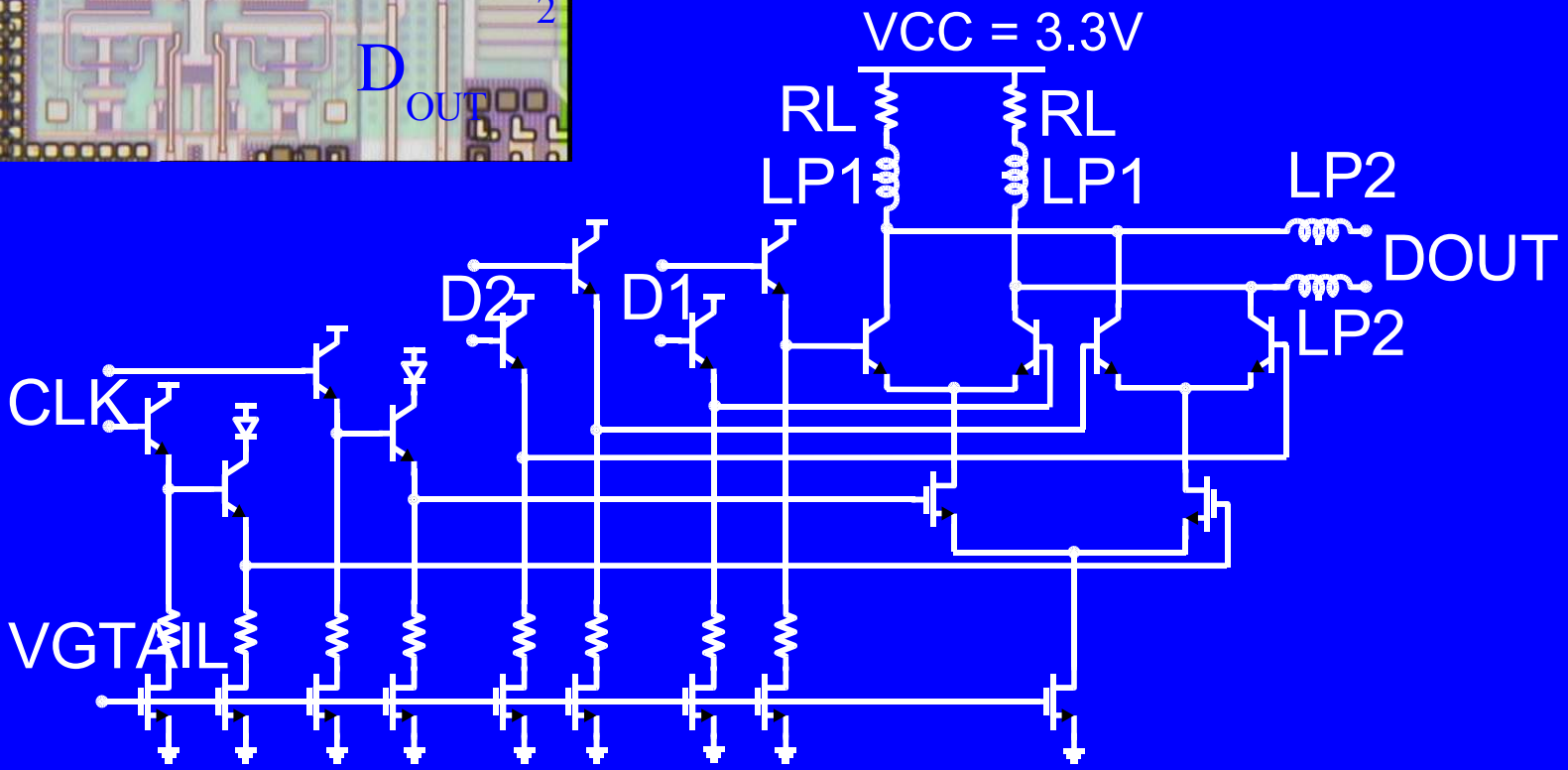


T. Dickson et al. ISSCC-2005

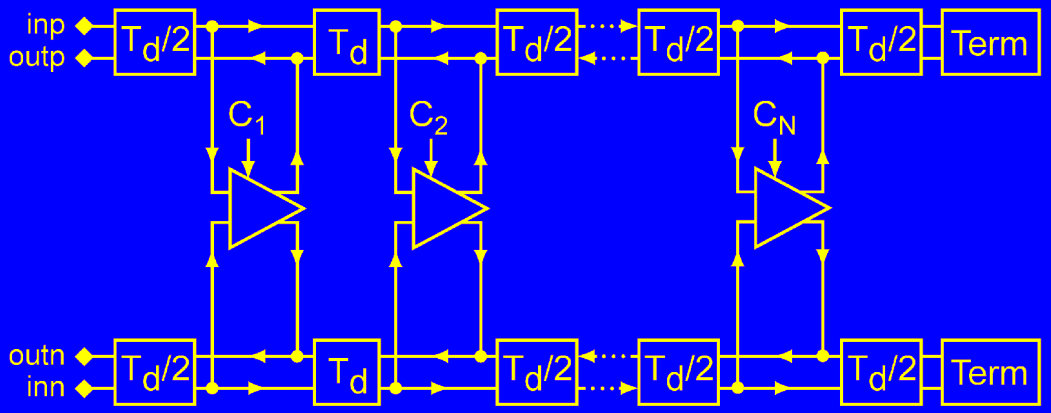
Selector: BiCMOS 80-Gb/s

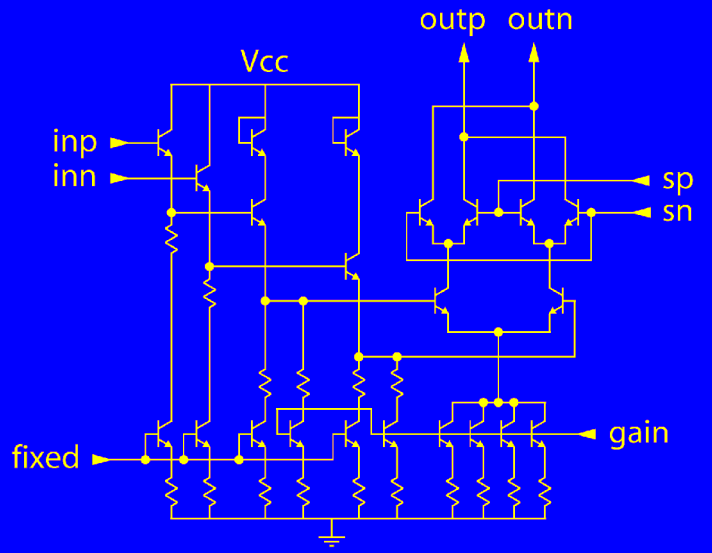


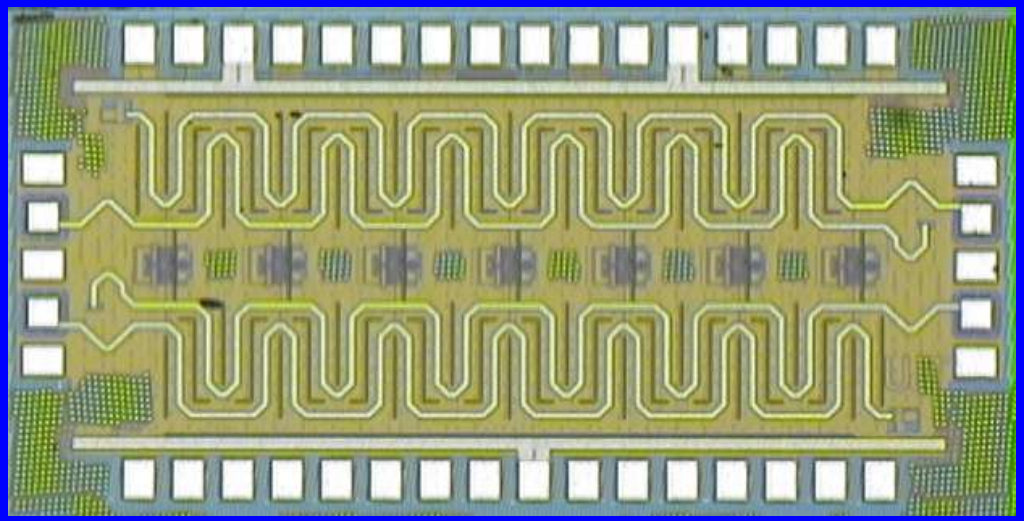
- EF^2 & series-shunt peaking for highest speed
- 3-D stacked inductor for reduced area and high SRF



40-Gb/s Feed Forward Equalizer



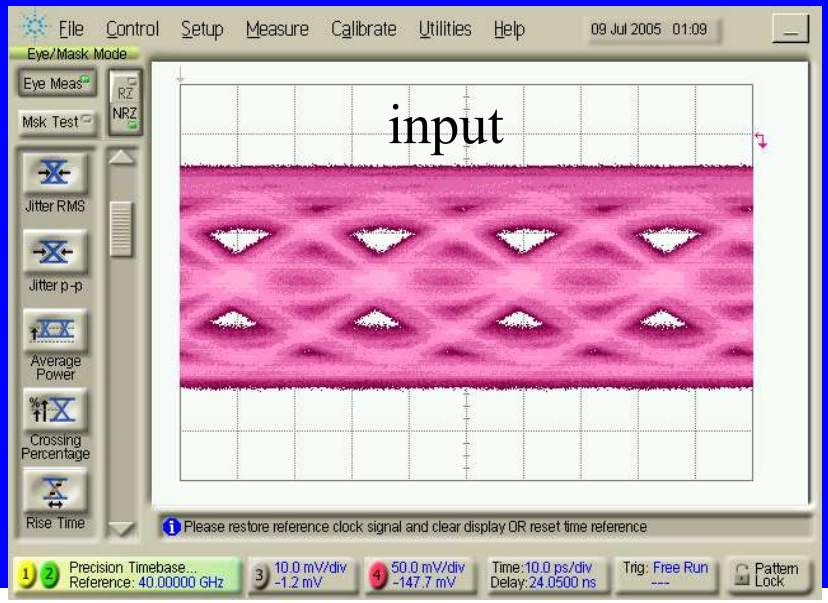


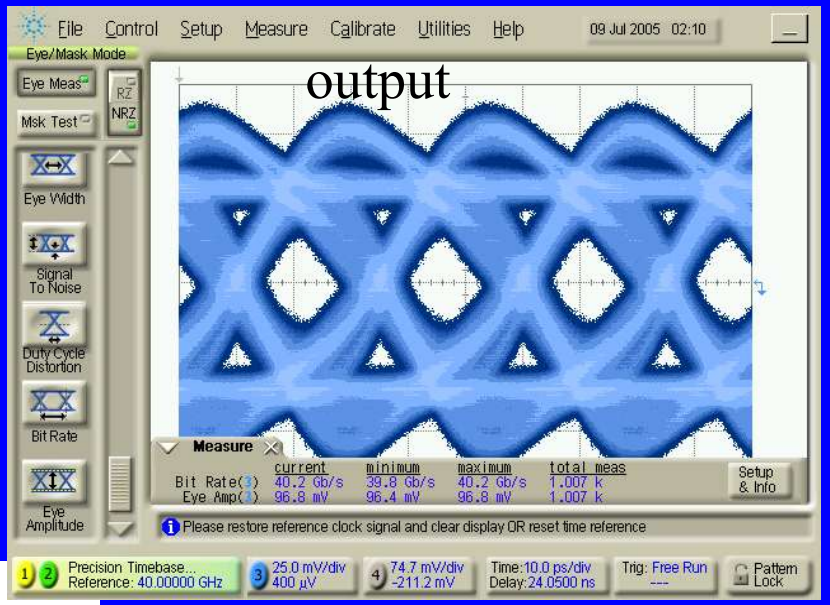


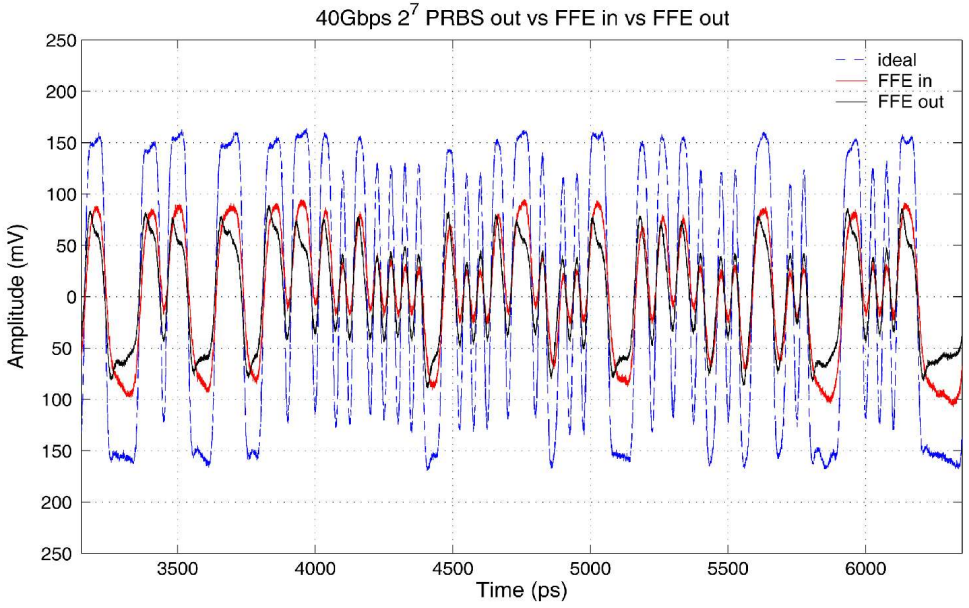
- core of each gain stage is a Gilbert cell
- tail current of the differential pair controls the tap weight (GAIN pad)
- SP/N pads control the tap sign

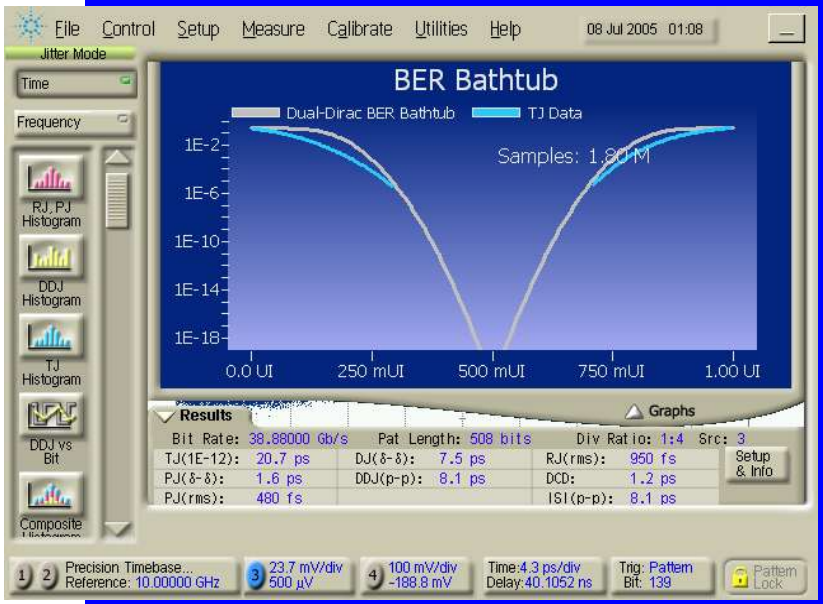
A. Hazneci et al. CSICS-2004

40 Gb/s over 9-ft SMA cable + 3dB attn.

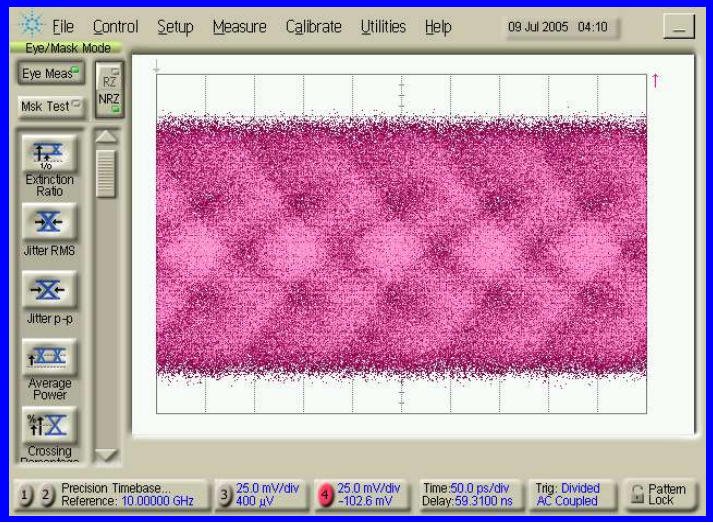


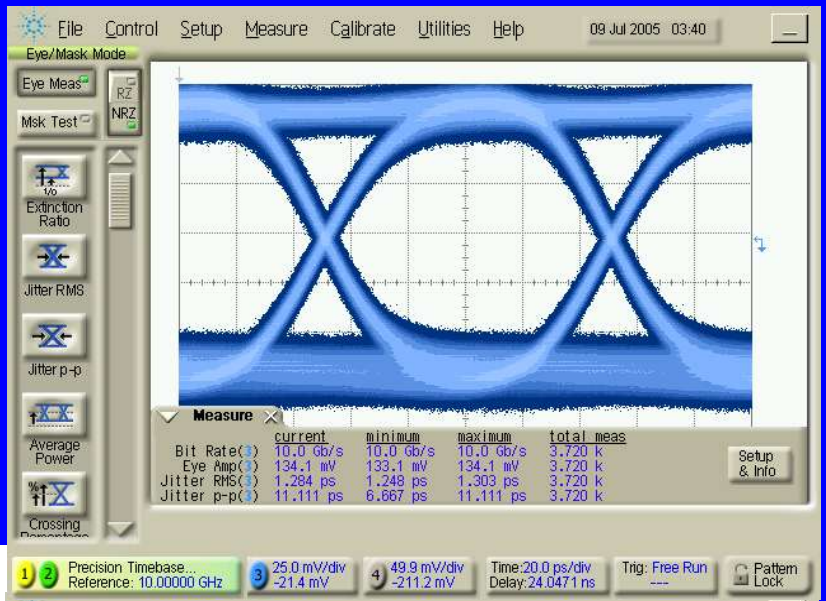


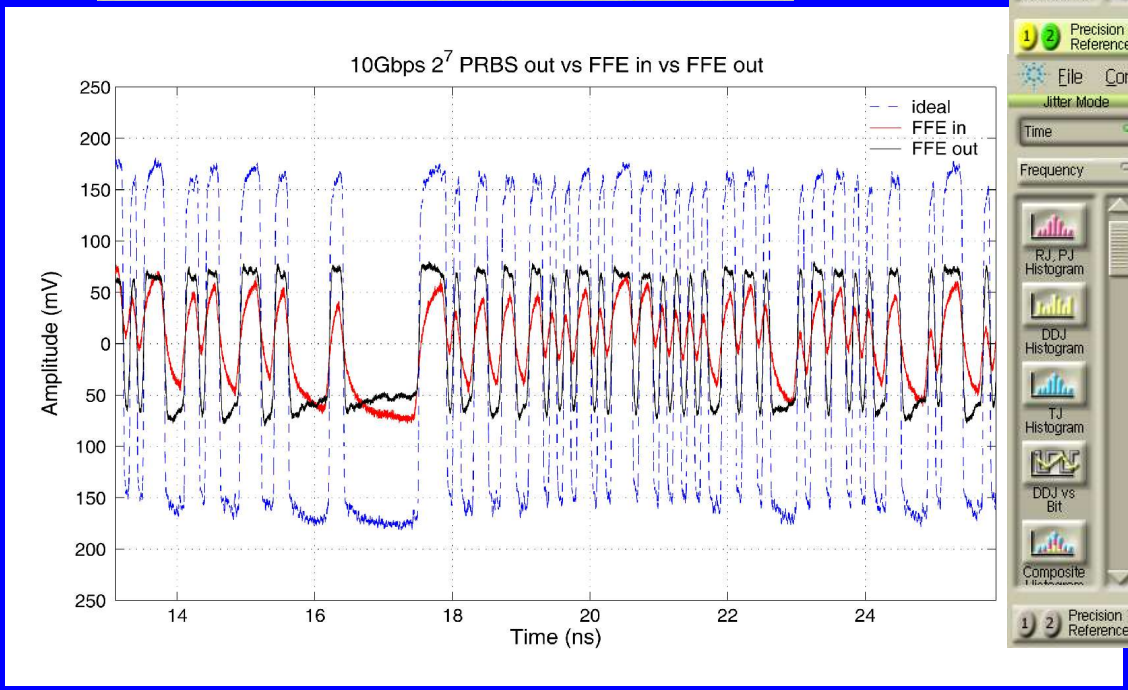


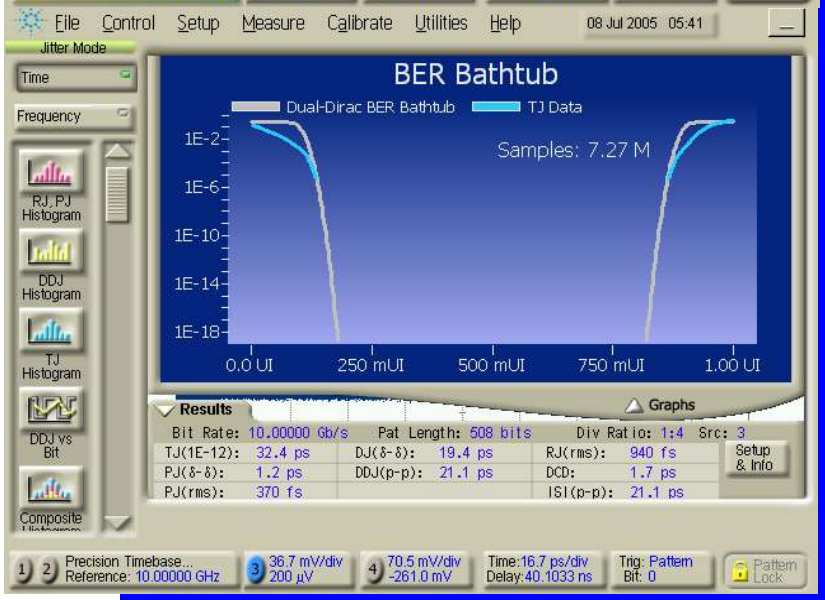


10 Gb/s equalization over 24-ft SMA cable +6dB attn.

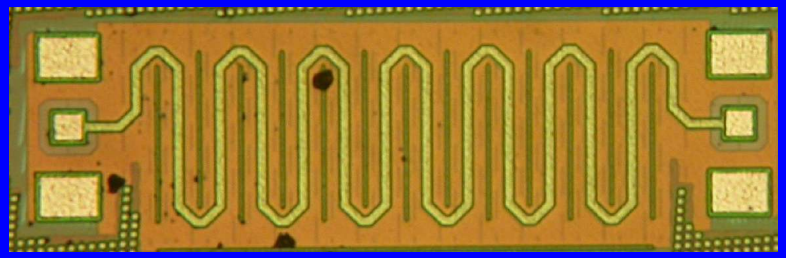




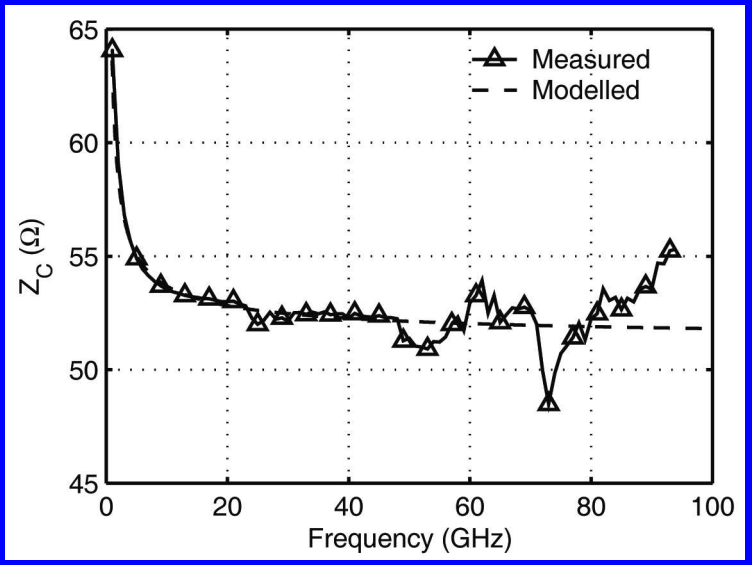


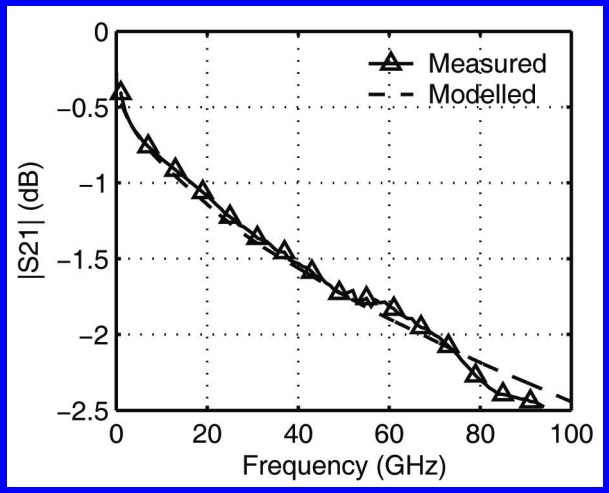


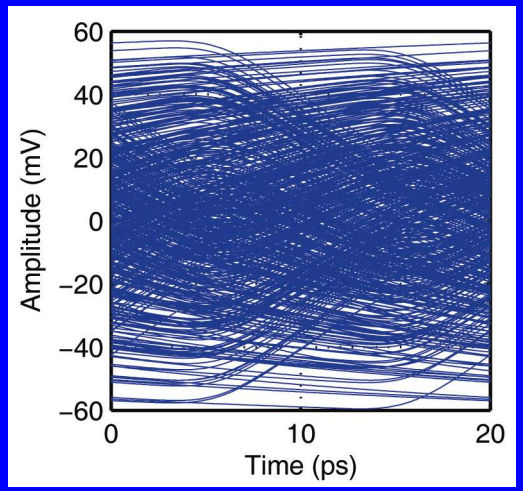
100-Gb/s transmission over 5cm of on-chip interconnect possible in 90nm SiGe BiCMOS

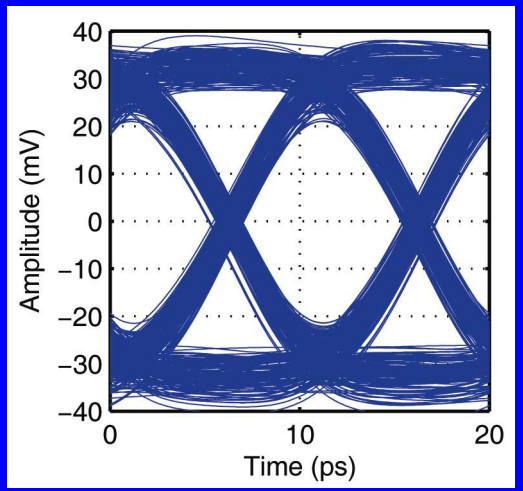


- Model extracted from meas. on 3.6-mm long line
- 7-tap FFE equalizer









Summary

- Key design ideas:
  - Optimal solutions exist for LNA, TIA, VCO, (Bi)CMOS-CML gate topologies
  - Biasing at minimum noise figure current density
  - Matching noise impedance to signal source (tank) impedance
- Key MOSFET circuit scaling ideas
  - FETs should be biased at constant current density
  - Circuit size and bias current invariant over nodes while performance improves with scaling
- Circuits in the 50-80 GHz range
- Sub-3W, 100 Gb/s Ethernet transceiver possible in 250-GHz, 90-nm SiGe BiCMOS technology

Acknowledgments

- Bernard Sautreuil for his support over many years
- STMicroelectronics for fabrication
- Micronet, NSERC, Gennum Corporation and STMicroelectronics for financial support
- OIT and CFI for equipment grant
- CMC for CAD licenses

Backup

Impact of scaling in deep-submicron MOSFETs (500nm to 50nm)

- As a result of the constant-field scaling rules being applied to every new CMOS technology node:
  - Voltages scale by factor *S*
  - Vertical & lateral electric fields remain constant
  - Charge per unit gate width and current per unit gate width remain constant
  - The classical MOSFET *I-V* square law remains valid only at very low V_{eff} beyond which it becomes linear

Mobility degradation

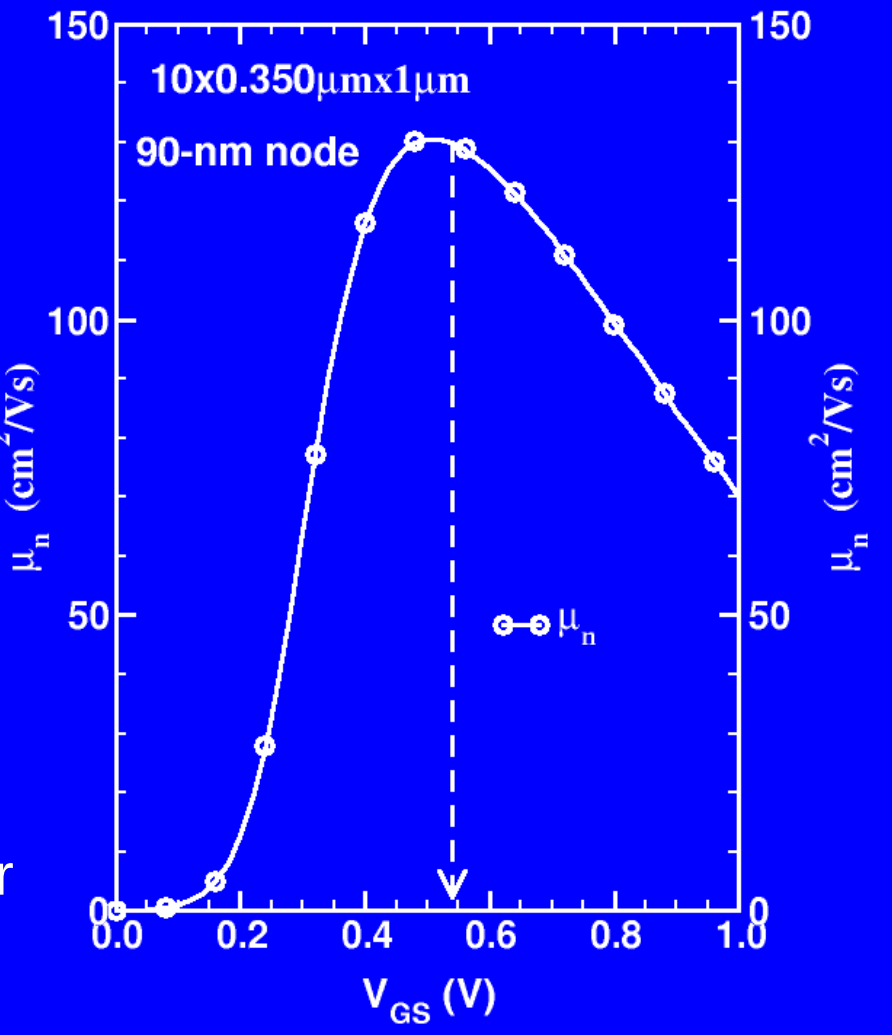
- Mobility degradation due to the vertical gate field dominates behaviour (based on Intel data, S. Thompson, IEDM'99 Short Course).

$$\mu_{eff} = \frac{\mu_{ac}\,\mu_{sr}}{\mu_{ac} + \mu_{sr}}$$

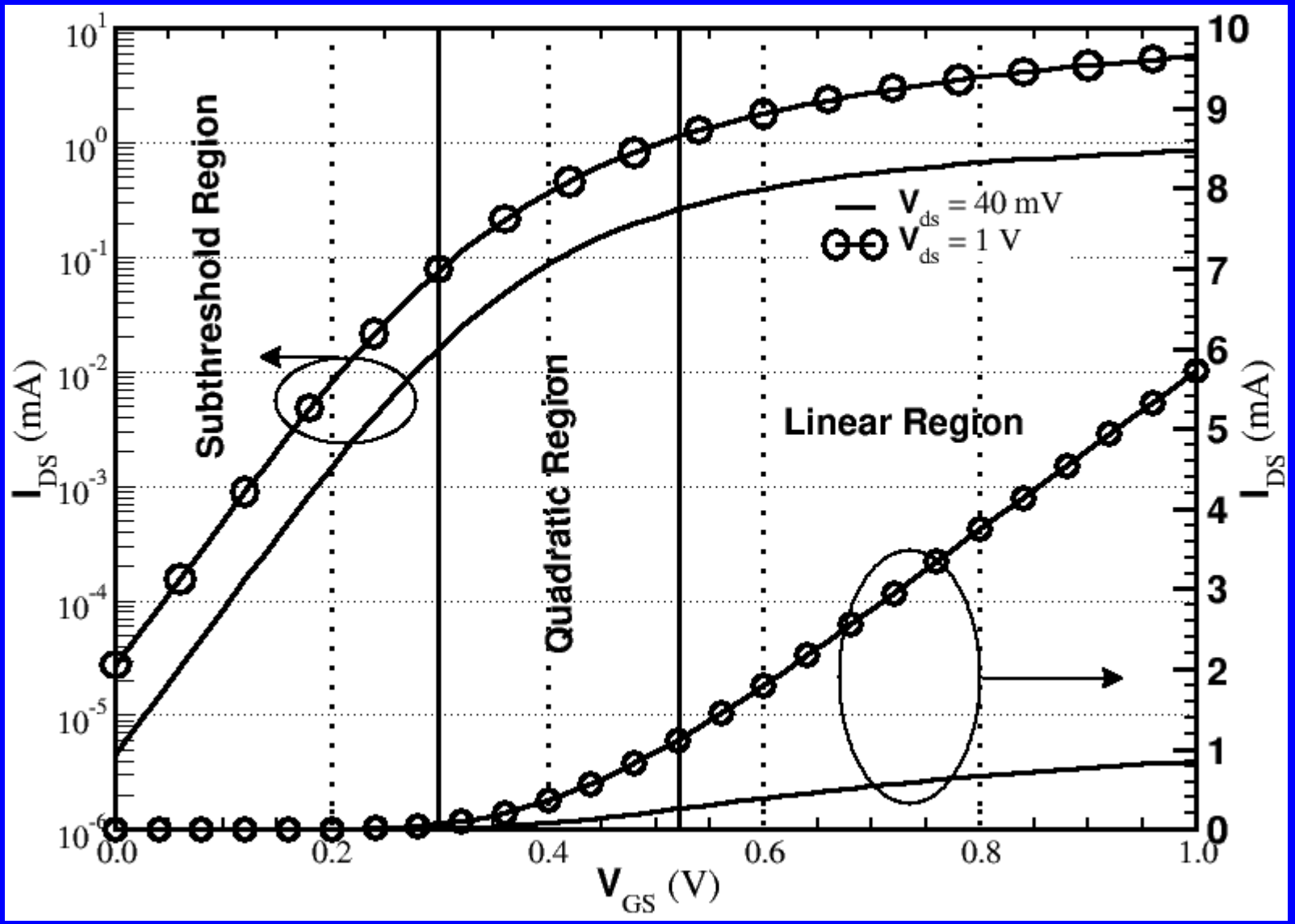
$$\mu_{ac}\left[\frac{cm^2}{Vs}\right] \approx 330\, E_{eff}^{\ -1/3}\left[\frac{MV}{cm}\right]$$

$$\mu_{sr}\left[\frac{cm^2}{Vs}\right] \approx 1450\, E_{eff}^{\ -2.9}\left[\frac{MV}{cm}\right]$$

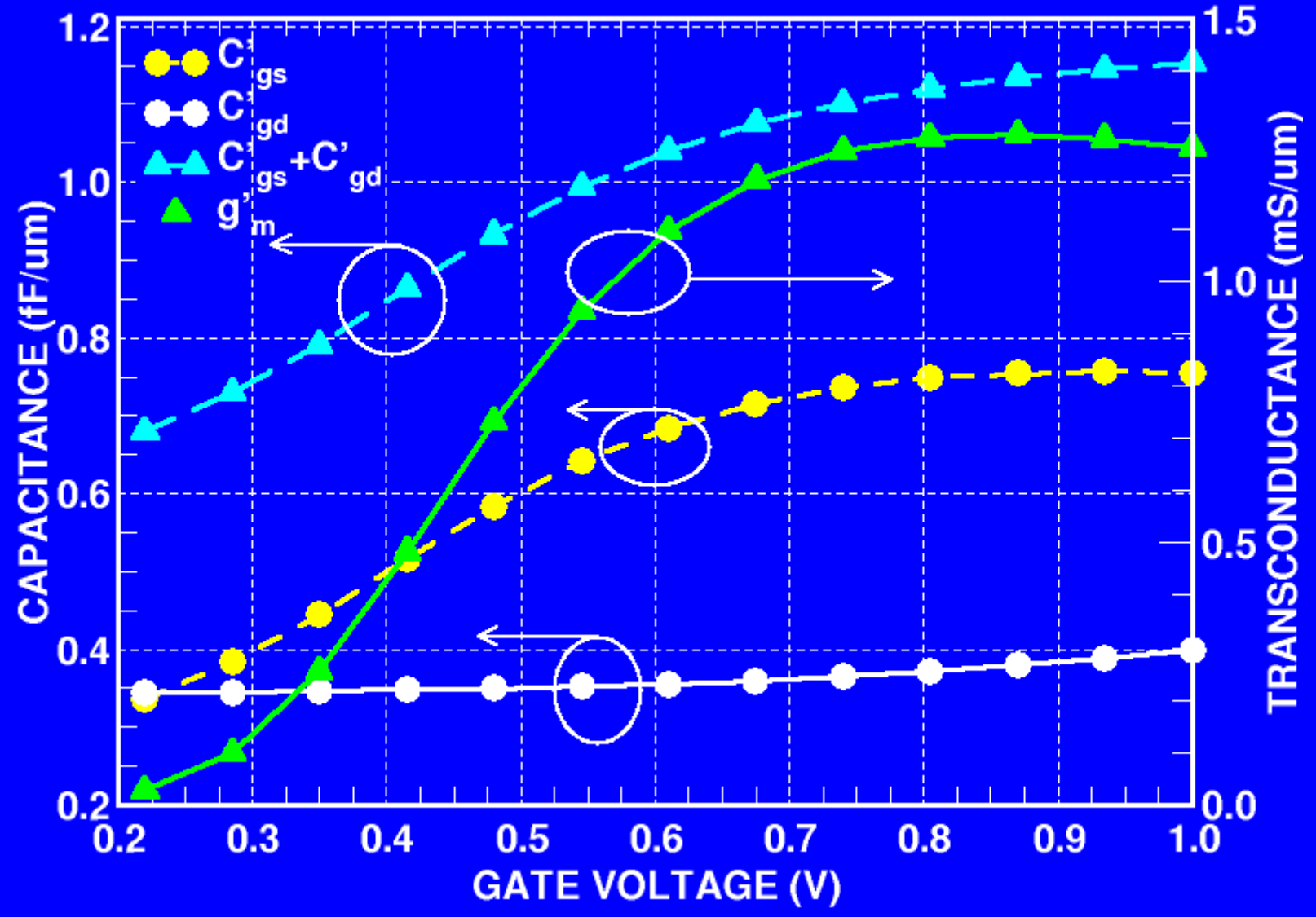
- The lateral field (due to V_{DS} bias) is about 50 times smaller than the vertical field



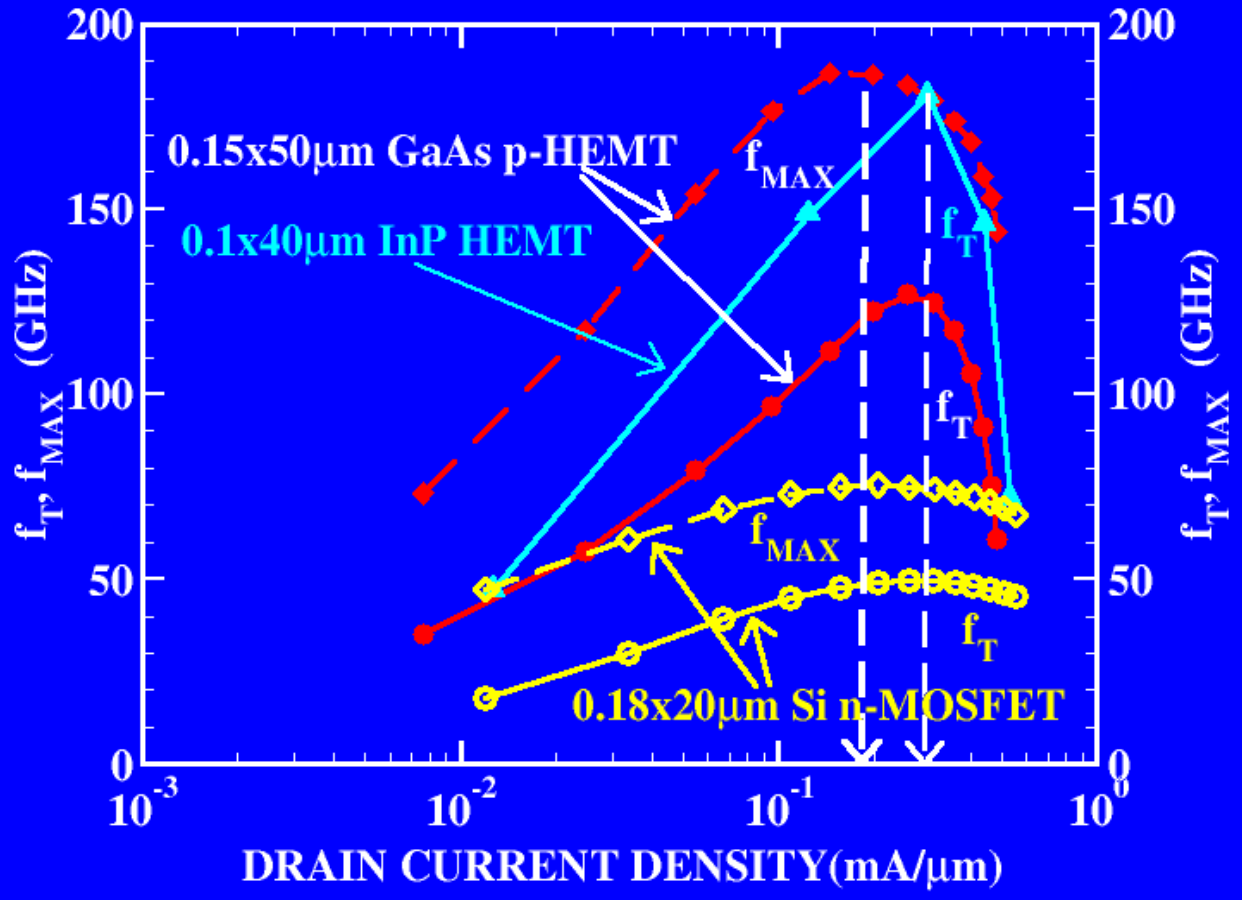
Measured transfer & subthreshold characteristics in 90-nm n-MOSFETS



Measured small signal g_m, C_{gs}, C_{gd} characteristics in 90-nm n-MOSFETS



Si vs. III-V FETs: f_T, f_{MAX}



S. Voinigescu et al. JHSES, March 2003

peak f_T: 0.3 mA/μm

peak f_{MAX}: 0.2 mA/μm

Consequences of constant-field scaling in 500 nm to 50 nm MOSFET channels:

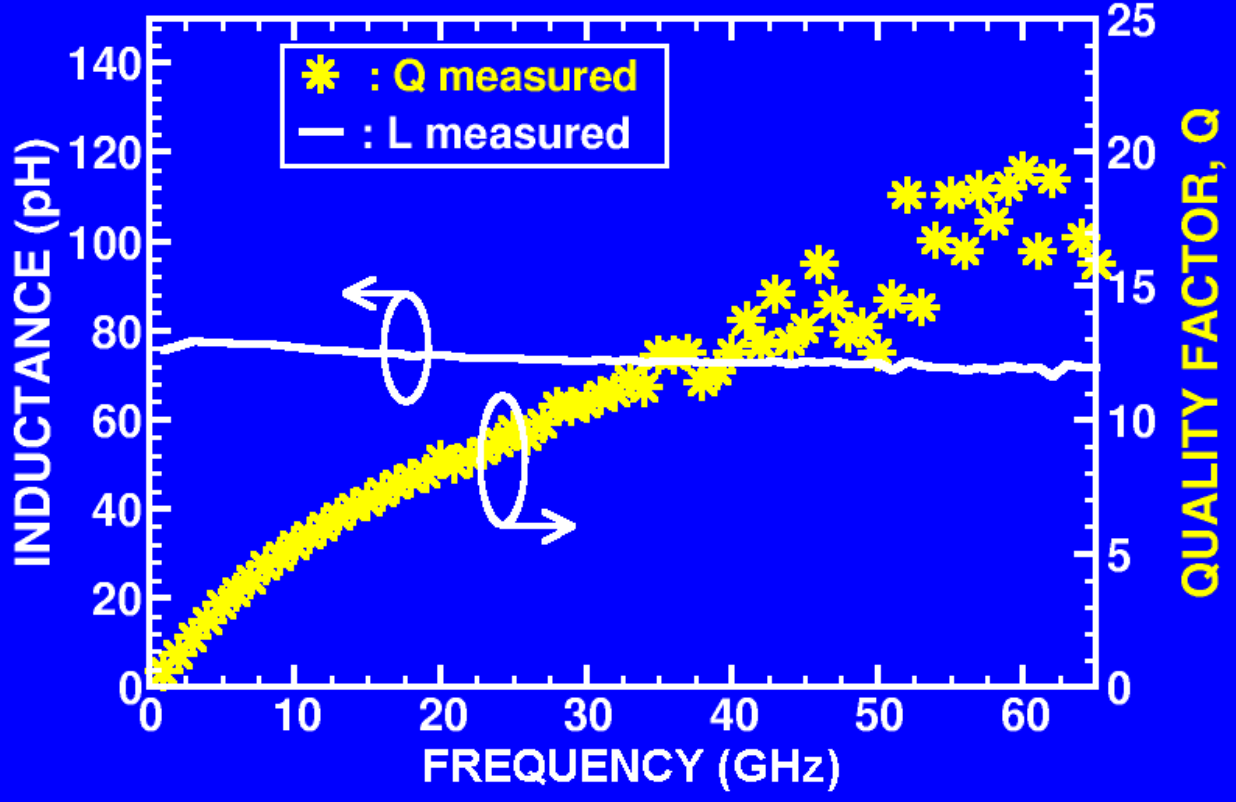
- C'_{gs}, C'_{gd}, C'_{db} constant over nodes down to 130 nm then decreasing as scaling of t_{OX} stopped at 1.2 nm
- g'_m, g'_{ds}, f_T, f_{MAX} increase
- F_{MIN}, R_n decrease
- RF & high-speed performance (except output swing) improves with scaling
- Constant current density biasing ensures design robustness over bias current, V_T, process variation, nodes & foundries

Scaling is good for high-speed digital/wireline

60-GHz, single metal inductor for VCOs

Planar spiral inductor:

Diameter = 27 μm
Turns = 1 ¾
S = 2 μm, W = 2.5 μm



C. Lee et al. CSICS-2004

Applying negative feedback for noise matching

- Negative feedback has similar impact on noise and input impedance
- *Use Y*-matrix to analyze noise params of:
  - Multifinger MOSFETs
  - CMOS inverter topology
  - Parallel (transimpedance) feedback circuits
- *Use Z*-matrix to analyze noise params of:
  - Differential stage
  - Series feedback circuits:
    - Tuned LNA with *L* (xfmr) degeneration
    - EF input
    - Inverter with resistive degeneration

Series feedback for noise matching

$$z_{SOP} = \sqrt{r_{SOPA}^2 + \frac{r_{NF}}{g_{NA}} + 2r_{CORA}\,\Re(Z_{11F}) + \Re^2(Z_{11F}) + \frac{\left|z_{CORF} - Z_{11F}\right|^2 g_{NF}}{g_{NA}}} + j\left[X_{SOP} - \Im(Z_{11F})\right]$$

$$F_{MIN} = 1 + 2g_{NA}\left[r_{CORA} + r_{SOP} + \Re(Z_{11}F)\right]$$

Parallel feedback for noise matching

$$Y_{SOP}=\sqrt{G_{SOPA}^{2}+\frac{G_{NF}}{R_{NA}}+2G_{CORA}\Re(Y_{11F})+\Re^{2}(Y_{11F})+\frac{\left|Y_{CORF}-Y_{11F}\right|^{2}R_{NF}}{R_{NA}}}+j\left[B_{SOP}-\Im(Y_{11F})\right.$$

$$F_{MIN}=1+2R_{NA}\left[G_{CORA}+G_{SOP}+\Re(Y_{11F})\right]$$

Inverter noise matching

$$F_{Zo} = 1 + \frac{1}{1 + \left(\frac{\omega L_0}{Z_0}\right)^2} + Z_0 \left(R_N \left| Y_{COR} + \frac{2}{Z_0} \right|^2 + G_N \right)$$

$$I_E(W_{OPT}) = \frac{1}{\omega} \frac{2}{Z_0} \sqrt{\frac{1}{\frac{G}{R} + G_C^2 + B^2}}$$

TIA noise matching

$$F_{Zo} = 1 + R_{NA} Z_0 \left| Y_{CORA} + \frac{1}{Z_0} + \frac{1}{R_F} \frac{1 - j\,\omega_0}{1 + \omega_0^2} \right|^2 + Z_0 G_{NA} + \frac{Z_0}{R_F} \frac{1}{1 + \omega_0^2}$$

$$I_E(W_{OPT}) = \frac{1}{\omega} \sqrt{\left(\frac{1}{Z_0} + \frac{1}{R_F} \frac{1}{1 + \omega_0^2} \right)^2 + \left(\frac{1}{R_F} \frac{\omega_0}{1 + \omega_0^2} \right)^2} \sqrt{\frac{1}{\frac{G}{R} + G_C^2 + B^2}}$$

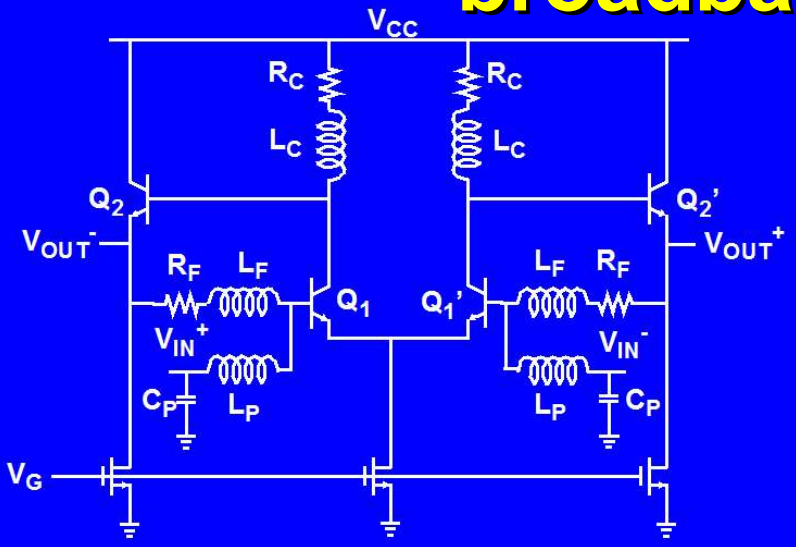
$$Z_{IN} = \frac{R_F}{1 + R_C I_T}$$

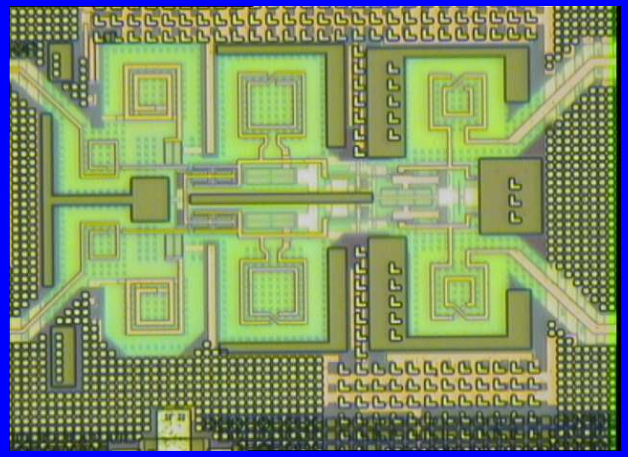
$R_F > Z_0$ for 50Ω match, resulting in lower noise & smaller transistor size than low-noise INV design

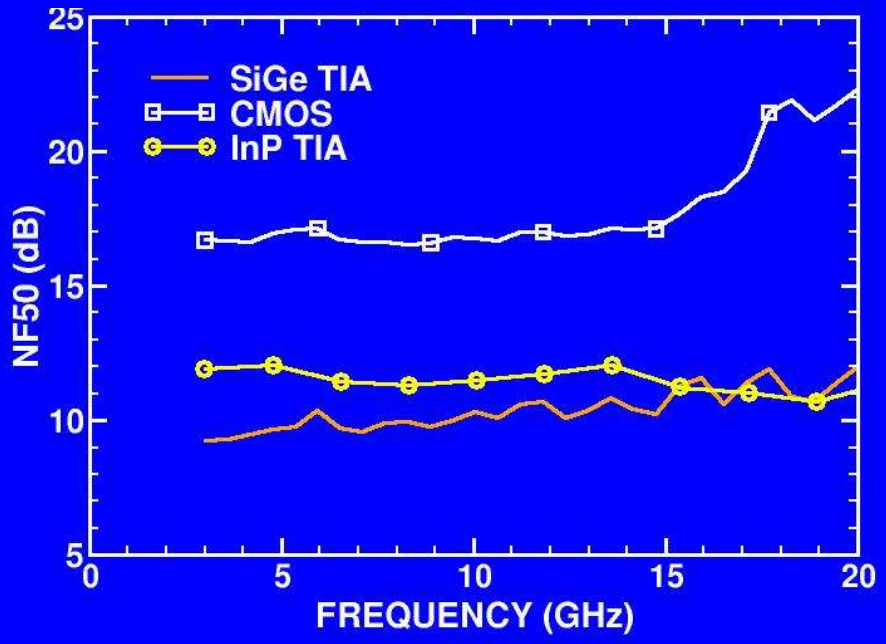
CMOS topology

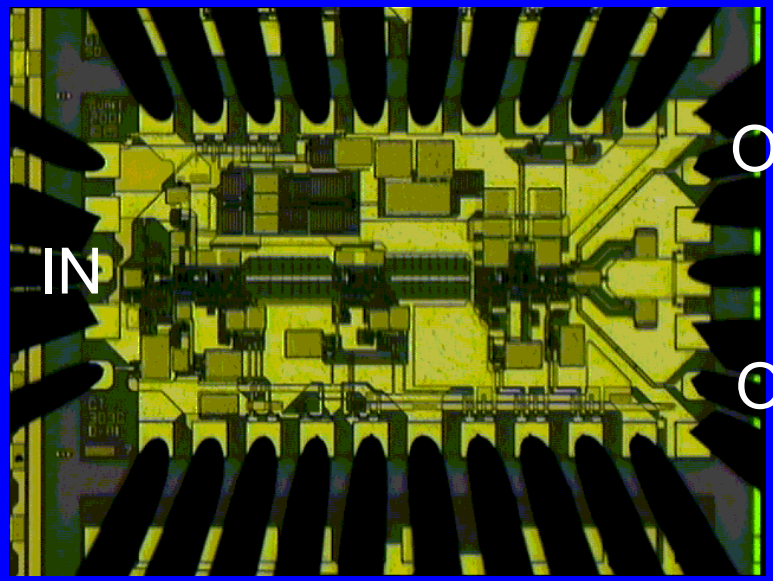
- In 90-nm CMOS, the p-MOSFET is low-noise and fast enough for most applications up to 40 Gb/s
  - Use CMOS inverter to improve g_m/I, R_n to save current over NMOS-only implementations

Si CMOS, SiGe BiCMOS, InP low-noise broadband preamps



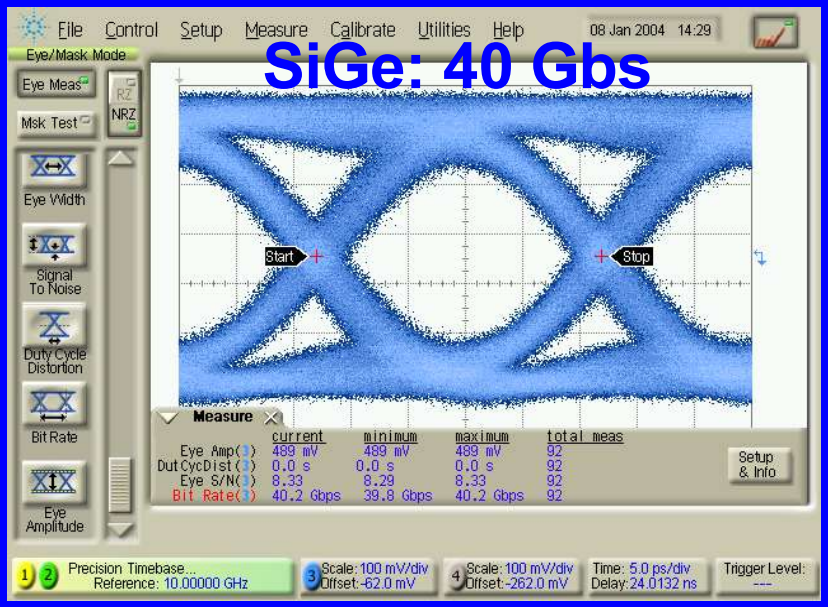


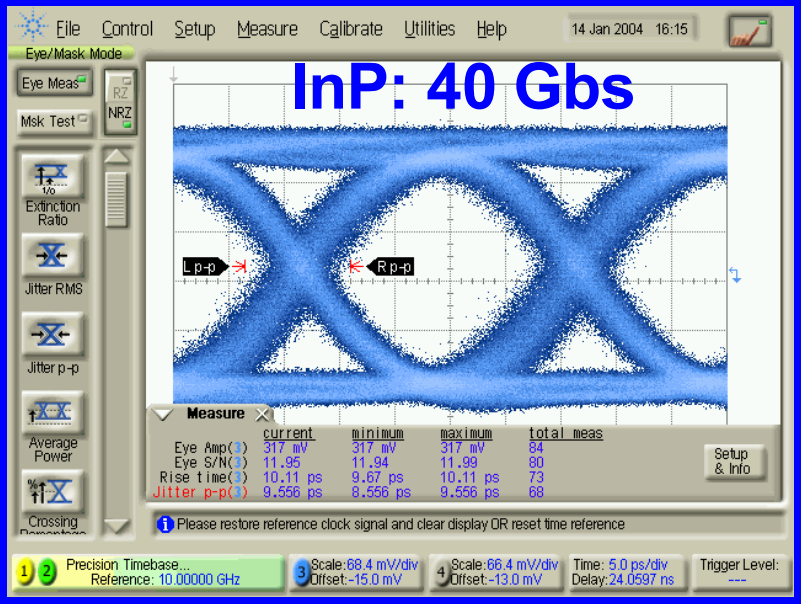




Low-noise broadband preamps: InP vs. SiGe BiCMOS

(H. Tran et al. GaAs IC Symp. 2003 for InP TIA)

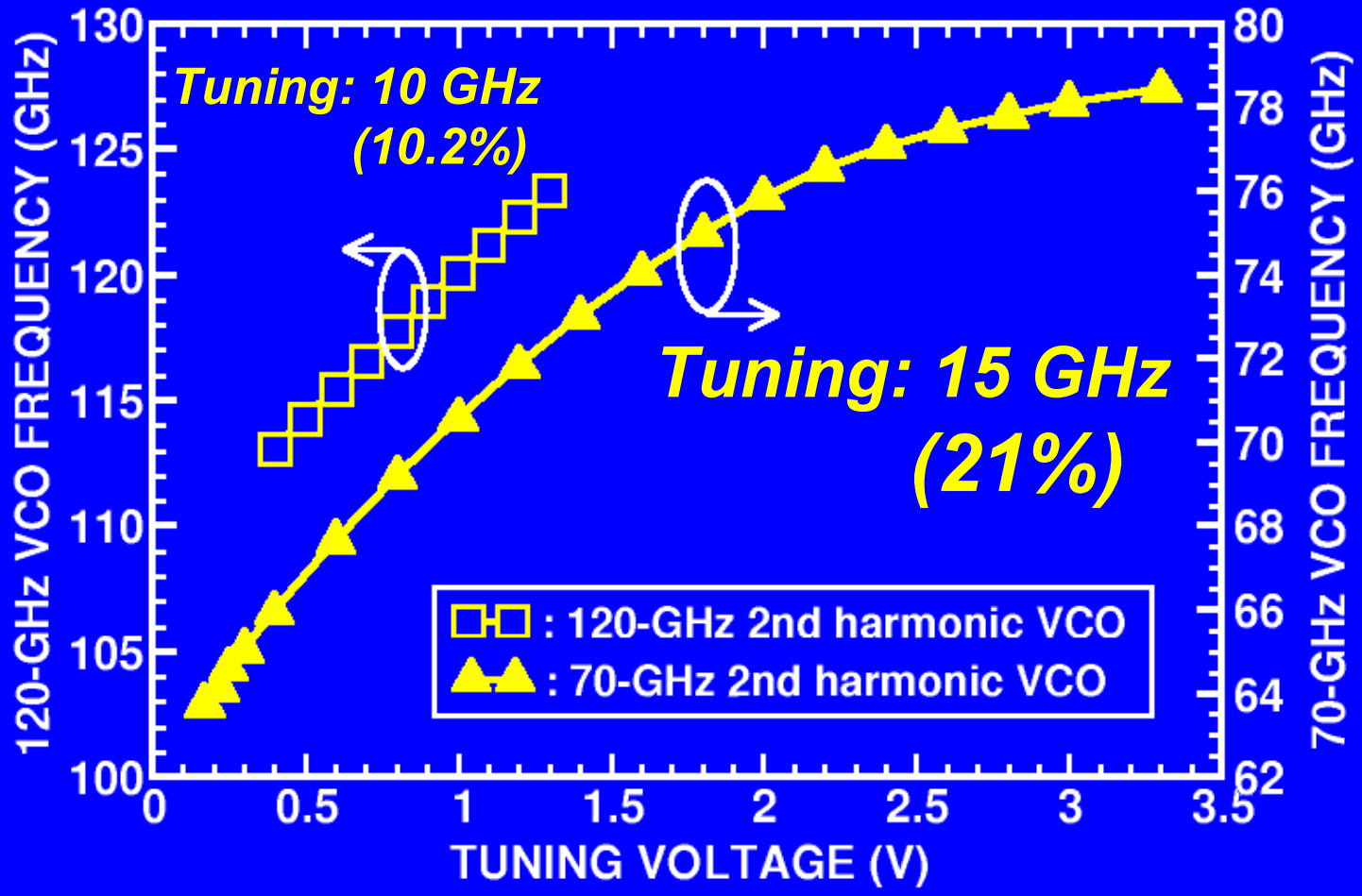




	NF at 10 Ghz	Data Rate	Sensitivity
CMOS	16.5 dB	20 Gb/s	20 mVpp
SiGe-HBT	10 dB	40 Gb/s	20 mVpp
InP-HBT	11.5 dB	40 Gb/s	8 mVpp

Push-Push VCO measurements (con't)

Tuning characteristics:



C. Lee et al. CSICS-2004

CMOS VCO design scaling and porting

- As technology scales to next node, g'_m increases but V_{MAX} decreases,
  - Ideally W and I_{DS} are fixed to maintain V_{OSC}
  - In reality W and I_{DS} must be reduced in sync with V_{MAX}
  - m*aximum* f_{OSC} increases hence larger C_{var} can be used
  - Scaling allows for smaller I_{DS}&W but not necessarily better $L(f_m)$

High-Speed Logic FoM: CML Gate Delay

$$SL_{HBT} = \frac{I_{CpeakfT}}{C_{bc} + C_{cs}} \qquad SL_{FET} = \frac{I_{DpeakfT}}{C_{gd} + C_{db}}$$

$$\tau_{HBT} \approx \Delta V \frac{C_{bc} + C_{cs}}{I_T} + \left(k + \frac{R_b}{R_L}\right) \Delta V \frac{C_\pi + (1 - A_V) C_{bc}}{I_T}$$

$$\tau_{FET} \approx \Delta V \frac{C_{gd} + C_{db}}{I_T} + \left(k + \frac{R_g}{R_L}\right) \Delta V \frac{C_{gs} + (1 - A_V) C_{gd}}{I_T}$$

$$\tau_{BiCMOS} \approx \Delta V \frac{C_\mu + C_{cs}}{I_T} + \left(k + \frac{R_g}{R_L}\right) \Delta V \frac{C_{gs} + C_{gd}}{I_T}$$

Scaling of MOS/BiCMOS CML logic

Table 1: fanout-of-1 latches ideal i.e. no parasitics, *) measured

Latch Family	*Rate:Gbs*	V_{DD} *(V)*	ΔV *(V)*	I_T *(mA)*	P_D*(mW)*	*Ind (nH)*
130nm MOSCML	40	1.8	0.5	1.5(2.4)	2.7	2
130nm BiCMOS CML	40	1.8	0.2	0.83 (1.6)	1.5 (2.9)	1
130nm BiCMOS CML *)	12	2.5	0.2	1	2.5	0
130nm BiCMOS ECL *)	50	2.5	0.25	7.5(12.5)	18(30)	0.25
90nm MOSCML	40	1.2	0.38	1.8	2.2	0.5
90nm BiCMOS CML	40	1.5	0.2	1	1.5	0.5
90nm BiCMOS CML extracted	30	1.5	0.2	1	1.5	0.5
65-nm MOSCML	60	1	0.35	2.5	2.5	0.5

- Assumes maximum inductor SRF of 80 GHz*nH and SRF=2*Bitrate
- Numbers in brackets include emitter(source) followers

49 Gb/s over 6-ft cable