Advanced SiGe BiCMOS and CMOS platforms for Optical and Millimeter-Wave Integrated Circuits

P. Chevalier, D. Gloria, P. Scheer, S. Pruvost,
F. Gianesello, F. Pourchon, P. Garcia, J.-C. Vildeuil,
A. Chantre, C. Garnier, and O. Noblanc
STMicroelectronics
FTM – Analog & RF Advanced R&D
850 rue Jean Monnet, F-38926 Crolles, France
pascal.chevalier@st.com

S.P. Voinigescu, T.O. Dickson, E. Laskin,
S.T. Nicolson, T. Chalvatzis, K.H.K. Yau
Edward S. Rogers Sr. Dept. of ECE
University of Toronto
Toronto, ON M5S 3G4, Canada
sorinv@eecg.toronto.edu

***Abstract*—This paper presents the status of most advanced CMOS and BiCMOS technologies able to address very high-speed optical communications and millimeter-wave applications. The performance of active and passive devices available on bulk Si and high-resistivity SOI is reviewed and HF characteristics of state-of-the-art SiGe HBTs and MOSFETs are compared. The performance of building blocks designed in different CMOS and BiCMOS platforms are also presented. Finally, we conclude on the suitability of different Si technologies to address such high-frequency applications.**

BiCMOS; CMOS; millimeter-wave circuits; optical communication

I. INTRODUCTION

Si-based technologies now offer competitive performance to address applications such as 60-GHz WLAN and 77-GHz automotive radar for which large volumes can be expected. This paper presents the state-of-the-art performance of active and passive devices both on bulk Si and high-resistivity (HR) silicon-on-insulator (SOI). Performances of 65-nm MOSFETs and 130-nm-based SiGe HBTs, featuring both f_T (current gain cut-off frequency) and f_{max} (maximum oscillation frequency) close to, or higher than, 200 GHz, are compared. The different design approaches for both inductors and transmission lines are discussed according to substrate choice. Next, the most advanced STMicroelectronics platforms are described, and results obtained on both digital and analog circuits above 40 Gb/s – 40 GHz are compared. Based on these results, the need for a dedicated Si platform for mm-waves operation is discussed and we conclude on the choices that appear to be the most relevant regarding performance, cost and time-to-market.

II. SI-BASED HIGH-PERFORMANCE DEVICES

A. Active Devices on Bulk and SOI

1) Bipolar devices:

HBTs feature many advantages compared to CMOS devices such as their lower *1/f* noise, higher output resistance and higher voltage capability for the same speed. Many companies now offer HBTs featuring $f_T \geq 200$ GHz [1]-[2]-[3]-[4] with f_{max} sometimes ≥ 300 GHz [1]-[2]-[3].

Fig. 1 and Fig. 2 summarize the performance of ST HBTs demonstrated in the 130-nm CMOS node. While the f_T vs. BV_{CEO} chart - BV_{CEO} being the emitter–collector breakdown voltage - is the traditional benchmark, the f_{max} vs. BV_{CBO} chart - BV_{CBO} being the collector-base breakdown voltage - provides complementary information. Indeed, f_{max} is often more suitable to reflect HF capability while BV_{CBO} gives the maximum available breakdown voltage i.e. in the common-base configuration. Three types of E–B structures are compared on these charts: a quasi-self-aligned (QSA) using a single-polysilicon layer (SP), a quasi-self-aligned (QSA) using a double-polysilicon layer (DP), and a fully-self-aligned (FSA) using a double-polysilicon layer (DP). Two types of collectors

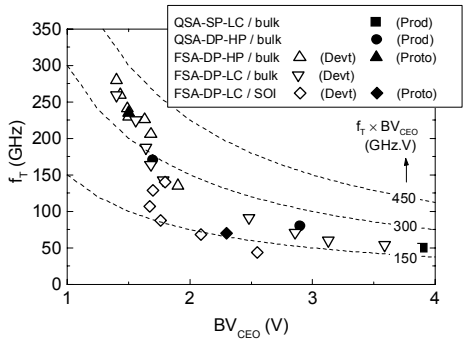

Fig. 1. $f_T - BV_{CEO}$ chart built with various Si/SiGeC HBTs available in 130-nm CMOS node. Different architectures with different maturities are compared.

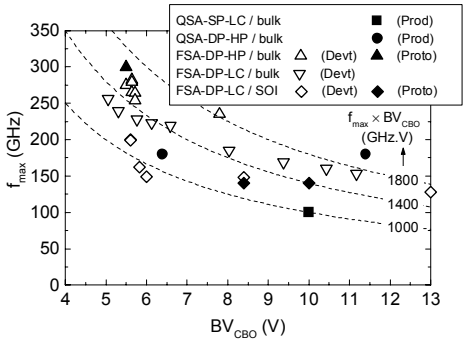

Fig. 2. $f_{max} - BV_{CBO}$ chart built with various Si/SiGeC HBTs available in 130-nm CMOS node. Different architectures with different maturities are compared.

are reported: a high-performance (HP) collector using a buried layer, a collector epitaxy and deep-trench isolation and a low-cost (LC) implanted collector. Finally devices fabricated on thin SOI (160 nm) are compared to bulk devices. These charts show that a 50-GHz f_T device, suitable for most low-power RF applications, can be obtained with a low-complexity structure (QSA-SP-LC). SOI requires a more complex E–B architecture but allows for a simple collector construction [5]. It is important to notice that a high-performance collector cannot be built on thin SOI which considerably limits the achievable f_T below 150 GHz [5]. The only way to overcome this issue is to locally etch the buried oxide and grow a selective epitaxial collector [6]. Finally, 300-GHz f_{max} HBTs can only be safely fabricated with HP collector and FSA E–B architecture.

2) CMOS devices:

CMOS technologies and their ability to follow Moore's law are at the root of the success of Si technologies. Continuous scaling, leading to always-increasing functional integration, is the driving force behind digital CMOS. 65-nm CMOS still uses a polysilicon gate with a nitridated gate oxide to get a low equivalent oxide thickness (EOT) together with a thicker oxide [7]. In fact, the main novelty comes from the solutions introduced to increase carrier mobility. In ST's 65-nm CMOS, the hole mobility in PMOS devices is increased by 15% by using rotated substrates and the electron mobility in NMOS devices is increased by 12% by using a tensile liner film.

RF-CMOS, too, benefits from the gate down scaling with the improvement of main figures of merit that are f_T, f_{max} and NF_{min}. Modifications of the core process may be needed to improve RF performance but they have to be limited in order to maintain low cost of CMOS. Then, most of the additional work needed for RF-CMOS concerns analog and HF characterization, and modeling. Fig. 3 shows the evolution of f_T with the gate length and the gate oxide thickness for different NMOS devices coming from the most recent ST technologies. Even though we would theoretically expect that $f_T \propto 1/L_g^2$, it is experimentally found that $f_T \propto 1/L_g^{\alpha}$ (with α close to 1) and that it is independent of the gate oxide thickness. 150 GHz and 200 GHz f_T's are reached in 65-nm node for "low power" (LP) and "general purpose" (GP) devices, respectively. Furthermore, as it will be seen in next section, excellent HF noise figures are measured on these devices.

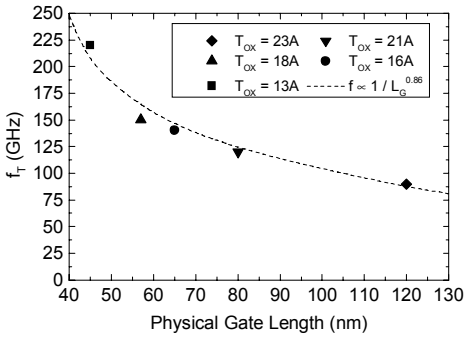

Fig. 3. Evolution of f_T with physical gate length for different NMOS devices (LP and GP) of 130-nm, 90-nm and 65-nm CMOS nodes.

Moving from bulk to thin SOI does not change the HF performance of CMOS devices significantly. Two kinds of devices are available on SOI [8], floating body (FB) and body contacted (BC) devices. FB devices are in fact devices using the same layout as on bulk. It is well known that FB devices, interesting for digital operation, suffer from a kink effect that degrades both voltage gain (high g_{ds}) and *1/f* noise. However, the kink effect has no impact on HF characteristics and SOI FB MOSFETs exhibit f_T and f_{max} at least identical to those in bulk devices with identical layout. On the contrary, HF performance of BC devices is penalized by their specific layout (higher gate resistance and gate to source capacitance). The body contacts avoid however the kink effect, making this device well suited for analog functions.

3) Performance comparison between state-of-the-art Si/SiGeC HBT and NMOS

Devices chosen for this comparison are from "contemporary" technologies, and both feature f_T close to or higher than 200 GHz: a 130-nm based FSA Si/SiGeC HBT named "BipX" [2] and a 65-nm LP NMOS [7]. Device geometries chosen for this comparison are used in mm-waves designs i.e. 3 emitter fingers of 2.5 µm each for the HBT and 10 cells of 9 gate fingers of 1 µm each for the NMOS (gate fingers are contacted at both sides). Fig. 4 presents the evolution of f_T, f_{max} and NF_{min} with current density (reduced respectively to emitter length L_E and gate width W_G). HBT and NMOS feature maximum f_T / f_{max} of 230 GHz / 300 GHz and 170 GHz / 325 GHz respectively. The first observation is the difference in current density between the two devices since cut-off frequencies peak at ~ 0.4 mA/µm and ~1.9 mA/µm for the MOSFET and the HBT, respectively. The difference is reversed if the currents are not normalized to device length/width since the emitter area is about 6 times lower than the total gate area. Minimum noise figures measured at 40 GHz are also reported in Fig. 4. NF_{min} of 1.1 dB and 0.95 dB are measured for the HBT and the NMOS, respectively. They

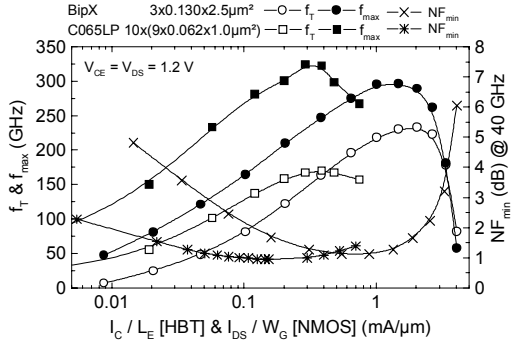

Fig. 4. f_T, f_{max} and NF_{min} @ 40 GHz vs. current density for BipX and 65-nm LP NMOS (measurements).

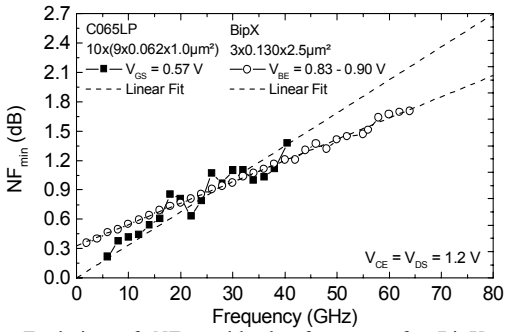

Fig. 5. Evolution of NF_{min} with the frequency for BipX and 65-nm LP NMOS (measurements).

correspond to f_T's of ~200 GHz and ~140 GHz for the HBT and the NMOS, respectively (NMOS exhibits ~1.1 dB noise at f_T ~ 170 GHz). The noise performance of the HBT is penalized by a higher noise resistance R_n, which is explained by a lower device development (R_B+R_E ~ 13 Ω > R_G+R_S ~ 4 Ω, and dominates R_n).

Fig. 5 presents the variation of NF_{min} with frequency up to 40 GHz for the NMOS, and up to 65 GHz for the HBT. Noise figure of the NMOS can be extrapolated to higher frequencies with confidence that would give NF_{min} ~ 2.7 dB at 80 GHz. This evolution is indeed linear and NF_{min} is always reached at same V_{GS}, irrespective of frequency [9]. A linear fit can be applied to HBT too, but without the same confidence (in spite of the very good fit shown in Fig. 5) since NF_{min} shifts to higher V_{BE} when frequency increases. Nevertheless, such a linear extrapolation is not unreasonable since an extrapolation from small-signal equivalent circuit gives NF_{min} ~ 2.2 dB at 80 GHz (vs. ~2.0 dB for linear extrapolation). We can then conclude that intrinsic HF performances of C065 NMOS and BipX devices are close, with a peak f_T advantage (+60 GHz) for the HBT however.

B. Passive Devices on Bulk and SOI

The comparison presented above is not sufficient to choose a technology since the quality of passives such as transmission lines (TL) and inductors usually available in Si technologies is often the main limitation to MMIC performance. The choice of the BEOL cannot be separated from the substrate choice i.e. bulk or SOI. In fact it is not the buried oxide that is important but the high-resistivity substrate (1 kΩ/sq) lying underneath. The trend when moving from one CMOS node to the next is the vertical shrink of the BEOL together with the decrease of the metal and dielectric thicknesses and of the metal pitch in order to increase integration density. This is in direct conflict with what is required for low TL losses. Indeed the attenuation constant of 50-Ω microstrip (MS) lines built in the digital BEOL with M1+M2 patterned ground shield (PGS) strongly degrades when moving from 130-nm (~0.9 dB/mm @ 40GHz) to 65-nm (~1.3 dB/mm @ 40GHz) CMOS using the same number of metal layers. Similarly, the performance of spiral inductors is degraded since a large metal pitch and thick dielectric are preferred to minimize the ohmic losses in the spiral coil and the substrates losses, respectively.

On the contrary, the main advantage of HR SOI is to provide good quality inductors and TL with standard digital CMOS BEOL. The second advantage is to allow the use of coplanar waveguides (CPW) instead of MS lines thanks to the low loss substrate. CPW lines could be preferred since they are less sensitive to process variations than MS lines (s/w ratio depends on inter-metal dielectric thickness). Furthermore, the reduced parasitic capacitances and low substrate losses associated with HR SOI are further improved as frequency increases.

On the other hand good performance can be obtained on bulk Si with MS if the BEOL is adapted to thicker dielectric and thicker metal lines [10] together with M1+M2 PGS. Results comparable to HR SOI i.e. 0.5 dB/mm at 40 GHz and < 1 dB/mm at 100 GHz have been reported [9]. This solution is preferred today since it is fully compatible with BiCMOS bulk technologies.

III. EVALUATION OF SI PLATFORMS FOR DESIGNS ABOVE 40 GB/S – 40 GHZ

The objective of this section is to present the results obtained on key building blocks using the most advanced ST technologies. These technologies, the main characteristics of which are presented in Table I, are 90-nm CMOS [11], 65-nm CMOS, 0.13-µm BiCMOS (BICMOS9) [12] and the BipX bipolar technology (0.13 µm) [2]. Frequency dividers and voltage controlled oscillators (VCO) results are presented here but other blocks such as decision circuits and low-noise amplifiers have been evaluated too. 65-nm CMOS results come from simulation only. Other recent results from the literature are provided for the sake of comparison.

During the last years a number of static frequency dividers have been reported with input frequencies above 60 GHz using SiGe BiCMOS [13], InP HBT [14] and CMOS [15] topologies. Measured data for these and other SiGe HBT-only [16]-[17]-[18] and InP HBT [19]-[20] circuits are collected in Table II together with simulation results for 65-nm CMOS. These results clearly indicate that there is a direct link between the f_T of the process and the maximum frequency of the divider [16]. The BipX experimental results (230-GHz f_T SiGe HBT of [16]) and the 65-nm CMOS simulations point to the continued and significant advantage of bipolar implementations.

Voltage controlled oscillators (VCOs) results are summarized in Table III. The difficulty with realizing high performance VCOs at mm-waves lies in the requirement to operate the transistors in the VCO as low noise amplifiers with large voltage swings. This imposes low-noise figure, high f_{max} and large breakdown requirements on the transistor. The former two are easily met by 65-nm CMOS transistors in which the minimum noise and peak f_{max} bias almost coincide at 0.2 mA/µm. The latter condition continues to favour SiGe and InP HBTs. This explains why, despite the significant progress made by mm-wave 90-nm CMOS VCOs [21]-[24] in the last year, their phase noise (depending on *1/f* noise), output power, and tuning range fall short of the best results reported with SiGe HBT VCOs [22]-[23]-[27]. No mm-wave VCOs have been reported to date in the 65-nm node. LP 65-nm devices, with their high f_{max}, low noise figure, and reliable 1.2 V swing, are expected to further narrow the gap to SiGe HBT VCOs for output power levels up to a few mW. GP 65-nm devices may suffer from reliability problems at 1.2 V swings.

TABLE I. MAIN CHARACTERISTICS OF ST TECHNOLOGIES USED FOR MM-W BUILDING BLOCKS COMPARISON. DATA WRITTEN IN ITALIC ARE EXTRACTED FROM MODELS AND THEN USED FOR SIMULATIONS.

Technology	**C090**		**C065**		**BC9**	**BipX**
Type	**CMOS**		**CMOS**		**BiCMOS**	**Bipolar**
Node (nm)	90		65		130	130
BEOL (Cu)	7ML+Al		NA		6ML+Al	6ML+Al
Device	LP	GP	LP	GP	HS	HS
L_G / W_E (nm)	90	65	57	45	170	130
f_T (GHz)	120	NA	*190*	*210*	170	230
f_{max} (GHz)	200	NA	*200*	*220*	170	300

TABLE II. COMPARISON BETWEEN INP, SIGE HBT, AND CMOS DIVIDERS. 65-NM CMOS IS SIMULATED.

Technology	Fond.	Self-Oscillation Freq.	Max. Divider Freq.	Power Consumpt.
135-GHz f_T InP	HRL [14]	33 GHz	100 GHz	750 mW
90nm CMOS	IBM [15]	48 GHz	66 GHz	80 mW (1.8V)
170-GHz f_T SiGe HBT	ST [16]	54 GHz	70 GHz	145 mW (3.3-3.6V)
225-GHz f_T SiGe HBT	Infineon [17]	65 GHz	110 GHz	1.35 W (-5.2V)
210-GHz f_T SiGe HBT	IBM [18]	71 GHz	96 GHz	770 mW (-5.0V)
230-GHz f_T SiGe HBT	ST [16]	77 GHz	100 GHz	122 mW (3.3-3.6V)
65nm LP CMOS	ST *(Sim.)*	*N/A*	*85 GHz*	*36 mW (1.2V)*
450-GHz f_T InP	UCSB [19]	86 GHz	150 GHz	?
400-GHz f_T InP	HRL [20]	95 GHz	143.6 GHz	90 mW

TABLE III. PHASE NOISE OF STATE-OF-THE-ART SIGE HBT AND CMOS W-BAND OSCILLATORS (WITH PROCESS F_T / F_{MAX}).

Technology	Fond.	Oscil. freq.	Tun. range	Phase Noise [dBc/Hz]	Pout (dBm)	P_{DC} (mW)
90nm CMOS	UMC [21]	60GHz	0.17	-100@1MHz	-23.2	1.9
175/275 GHz f_T / f_{max} SiGe HBT	Infineon [22]	77GHz	8.7	-97@1MHz	18.5	1200
		100GHz	6.2	-90@1MHz	14.3	1200
200/275 GHz f_T / f_{max} SiGe HBT	Infineon [23]	75GHz	6.1	-105@1MHz	3.5	72
90nm CMOS	ST [24]	77GHz	8.1	-100@1MHz	-13.8	37.5
205/290 GHz f_T / f_{max} SiGe HBT	IBM [25]	85GHz	2.7	-94@1MHz	-8	25
130nm CMOS	UMC [26]	90GHz	2.4	-105@10MHz	-16	15.5
170/180 GHz f_T / f_{max} SiGe HBT	ST [27]	96GHz	4.6	-94@1MHz	0.7	133
206/197 GHz f_T / f_{max} SiGe HBT	Infineon [28]	98GHz	33	-85@1MHz	-6	60
230/300 GHz f_T / f_{max} SiGe HBT	ST [27]	105GHz	4.4	-98@1MHz	2.7	133
75/ 200GHz f_T / f_{max} InP HBT	TRW [29]	108GHz	2.6	-88@1MHz	0.92	204
130nm CMOS	TSMC [30]	114GHz	2.1	-108@10MHz	-22.5	8.4

IV. A DEDICATED STMICROELECTRONICS PLATFORM FOR WLAN AND AUTOMOTIVE RADAR

Results presented in the previous section demonstrate that Si-based technologies available today are able to address mm-waves applications. While CMOS devices now compete with bipolar devices and can give design advantages (power consumption for instance), on the whole, Si/SiGeC HBTs give more design margin since they provide higher gain and higher voltage swing, which are important criteria for critical blocks such as VCOs or PAs, especially in harsh environments (high-temperature in automotive). Furthermore CMOS devices suffer from the lack of design maturity in this frequency range and there are concerns regarding device reliability for applications requesting large voltage swings (especially for smallest gate lengths giving best HF performances). As a consequence BiCMOS technologies are the most reliable (and cheaper) choice for emerging applications such as automotive radars and 60-GHz WLAN [31]. Indeed, bipolar-only technologies suffer from the absence of the CMOS devices [32], which make better varactors than the p-n junctions at mm-waves.

Nonetheless, as good as the HBT performance may be, even featuring 300-GHz f_{max}, there is not enough margin for a demanding system such as 77-GHz automotive radar to allow for poor passives. In that situation, since HR SOI is not easily compatible with high-performance HBT (SOI use would introduce an additional complexity/cost), a dedicated BEOL is required. Development of such a BiCMOS technology (BiCMOS9MW [33]), with a state-of-the-art HBT and dedicated BEOL, is under way at STMicroelectronics. The 0.13-µm CMOS node has been chosen as the best trade-off between technology cost and a CMOS density able to cover systems-on-chip (SoC) such as WLAN. Applications that would require higher CMOS density will use a system-in-package (SiP) approach with a 65-nm CMOS companion chip.

V. CONCLUSION

The performance and design maturity of 65-nm CMOS are not sufficient to replace today's SiGe BiCMOS for most MMICs above 50 GHz. Furthermore a BiCMOS technology, relying on the *n-2* CMOS generation, has a significant cost advantage especially for applications that do not require very high density of digital functions. CMOS may only emerge as a competing technology for mm-waves SoC (if feasible and/or relevant), while BiCMOS appears more favorable for mm-waves SiP.

REFERENCES

[1] A.J. Joseph, in Proceedings of the IEEE, vol. 93, no. 9, Sept. 2005, pp. 1539-1558.
[2] P. Chevalier et al., in Proc. BCTM, 2005, pp. 120-123.
[3] J. Böck et al., in IEDM Tech. Dig., 2004, pp. 255-258.
[4] M. Racanelli et al., IEEE TED, vol. 52, no. 7, Jul. 2005, pp. 1259-1270.
[5] P. Chevalier et al., in IEDM Tech. Dig.,2005, pp. 983-986.
[6] H. Rücker et al., in IEDM Tech. Dig., 2004, pp. 239-242.
[7] F. Arnaud et al., in Symp. on VLSI Technology Tech. Dig., 2004, pp. 10-11.
[8] C. Raynaud et al., in Proc. 207th ECS, 2005, pp. 331-344.
[9] S.P. Voinigescu et al., in CICC Proc., 2005, pp.111-118.
[10] M. Gordon et al., in SiRF Tech. Dig., 2004, pp. 53-56.
[11] L.F. Tiemeijer et al., in IEDM Tech. Dig., 2004, pp. 441-444.
[12] M. Laurens et al., in Proc. BCTM, 2003, pp 199-202.
[13] T. O. Dickson and S. P. Voinigescu, in SiRF Tech. Digest, 2006, pp. 273–276.
[14] M. Mokhtari et al., IEEE JSSC, vol. 38, no. 9, Sept. 2003, pp. 1540–1544.
[15] J. O Plouchart et al., in ISSCC Tech. Dig., 2006, pp. 526–527.
[16] E. Laskin et al., in Proc. BCTM, 2006, in press.
[17] S. Trotta et al., in CSICS Tech. Dig., 2005, pp. 291–294.
[18] A. Rylyakov and T. Zwick, IEEE JSSC, vol. 39, no. 10, Oct. 2004, pp. 1712–1715.
[19] Z. Griffith et al., IEEE JSSC, vol. 40, no. 10, Oct. 2005, pp. 2061–2069.
[20] D. A. Hitko et al., in CSICS Tech. Dig., 2004, pp. 167–170.
[21] D. Huang et al, in ISSCC Tech. Dig., 2006, pp. 314-315.
[22] H. Li et al., IEEE JSSC, vol. 39, no. 10, Oct. 2004, pp. 1650-1658.
[23] R. Wanner et al., in SiRF Tech. Dig., 2005, pp. 375-378.
[24] K.W. Tang et al., in CSICS Tech. Dig., 2006, in press.
[25] B.A. Floyd, in RFIC Symp. Dig., 2004, pp. 295-298.
[26] C. Cao et al., in Sym. on VLSI Circuits Tech. Dig., 2005, pp. 242-243.
[27] S.T. Nicolson et al., in Proc. BCTM, 2006, in press.
[28] W. Perndl et al., IEEE JSSC, vol. 39, no. 10, Oct. 2004, pp. 1773-1777.
[29] K.W. Kobayashi et al., IEEE JSSC, vol. 34, no. 9, Sept. 1999, pp. 1225-1232.
[30] P. Huang et al., in ISSCC Tech. Dig., 2005, pp. 404-406.
[31] B. Gaucher et al., in SiRF Tech. Dig., 2004, pp. 81-84.
[32] S.P. Voinigescu et al., in Proc. BCTM, 2006, in press.
[33] P. Chevalier et al., Submitted to SiRF'07.