Charge Dynamics in Heterostructure Schottky-Gate Capacitors and Their Influence on the Transconductance and Low-Frequency Capacitance of MODFET's

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Abstract—**This paper presents a computer investigation of the gate capacitance and transconductance characteristics of MODFET's and related capacitors. The quantum-mechanically predicted behavior of single- and multiple-heterostructure transistors is in excellent agreement with experiments presented in the literature. The donor level energy is shown to directly affect the transconductance and capacitance characteristics. For the first time, the capacitance of multiple-heterojunction devices is predicted to exhibit a staircase nature with possible applications in *n*-ary logic circuits. A critical analysis of the application of *C–V* profiling techniques to heterostructure capacitors is also presented.**

I. Introduction

THE advent of the modulation-doped field-effect transistor (MODFET, also called TEGFET, HEMT, and SDHT) in very high speed (VHS-) and microwave monolithic (MM-) IC's has been accompanied by a large body of theoretical and experimental work dedicated to the understanding and modeling of the physical phenomena pertaining to the operation of this novel device. Like the MOS capacitor in C-MOS integrated circuits, the heterostructure Schottky-gate capacitor can play an important part in the theoretical and experimental characterization of MODFET IC's, as well as in fundamental research (integral and fractional quantum Hall effect [1], [2], etc.). As indicated in the literature [3], gate capacitance is one of the most significant parameters in small- and large-signal modeling and an extremely valuable tool in assessing the transconductance and the current-driving capabilities of MODFET's.

Since the initial work of Delagebeaudeuf and Linh [4] quite a few papers have been involved with analytical models investigating the C–V_{gs} and g_m–V_{gs} characteristics of MODFET's. Most of the theoretical studies are rather simplistic in their treatment and fail to explain the complex experimentally observed capacitance–voltage behavior. One good model, proposed by Maloney *et al.* [5], manages to at least qualitatively grasp all the main features of charge dynamics in modulation-doped heterostructure (MDH) capacitors as reflected in transconductance and capacitance measurements. Vinter [6] has also tackled the problem by numerical analysis (including a quantum-mechanics derivation of the 2-DEG) of the gate and free-electron charge capacitance of SH-MODFET's. However, he does not delve deeper into the intrinsic properties of the charge dynamics in these devices.

It is the purpose of this paper to: 1) offer a refined quantum-mechanics model for the calculation of gate capacitance and transconductance of MDH capacitors and FET's; 2) estimate the error associated with the "classical" numeric model, which solves the Poisson equation using the 3-D Fermi–Dirac distribution function to determine the carrier profiles in the channel; 3) investigate the C–V_{gs} characteristic's dependence on donor level energy and extract the electron profile by numeric simulation of experimental C–V profiling techniques; 4) prove that the so-called "transconductance degradation" is primarily an intrinsic property of the charge dynamics of MDH's and is to a lesser extent affected by the carrier mobility in the barrier layer; 5) derive the C–V_{gs} and g_m–V_{gs} characteristics of multiple-heterojunction FET's (MH-MODFET's).

II. Quantum-Mechanical Numeric Modeling of C–V_{gs} and g_m–V_{gs} Characteristics

Consider the MDH capacitor structures shown in Fig. 1. The static gate capacitance C_T and free-electron charge capacitance C_n (which includes 2-DEG and barrier electrons) can be computed as functions of the gate voltage according to (1) and (2)

$$C_T(V_{gs}) = \Delta Q_T/\Delta V_{gs} \cdot Q_T(V_{gs}) = q\int [N_A(z) - N_D^+(z) + n(z)]dz \tag{1}$$

$$C_n(V_{gs}) = \Delta Q_n/\Delta V_{gs} \cdot Q_n(V_{gs}) = q\int n(z)dz \qquad V_{gs} = |V_{gs2} - V_{gs1}| = 50\ \text{meV} \tag{2}$$

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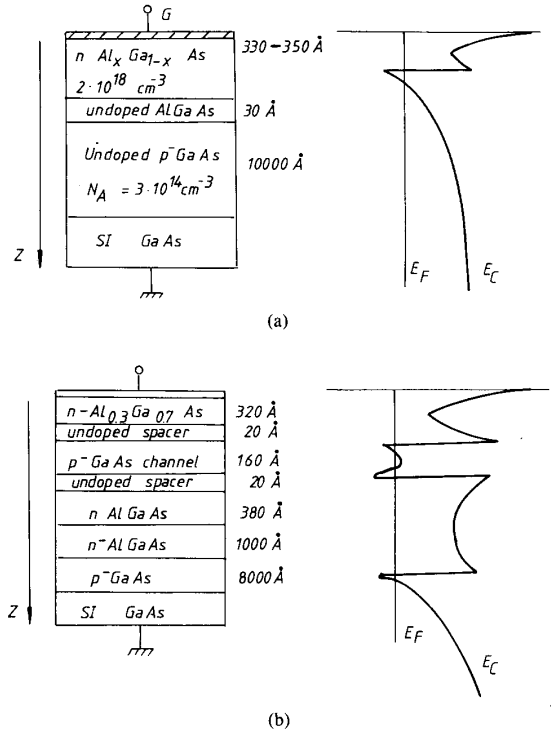

Fig. 1. Modulation-doped-heterostructure Schottky-gate capacitors. Layer sequence: (a) single-heterostructure capacitor; (b) triple-heterostructure capacitor.

in which the ionized donor impurity and electron profiles are obtained either by self-consistently solving the coupled Schrödinger and Poisson equations (quantum model)

$$\frac{-\hbar^2}{2}\frac{d}{dz}\left[\frac{1}{m_e(z)}\frac{d\psi_i(z)}{dz}\right] + [u(z) - E_i]\psi_i(z) = 0 \quad (3)$$

$$\frac{d}{dz}\left[\epsilon_0\epsilon_s(z)\frac{du(z)}{dz}\right] = q\sum_{i=0} N_i|\psi_i(z)|^2 - \rho(z) \quad (4)$$

$$N_i(z) = m_e(E_i - V(z))[kT/(\hbar^2)] \cdot \ln\left\{1 + \exp\left[(E_F - E_i)/(kT)\right]\right\} \quad (5)$$

$$\rho(z) = q[N_D^+(z) - N_A(z) - n_B(z) + p(z)] \quad (6)$$

or by employing the 3-D Fermi–Dirac distribution to solve the Poisson equation ("classical" model) in which the sum term in the right-hand side (RHS) of (4) disappears.

Equation (5) describes the occupancy of the ith electron subband in the quantum well and includes energy-dependent mass effects. $n_B(z)$ in (6) refers to the 3-D free-electron charge present in the barrier layers and is considered only in those regions of the device where the conduction band is at least $2kT$ above the highest energy subband of the well.

As compared to previous quantum analyses of the 2-DEG [6]–[10], the present approach features the dependence of carrier mass on energy (a third-order Taylor expansion) and deep and shallow donor levels:

$$m_e(E - V) = (0.0665 + 0.0436(E - V) + 0.0236 \cdot (E - V)^2 - 0.147(E - V)^3)m_0 \quad (7)$$

$$N_D^+(z) = sN_D(z)/\left\{1 + 2 \cdot \exp\left[-(E_C - E_F - E_{Dsh})/kT\right]\right\} + (1 - s)N_D(z)/\left\{1 + 2 \cdot \exp\left[-(E_C - E_F - E_{Dd})/kT\right]\right\} \quad (8)$$

where m_0 is the free-electron mass, E_{Dsh} (40–50 meV) and E_{Dd} (0.4–0.6 eV) are the energy levels of the shallow and deep donors relative to the bottom of the conduction band, respectively, and s describes the proportion of shallow and deep donors in the overall impurity concentration. To make the results of Section IV more easily tractable, only shallow donors have been considered in the present calculations, i.e., $s = 1$. A detailed account of the numeric procedure can be found in [11], and only the main points will be reviewed here.

The Schrödinger and Poisson equations are alternately solved with an iterative fast-converging Newton scheme until the potential update from the previous iteration drops below 10^{-6} V. In the conventional SH structure (Fig. 1(a)) a floating boundary is imposed to the Schrödinger equation, i.e., ψ_i and $(1/m)d\psi_i/dz$ must be continuous at the fixed hetero-interface and floating-bulk boundaries. The latter boundary shifts toward the substrate as the eigen energies considered in the Schrödinger equation become larger. Outside the bounded region, the wave functions are evaluated by the WKB approximation. As mentioned earlier, for regions where the conduction band rises by $2kT$ above the highest eigen energy of the well, the 3-D Fermi–Dirac electron distribution is added to the quantum electron distribution to obtain the free-electron charge $n(z)$. The usual Schottky-contact boundary condition is assumed in the Poisson equation, which is solved throughout the device. For the substrate boundary, either a fixed potential or zero electric field ($du/dz = 0$) is considered. Although not strictly accurate, this computational scheme enjoys the advantage of very high speed (because of the economic mesh deployed in the Schrödinger equation, the computer time spent in this equation is only two to three times longer than in the Poisson equation) and still accurately predicts wave-function tunneling into the barrier layers and smooth electron profiles at the heterointerface. In the multiple-heterostructure (MH) capacitor (Fig. 1(b)), a similar strategy is employed, but the Schrödinger equation is solved separately in the two uncoupled channels. It must be remarked at this point that a rigorous analysis of any MDH capacitor or FET requires the Schrödinger equation to be solved throughout the device and no 3-D electrons to be involved in the computation. Such an approach is very difficult because sepa-

ration of the higher eigen energies of a "quantum well," usually larger than 0.5 μm, may prove a formidable task and is surely impaired by the discretization error introduced by the finite mesh refinement available with current computers.

The algorithm resumed above has been implemented in Pascal on IBM-PC-compatible and PDP-11 computers. Simulations have been performed with a nonuniform one-dimensional mesh of 200–500 points. Mesh refinement has been optimized for each structure in order to minimize discretization errors.

III. Analysis of the Electron Charge Distribution

The first step in the derivation of the capacitance and transconductance characteristics is the calculation of the electron distribution in the channel(s) and barrier(s). It is interesting to notice that, for room-temperature SH capacitors, 15 to 20 eigen energies are considered in the channel so that the occupancy of the highest subband should be less than 1 percent of the total 2-DEG charge. This finding strongly challenges the usual assumption that only the two lowest subbands are occupied. The latter may be true of narrow quantum-well devices (QW-MODFET's) [12] and/or 77 K operation. In the room-temperature SH device, the number of occupied subbands considered in calculations is important for the values of the resulting eigen energies, but, due to the strong feedback effect between the Schrödinger and Poisson equations, it hardly affects the value of the overall 2-DEG channel charge. In essence, the potential and donor profiles adjust themselves to compensate for changes in the 2-DEG. This explains the minor differences (below 1 percent) between the integral of the electron charge in the device computed with energy-dependent mass and effective-mass approximation models, despite a difference of as much as 5–8 percent in eigen energies. Since the operation of a MODFET is essentially three dimensional and of a macroscopic nature (at least source–drain conduction), the values and number of the eigen energies in the channel are, in a first-order approximation, unimportant as long as the electron profile is well predicted and a conventional experiment-fitted mobility is employed to model source–drain conduction.

To support these assertions, Figs. 2 and 3 present "quantum" and "classic" derivations of the electron profiles in single quantum-well (QW) capacitors and FET's [12]. (These devices lack the substrate channel present in Fig. 1(b).) Note that, due to the well profile, these devices show a more pronounced quantum nature than previously investigated SH structures [11], and a large difference between the results of the two models is expected. However, the error associated with the "classic" approach does not rise above 8 percent, and, for wide wells (>150 Å), the charge profile even follows the "quantum" one. For narrow wells (Fig. 3) the two models predict totally different distributions, but the overall charge is roughly the same. This is a consequence of the fact that the integral of the free-electron charge in the direction perpendicular to the heterointerface is determined by the gate voltage and doping profile and hardly at all by the width of the well. As a confirmation, computations have revealed that the substrate potential (back bias) has more influence on the computed overall charge than the number (set by the well profile) and values (dependent on Fermi level) of the subband levels. For the design of QW-FET's (single- or multiple-channel [12]–[15]) this suggests that narrow channels should be favored because in such devices the largest percentage of channel electrons reside in the high-mobility ground level and barrier tunneling is insignificant.

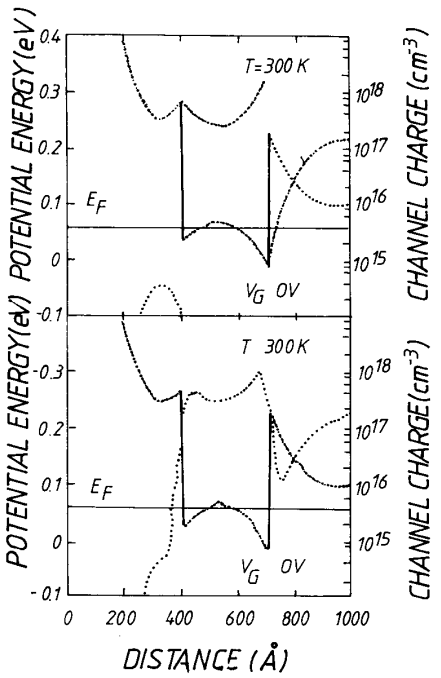

Fig. 2. Conduction band and free-electron charge profiles in a double-heterostructure (Al_xGa_{1-x})As/GaAs capacitor having the following layer sequence (Z_i indicates distance from the gate while N_i represents the doping of the layer that terminates at Z_i):

Zd_1 = 390 Å; $N_{D1} = 10^{18}$ cm^{-3}; ($Al_xGa_{1-x}As$) $x = 0.3$

$Zint_1$ = 400 Å; $N_{D2} = 10^{15}$ cm^{-3}; ($Al_xGa_{1-x}As$) $x = 0.3$

$Zint_2$ = 700 Å; $N_A = 10^{14}$ cm^{-3}; (GaAs)

Zd_2 = 710 Å; $N_{D2} = 10^{15}$ cm^{-3}; ($Al_xGa_{1-x}As$) $x = 0.3$

Zd_3 = 2000 Å; $N_{D3} = 10^{18}$ cm^{-3}; ($Al_xGa_{1-x}As$) $x = 0.3$

The substrate is 0.2 μm from the gate, and the well width is 300 Å. The "classic" results are presented in the upper plot while the "quantum" profiles are shown in the bottom picture.

IV. Gate Capacitance and Transconductance Characteristics

In a short-channel MODFET the saturation current is, with good approximation, linearly dependent on Q_n so that the following expression holds [16]:

$$C_n(V_{gs}) = g_m(V_{gs})/(Wv_{sat}) \tag{9}$$

where W is the gate width.

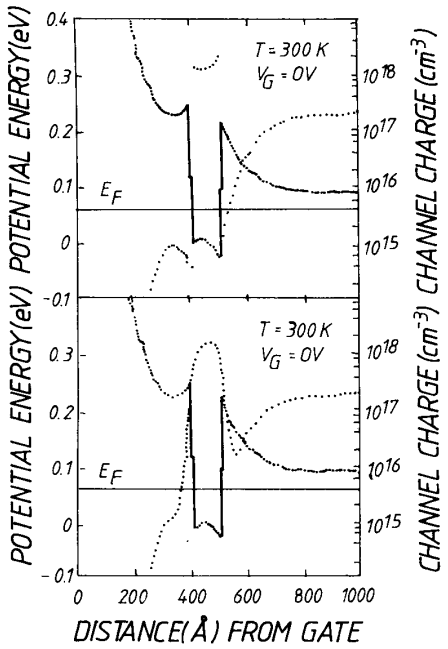

Fig. 3. Conduction band and free-electron charge profiles in a double-heterostructure (Al_xGa_{1-x})As/GaAs capacitor having the following layer sequence:

Zd_1 = 390 Å; $N_{D1} = 10^{18}$ cm^{-3}; ($Al_xGa_{1-x}As$) x = 0.3

$Zint_1$ = 400 Å; $N_{D2} = 10^{15}$ cm^{-3}; ($Al_xGa_{1-x}As$) x = 0.3

$Zint_2$ = 500 Å; $N_A = 10^{14}$ cm^{-3}; (GaAs)

Zd_2 = 510 Å; $N_{D2} = 10^{15}$ cm^{-3}; ($Al_xGa_{1-x}As$) x = 0.3

Zd_3 = 2000 Å; $N_{D3} = 10^{18}$ cm^{-3}; ($Al_xGa_{1-x}As$) x = 0.3

The substrate is 0.2 μm from the gate, and the well width is 100 Å. The "classic" results are presented in the top plot while the "quantum" profiles are shown in the bottom picture.

Equations (1), (2), and (9) allow for a reliable prediction of the microwave performance of MODFET's simply by carrying out dc calculations on the corresponding MDH capacitor.

$C_n(V_{gs})$ is not directly measureable, and, for that matter, in some cases, the transconductance will be derived instead. In this way, the plotted results will not detract from the effects caused by the intrinsic charge dynamics, and a qualitative comparison with Maloney *et al.*'s measurements [5] and other transconductance data [16] can be made.

A. Single MDH Capacitors and FET's

Fig. 4 reproduces the experimental high-frequency (thick line) and analytically derived (dc: dashed line and high frequency: dashed-dotted line) C_T–V_{gs} characteristics of a 100 μm × 2 μm gate SH-MODFET, as presented by Moloney *et al.* [5]. Results obtained with our low-frequency quantum model (dotted line) are also included and exhibit excellent agreement with the experimental hf curve in the threshold region. To support the ensuing discussion, quantum and "classic" computations of $C_T(V_{gs})$ and

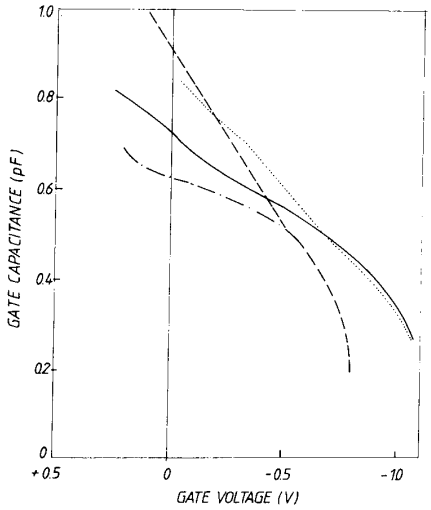

Fig. 4. The theoretical and experimental C_T–V_{gs} characteristics of the SH-MODFET analyzed by Moloney *et al.* [5]. The present low-frequency (lf) results are shown by a dotted line. The experimental high-frequency (hf) curve (solid line), and analytical hf (dashed-dotted line) and dc (dashed line) curves are reproduced from the plot of Moloney *et al.* [5].

$C_n(V_{gs})$ for a slightly different single MDH capacitor are shown in Fig. 5. In view of the previous section, it comes as no surprise that the "classical" approach slightly overestimates the ac performance (it predicts lower C_T (dashed line) and higher C_n (thin line) values). The individual error does not exceed 5 percent at room temperature and leads to an overestimation of the cutoff frequency by at most 10 percent. Note that all of the features of the "quantum" traces are also present in the "classic" ones.

The results of Figs. 4 and 5 support Moloney *et al.*'s model and can be explained as follows. In the threshold region (large negative gate bias), capacitance and transconductance (C_n) are identical because only channel (2-DEG) electrons contribute to the charge dynamics.

Since the channel is virtually depleted, the center of mass of the electron distribution is located far away from the interface resulting in low capacitance and transconductance. When the reverse gate bias decreases, the electrons respond by shifting closer to the heterointerface and the 2-DEG concentration rises rapidly in the channel. This free charge movement causes a sharp increase in capacitance and transconductance. The ionized donors in the barrier remain unaffected because the donor level is still far above the Fermi level. Consequently, the low-frequency and high-frequency gate capacitance, as well as the free-electron charge capacitance (transconductance) characteristics, are virtually identical, as in Figs. 4 and 5.

With a further increase in gate bias, the 2-DEG concentration continues to rise, but the mass centroid's drift slows down as it already is very close to the heterointerface. This trend manifests itself in a softer slope of the $C_T(V_{gs})$ characteristics and in transconductance saturation. The length of this second region depends on temperature and donor level energy, as clearly indicated in

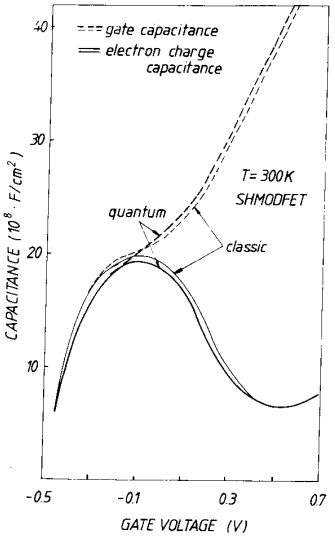

Fig. 5. "Quantum" and "classic" derivation of the gate capacitance and free-electron charge capacitance of an SH-MODFET having the following layer sequence:

Zd_1 = 400 Å; $N_{D1} = 10^{18}$ cm^{-3}; $(Al_xGa_{1-x}As)$ $x = 0.3$

Zint = 420 Å; $N_{D2} = 10^{15}$ cm^{-3}; $(Al_xGa_{1-x}As)$ $x = 0.3$

Zsub = 10000 Å; $N_A = 10^{14}$ cm^{-3}; (GaAs)

Figs. 6 and 7, and can be regarded as a valuable check for device design and fabrication quality. The wider the gate bias range of this region, the smaller the chance of parasitic channel formation in the barrier layer. It is well known that parasitic channel formation is always present at room temperature, as evidenced in Fig. 6, and less significant at 77 K (Fig. 7), when the device operation is nearly ideal. Measurements at 77 K may be used to determine the donor level energy from the length of the mild-slope zone.

When the gate bias is further shifted toward positive values, the increase in the 2-DEG concentration is partially quenched by the neutralization of donors and the emergence of the 3-D electron charge in the barrier layer. This phenomenon appears earlier at 300 K (immediately after transconductance saturation) and is characterized by a renewed steep rise of the $C_T(V_{gs})$ characteristic and a sharp drop in $C_n(V_{gs})$ (so-called "transconductance degradation"). Because of the involvement of the slow-response donors in the charge dynamics, the low-frequency and high-frequency gate capacitance curves no longer match and, consequently, the present dc model overestimates the hf capacitance in this region (Fig. 4).

Calculations have shown that donor neutralization and parasitic channel formation take place simultaneously. To confirm this, lf and hf capacitance characteristics should be measured at diverse temperatures (77–300 K) and the length of the second region should be monitored as a function of frequency.

In normally-on FET's, an additional fourth region was observed at positive bias ($V_{gs} > 0.4$ V), and it features

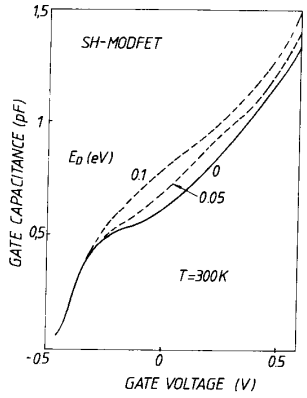

Fig. 6. The 300 K gate capacitance characteristics of a single MDH capacitor as a function of the donor level energy. The 2 μm × 100 μm structure has the following composition:

Zd_1 = 300 Å; $N_{D1} = 2 \times 10^{18}$ cm^{-3}; $(Al_xGa_{1-x}As)$ $x = 0.24$

Zint = 320 Å; $N_{D2} = 10^{15}$ cm^{-3}; $(Al_xGa_{1-x}As)$ $x = 0.24$

Zsub = 10000 Å; $N_A = 5 \times 10^{14}$ cm^{-3}; (GaAs)

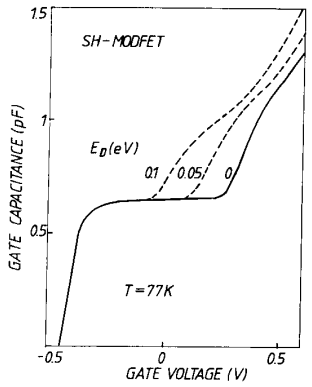

Fig. 7. The 77 K gate capacitance characteristics of a single MDH capacitor as a function of the donor level energy. The 2 μm × 100 μm structure is identical to that of Fig. 6.

a secondary transconductance peak (much lower than the main one) as a result of the renewed increase in the 2-DEG concentration [5]. This trend is predicted by the present model, despite the fact that a constant Fermi level is assumed throughout the simulated structures at all bias voltages. Similar results were obtained by Moloney *et al.* [5] who allowed for a variable Fermi level at high positive gate bias.

B. Multiple MDH Capacitors and FET's

A typical multiple modulation-doped heterostructure is sketched in Fig. 1(b). Although newer than the established SH-MODFET, these devices have proliferated in the last few years [12]–[16] due to their enhanced current-driving capability and are known in the literature under several acronyms. When containing rectangular well channels (Figs. 2 and 3), the common usage is single or multiple quantum-well MODFET. For devices having a

combination of rectangular and triangular wells, the name multiple-heterojunction MODFET is favored in this work (Fig. 1(b)).

Fig. 8 shows the computed gate capacitance and transconductance of the MH capacitor structure from Fig. 1(b) at 300 and 77 K. The transconductance was computed assuming velocity saturation in a 2 × 100 μm gate FET. To highlight the charge dynamics, the same values of the saturation velocity were used at 77 and 300 K, i.e., $v_{sat} = 1.4 \times 10^7$ cm/s in GaAs and $v_{sat} = 10^7$ cm/s in AlGaAs. These values may be argued against (indeed, carriers in a 2-μm device may not travel at saturation velocity near the source end of the gate), but they have been retained solely for the purpose of maintaining compatibility with the results in [5] and the preceding SH-MODFET calculations. The calculated $g_m(V_{gs})$ and $C_n(V_{gs})$ profiles are identical within a multiplicative constant. The higher transconductance predicted at 77 K is purely a result of the favorable charge dynamics (less parasitic conductance). The transconductance of the actual device will be even higher due to the larger electron velocity at 77 K.

Experimental support for these results are provided in [14] and [15]. Although a quantitative agreement cannot be expected because the cited publications refer to structures having more channels and superlattice buffer layers, the transconductance curves have remarkably similar profiles. They all exhibit a staircase characteristic, each step being associated with the activation of a particular channel. At room temperature, as in the SH device, the special features of the capacitance and transconductance behavior are smeared out by donor neutralization and barrier electrons. At 77 K, however, the gate capacitance exhibits three distinct regions in which the capacitance is nearly constant, each of them linked to electron accumulation at the three heterointerfaces. The transconductance presents a lower value quasi-saturation associated with the population of the substrate triangular well and a large maximum related to the accumulation of the rectangular well positioned close to the gate. A recent publication [17] presents analytically derived 300 K C–V characteristics of a QW-MODFET that show a hardly detectable staircase nature, left unexplained.

The behavior of the capacitance and transconductance in multiple-channel devices can be understood as follows. At very large negative bias, all channels are depleted. Increasing the voltage, the threshold region is reached when the electrons quickly drift toward the first heterointerface (farthest away from the gate) and cause a sharp rise in capacitance and transconductance. The characteristics then saturate as the electrons accumulate at the first heterointerface. A further shift in gate bias activates the second interface and the capacitance and transconductance characteristics resume the previous profiles at higher values (because the second interface and the mass centroid of the electron distribution are closer to the gate). This process repeats itself until the last heterointerface becomes accumulated with electrons. If the gate bias is again increased, the behavior becomes identical to that of SH

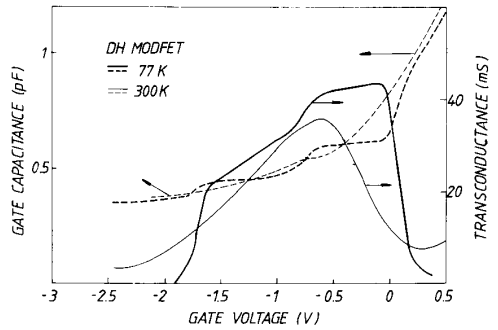

Fig. 8. Gate capacitance (dashed lines) and transconductance (solid lines) characteristics of a 2 μm × 100 μm gate MH-MODFET (see Fig. 1(b)) with the following layer sequence:

Zd_1 = 320 Å;	$N_{D1} = 2 \times 10^{18}$ cm^{-3};	$(Al_xGa_{1-x}As)$ $x = 0.24$
$Zint_1$ = 340 Å;	$N_{D2} = 10^{15}$ cm^{-3};	$(Al_xGa_{1-x}As)$ $x = 0.24$
$Zint_2$ = 500 Å;	$N_A = 3 \times 10^{14}$ cm^{-3};	(GaAs)
Zd_2 = 520 Å;	$N_{D2} = 10^{15}$ cm^{-3};	$(Al_xGa_{1-x}As)$ $x = 0.24$
Zd_3 = 900 Å;	$N_{D3} = 2 \times 10^{18}$ cm^{-3};	$(Al_xGa_{1-x}As)$ $x = 0.24$
$Zint_3$ = 2000 Å;	$N_{D2} = 10^{15}$ cm^{-3};	$(Al_xGa_{1-x}As)$ $x = 0.24$
Zsub = 10000 Å;	$N_A = 3 \times 10^{14}$ cm^{-3};	(GaAs)

devices, i.e., the gate barrier starts to deionize and to parasitically conduct, causing a sharp decrease in transconductance and a fast rise in capacitance.

At room temperature this behavior is further complicated by parasitic conduction in the intermediate barrier layers, smearing out the capacitance steps and even causing a "camel hump-back" transconductance characteristic [14].

Judging from the transconductance and gate capacitance characteristics presented in Figs. 5 and 8, the following conclusions may be drawn: 1) The transconductance degradation is mainly caused by the emergence of a parasitic channel in the barriers and to a lesser extent by the value of carrier mobility in those regions and source series resistance [12], although these two effects may further aggravate it. 2) Before the onset of parasitic channel formation, the capacitance and transconductance characteristics closely match, and the length of the region of high transconductance is mainly determined by the degree of barrier conduction and not by the shape of the quantum well. 3) Multiple-channel devices exhibit staircase-like characteristics that may find useful applications in multichannel charge-coupled circuits and n-ary logic.

V. Simulation of Experimental C–V Profiling

The C–V profiling technique is widely used for the experimental characterization of MESFET IC's and heterostructure devices [18]–[20]. A useful introduction to the numerical simulation of capacitance–voltage measurements, with applications to heterostructure capacitors, can be found in Gray and Lundstrom [18]. Although the importance of quantum-confinement effects was recognized, their study, like that of Jeong *et al.* [19], overlooks such

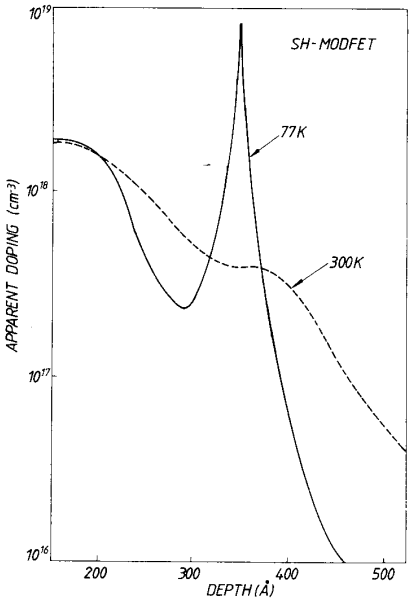

Fig. 9. Computed apparent doping profile of the structure analyzed in Fig. 6.

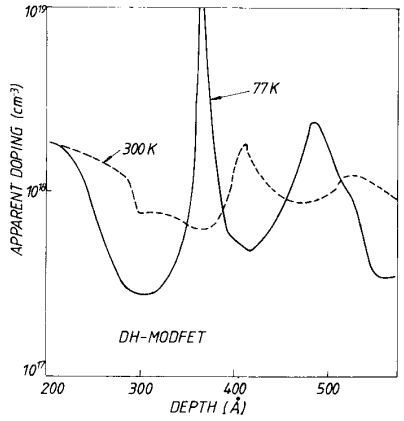

Fig. 10. Computed apparent doping profile of the structure analyzed in Fig. 8.

effects by classically solving the Poisson equation with 3-D Fermi–Dirac statistics. This section extends their approach to derive the apparent doping profile in various MDH FET's starting from the quantum-mechanically computed C_T–V_{gs} characteristics:

$$N_{\text{app}}(z_{\text{app}}) = \left[(q\epsilon_s\epsilon_0/2)d(1/C_T^2)/dV_{gs}\right]^{-1} \quad (10)$$

with $z_{\text{app}}(V_{gs}) = \epsilon_s\epsilon_0/C_T(V_{gs})$.

Figs. 9 and 10 contain the apparent doping results for the previously described SH- and MH-MODFET's. To the authors' knowledge, such profiles are computed here for the first time and they match the experiments carried out by Schubert *et al.* [20] on single-heterostructure MODFET's. Also, these plots present a confirmation of the accuracy of the numeric procedure, since they all predict the exact doping profile near the gate. Notice that, at 77 K, when parasitic conduction is very low, the position of the 2-DEG is correctly estimated and the distribution peak is very large (near or above 10^{19} cm^{-3}). At room temperature, quite a few electrons reside in the barrier layer(s), screening the 2-DEG channel(s). Consequently, no peak appears at the heterointerface in the SH device, while in the MH-FET the two peaks (corresponding to the two heterointerfaces of the rectangular well) are wider with a lower concentration and shifted toward the substrate. This is exactly opposite Schubert *et al.*'s [20] experimentally derived interpretations (see [20, Figs. 5 and 6]) who state that parasitic channel formation should be linked to a sharp peak in the apparent doping at the heterointerface. The present results and interpretation, sustained by "common sense" (a device having parasitic conduction at 77 K will surely exhibit it at 300 K), are also supported by the experimental and theoretical studies of Jeong *et al.* [19] who have investigated InGaAs/GaAs strained heterojunctions.

In any event, all three papers indicate that there are distinct profiles for devices with and without parasitic channels. One can conclude that, for a reliable experimental diagnosis, all three characteristics, i.e., $C_T(V_{gs})$, $C_n(V_{gs})$ and $N_{\text{app}}(z_{\text{app}})$ should be investigated and matched. Also, as evidenced in previous publications [19], [20], care must be taken when using the experimental apparent doping profile because it is prone to overestimate the channel electron charge in MODFET's without conduction (Fig. 9). Qualitatively, the apparent doping profile can reliably predict the level of parasitic conduction and the position and number of electron (or hole) channels in multiple-heterojunction devices.

VI. Conclusions

A thorough quantum-mechanical investigation of the charge distribution, capacitance–voltage, and transconductance–voltage characteristics of single- and multiple-MDH capacitors and FET's was performed. This study contributes to the understanding of MODFET's and has led to a number of important conclusions:

1) If errors of up to 10 percent are acceptable, classic simulation of MODFET's based on solving the Poisson equation should be preferred to the quantum one due to the former's higher speed and easier extension to 2-D and 3-D analyses.

2) Analytical models that include a numeric fit of the quantum-mechanically derived 2DEG and parasitic conduction in the barrier layers [5], [17], provide very good qualitative results of the capacitance and transconductance behavior.

3) Transconductance degradation is indeed accompanied by parallel parasitic channel formation in the barrier layer, but it is primarily a consequence of the intrinsic charge dynamics of MDH's (donor deionization and barrier electrons). The lower carrier mobility in the barriers and the source parasitic resistance can further aggravate the degradation as secondary causes.

4) The region of high transconductance is linked to the region of reduced capacitance variation with gate voltage, and both are dependent on the donor energy level and device temperature.

5) The gate capacitance–voltage characteristics of multiple heterojunction devices exhibit a staircase profile with steps associated with each heterointerface. This effect is more obvious at low temperatures [21] and should find useful applications in n-ary logic circuits, but it is liable to cause nonlinearities in analog devices.

6) The apparent doping profile, obtained from C–V measurements, qualitatively predicts the device quality by giving a clear indication of parasitic channel formation. The value of the channel charge should be used with caution since it is either overestimated or incorrectly located.

All these conclusions were derived theoretically, and experimental support was found in various publications. They were facilitated by the development of a very fast numerical procedure to integrate the Schrödinger and Poisson equations.

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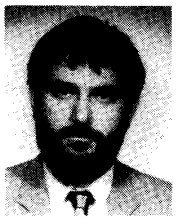

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