A Transmission-Line Based Technique for De-Embedding Noise Parameters

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***Abstract*— A transmission line-based de-embedding technique for on-wafer S parameter measurements is extended to the noise parameters of MOSFETs and HBTs. Since it accounts for the distributed effects of interconnect lines and for the pad-interconnect discontinuity, it is expected to yield more accurate results at high frequencies than existing approaches. Furthermore, by requiring only two transmission line test structures to de-embed all test structures in a (Bi)CMOS process, it is one of the most area-efficient. Experimental validation is provided on 90 nm and 130 nm n-MOSFETs and SiGe HBTs and its accuracy is compared with that of other lumped or distributed de-embedding techniques.**

I. Introduction

Accurate characterization of the noise parameters of active devices relies on the complete removal of test structure parasitics from the measured data. The limitations of a lumped-element approach and the need to account for the distributed nature of the interconnect linking the pads with the device have been recognized and different techniques have recently been developed based on a cascade configuration [1], [2] and a four-port parasitic model [3]. Although the techniques in [1], [3] account for the distributed effects, they require, respectively, three and five de-embedding structures for each device to be characterized. This results in a large area overhead, long testing times and becomes very expensive in nano-scale CMOS technologies. This paper expands on a recently proposed transmission line characterization technique [4], [5], to present a noise parameter de-embedding method that requires only two dummy structures to characterize the noise parameters of all the test structures fabricated on a wafer. The new technique differs from that in [2] in the method employed to obtain the characteristic impedance (Z_C) and the propagation constant (γ) of the transmission line. It is experimentally validated on 130 nm and 90 nm n-MOSFETs and on SiGe HBTs with f_T's of 150 GHz and 230 GHz, respectively, from two generations of 130 nm SiGe BiCMOS processes [6], [7].

II. Theory

A transistor test structure can be represented as a cascade of three two-port networks as shown in Fig. 1. The electrical and noise properties of the input and output networks, which are composed of the probe pads and the interconnects leading to the transistor, are described by their two-port network parameters and noise correlation matrices [8], with the notation defined in Fig. 1. The transistor is represented by its own two-port parameters and noise correlation matrix, $\mathbf{C_T^i}$. Two-port parameter and noise correlation matrix conversions are assumed implicitly for a concise presentation. For instance, both $\mathbf{Y_T}$ and $\mathbf{A_T}$ represent the transistor, but one is a Y-parameter representation and the other is an $ABCD$ parameter representation, likewise for $\mathbf{C_T^Y}$ and $\mathbf{C_T^A}$. Noise correlation matrix conversions are accomplished using the formulae in [8]. Figure 2 describes the dummy structures required for de-embedding and defines relevant symbols.

The noise parameter de-embedding technique can be separated into three major steps: (1) de-embedding the probe

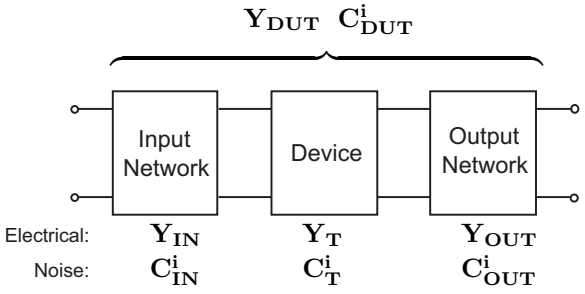

Fig. 1. A test structure modelled as a cascade of two-port networks. The superscript "i" denotes the representation (A: chain, Y: admittance, etc.) of the noise correlation matrix.

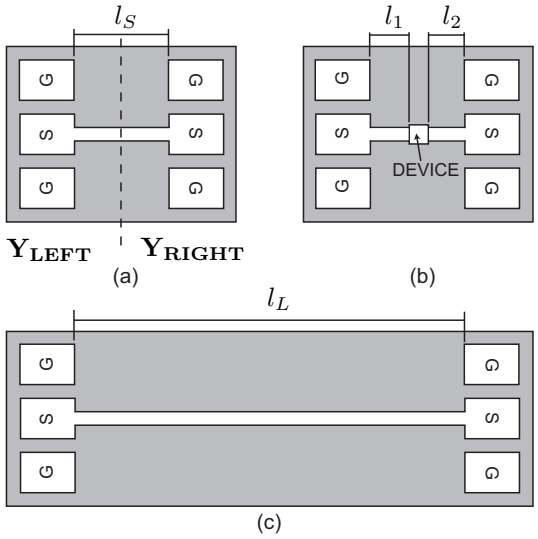

Fig. 2. Test structures required for noise parameter de-embedding. (a) short transmission line, (b) transistor test structure utilizing interconnects with the same width at the in the input and output ports, and (c) long transmission line.

pads from the transmission line test structures to obtain the characteristic impedance (Z_C) and propagation constant (γ), (2) splitting the short transmission line into two halves as illustrated in Fig. 2(a) and determining the matrices $\mathbf{Y_{LEFT}}$ and $\mathbf{Y_{RIGHT}}$, and (3) calculate the electrical and noise matrices of the input and output networks (*i.e.* $\mathbf{Y_{IN/OUT}}$ and $\mathbf{C^Y_{IN/OUT}}$) and de-embed their contributions from the measured noise parameters. The remainder of this section shall describe each of the three steps in sequence.

A. De-embedding the Transmission Line Test Structures

For simplicity, the interconnects at the input and output of the transistor are assumed to have the same width. A method to remove this restriction will be illustrated at the end of the last subsection.

In this work, the interconnects from the probe pads to the transistor are characterized as transmission lines. Z_C and γ of the interconnects are determined from two transmission line test structures of different lengths, but having the same width as the interconnects, using the technique described in [4].

B. Splitting Short Transmission Line Test Structure

Splitting the short transmission line test structure and calculating the electrical matrices of the two halves form the basis of the noise parameter de-embedding technique. The method used was presented in [5] and summarized in the remainder of this subsection.

From transmission line theory, the Y-parameters of a transmission line of length l are given by [9]

$$\mathbf{Y} = \frac{1}{Z_C}\begin{bmatrix} \coth\gamma l & -\mathrm{csch}\gamma l \\ -\mathrm{csch}\gamma l & \coth\gamma l \end{bmatrix}. \tag{1}$$

If the transmission line is short such that $|\gamma l| \ll 1$, then the hyperbolic functions can be approximated by the first non-zero term of their Maclaurin series expansion [5]. By approximating the probe pads as lumped elements (Y_P) and accounting for the pad-line discontinuity through (Z_D) as illustrated in Fig. 3, it can be shown that the Y-parameter matrix of the left half of the short transmission line, including the probe pads, is given by [5]

$$\mathbf{Y_{LEFT}} = \begin{bmatrix} y^S_{11} - y^S_{12} - \frac{\gamma l_S}{4Z_C} & 2y^S_{12} \\ 2y^S_{12} & \frac{\gamma l_S}{4Z_C} - 2y^S_{12} \end{bmatrix}, \tag{2}$$

where $\{y^S_{ij}\}$ are the measured Y-parameters of the short transmission line test structure before de-embedding and l_S is the length of the short transmission line. Since the left and right halves are mirror images of each other, $\mathbf{Y_{RIGHT}}$ can be obtained by simultaneously interchanging the rows and columns of $\mathbf{Y_{LEFT}}$ as

$$\mathbf{Y_{RIGHT}} = \mathbf{P} \times \mathbf{Y_{LEFT}} \times \mathbf{P}, \tag{3}$$

where $\mathbf{P}$ is the permutation matrix

$$\mathbf{P} = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}. \tag{4}$$

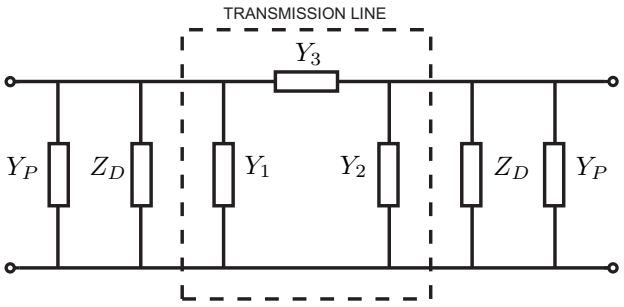

Fig. 3. Equivalent circuit model of a transmission line test structure. Note that the lumped pad approximation is the only assumption made. Any transmission line can be represented exactly by the π-network inside the dashed box by frequency dependent impedances, although the impedances may not be realizable with physical R, L, and C elements.

Since the short transmission line test structure is symmetric, its S-parameter matrix should also be symmetric. However, because of measurement errors, this is strictly not the case. In this work, the measurement error is handled by averaging the measured S-parameter matrix according to

$$s'_{11} = s'_{22} = \frac{s_{11} + s_{22}}{2} \tag{5}$$

$$s'_{12} = s'_{21} = \frac{s_{12} + s_{21}}{2}, \tag{6}$$

where the quantities without primes are the measured values. The averaged S-parameter matrices are used in (2) to calculate $\mathbf{Y_{LEFT}}$.

C. De-embedding Noise Parameters

The Y-parameter matrices of the input ($\mathbf{Y_{IN}}$) and output networks ($\mathbf{Y_{OUT}}$) have to be determined in order to de-embed the measured noise parameters. Based on the transmission line de-embedding technique summarized in section II-A, the input network is obtained by appending (or subtracting) a transmission line of length $|l_1 - l_S/2|$ to the network represented $\mathbf{Y_{LEFT}}$. Likewise, the matrix of the output network is calculated by appending (or subtracting) a $|l_2 - l_S/2|$ long line to $\mathbf{Y_{RIGHT}}$. Mathematically,

$$\mathbf{A_{IN}} = \mathbf{A_{LEFT}} \times \mathbf{A}_{l_1 - l_S/2} \tag{7}$$

$$\mathbf{A_{OUT}} = \mathbf{A}_{l_2 - l_S/2} \times \mathbf{A_{RIGHT}}, \tag{8}$$

where $\mathbf{A}_{l_1 - l_S/2}$ and $\mathbf{A}_{l_2 - l_S/2}$, respectively, are $ABCD$ matrices of intrinsic transmission lines of lengths $l_1 - l_S/2$ and $l_2 - l_S/2$ obtained from (1). Note that if $l_1 - l_S/2$ and/or $l_2 - l_S/2$ is negative, the above equations elegantly subtract the appropriate transmission length from $\mathbf{A_{LEFT}}$ and/or $\mathbf{A_{RIGHT}}$.

Since the input and output networks are passive, their noise correlation matrices can be determined from their Y-parameter matrices as in [10]

$$\mathbf{C^Y_{IN/OUT}} = k_B T \left(\mathbf{Y_{IN/OUT}} + \mathbf{Y^\dagger_{IN/OUT}} \right), \tag{9}$$

where † represents the conjugate-transpose (adjoint) operation. This equation, which reduces to $2k_BT\Re\{\mathbf{Y}\}$ if the real part

of the Y-parameter matrix is symmetric, ensures that the noise matrix is also symmetric even in the presence of measurement errors.

Having determined both the electrical and noise matrices of the input and output networks, the chain noise correlation matrix of the transistor from which the de-embedded noise parameters are calculated can be isolated as [8], [11]

$$\mathbf{C_T^A} = \mathbf{A_{IN}^{-1}}\left(\mathbf{C_{DUT}^A} - \mathbf{C_{IN}^A}\right)\left(\mathbf{A_{IN}^{\dagger}}\right)^{-1} - \mathbf{A_T}\mathbf{C_{OUT}^A}\mathbf{A_T^{\dagger}}. \tag{10}$$

$\mathbf{A_T}$ is the $ABCD$ parameter matrix of the transistor and can be calculated as

$$\mathbf{A_T} = \mathbf{A_{IN}^{-1}}\mathbf{A_{DUT}}\mathbf{A_{OUT}^{-1}} \tag{11}$$

and $\mathbf{C_{DUT}^A}$ is reconstructed from the measured noise parameters of the test structure using the formulae in [8], [11].

An additional pair of long and short transmission line test structures is necessary to remove the restriction that the interconnects at the input and output of the transistor have identical widths. $\mathbf{A_{IN}}$ and $\mathbf{C_{IN}^Y}$ are determined from the pair of transmission line test structures that have the same line width as the input interconnect. Likewise, $\mathbf{A_{OUT}}$ and $\mathbf{C_{OUT}^Y}$ are obtained from the lines whose width is identical to that of the output interconnect. The de-embedding technique will otherwise remain unchanged.

III. Results and Discussion

Verification of the proposed de-embedding technique is provided in two steps. First, electromagnetic simulations are employed to assess the accuracy of using (2) to split the short transmission line test structure. Next, the noise parameter de-embedding technique is verified experimentally on 90 nm and 130 nm n-MOSFETs and SiGe HBTs and compared to existing techniques.

A. Three Dimensional Electromagnetic Simulations

The error assoicated with using the approximation in (2) to split the short transmission line test structure was assessed using 3-D electromagnetic simulations. The S-parameters of the long and short transmission line test structures, together with the pads, were calculated using Ansoft HFSS. The transmission line de-embedding technique in [4] was applied to the simulated S-parameters to extract Z_C and γ, and (2) was applied to split the short transmission line test structure.

The simulated test structures have $40 \times 40 \mu\mathrm{m}^2$ signal pads. The length of the long line (l_L) is $600\mu\mathrm{m}$, while that of the short line (l_S) is $100\mu\mathrm{m}$. The transmission lines are $5\mu\mathrm{m}$ wide and $0.9\mu\mathrm{m}$ thick and the dielectric is $7\mu\mathrm{m}$ thick.

The S-parameters calculated from (2) are compared with those obtained directly from HFSS simulations in Figs. 4-6. The errors for the real and imaginary parts of each of the S-parameters are summarized in Table II. A validation of this de-embedding technique on the measured Y-parameters of MOSFETs, SiGe HBTs, inductors and varactors in the up to 65 GHz range will be presented in [12]. Below, we focus only on noise parameter measurements.

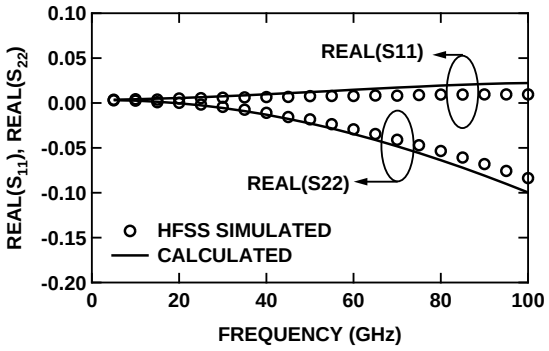

Fig. 4. Real parts of s_{11} and s_{22} of the left half of the splitted short transmission line test structure as calculated from (2): solid line and directly from HFSS simulations: symbols.

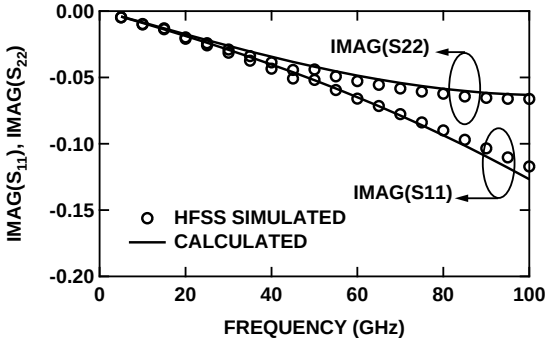

Fig. 5. Imaginary parts of s_{11} and s_{22} of the left half of the splitted short transmission line test structure as calculated from (2): solid line and directly from HFSS simulations: symbols.

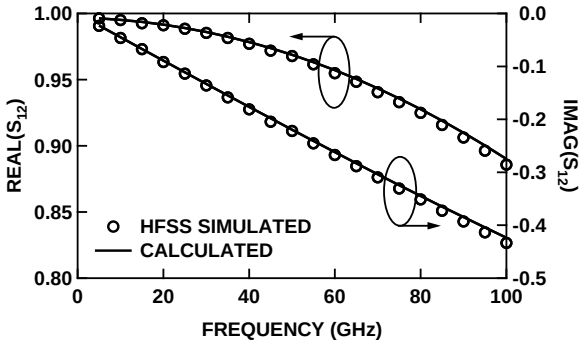

Fig. 6. s_{12} of the left half of the splitted short transmission line test structure as calculated from (2): solid line and directly from HFSS simulations: symbols.

TABLE I

Percentage error in the S-parameters due to (2)

Real	100 GHz	50 GHz	Imag	100 GHz	50 GHz
s_{11}	134.5%	60.2%	s_{11}	8.28%	0.48%
s_{22}	19.13%	25.29%	s_{22}	4.68%	4.72%
s_{12}	0.48%	0.103%	s_{12}	2.26%	1.08%

B. Experimental Verification

Figure 7 is a die photo of the SiGe HBT and n-MOSFET test structures and the necessary dummy structures fabricated to

TABLE II

ABSOLUTE ERROR IN THE S-PARAMETERS DUE TO (2)

Real	100 GHz ($\times 10^{-3}$)	50 GHz ($\times 10^{-3}$)	Imag	100 GHz ($\times 10^{-3}$)	50 GHz ($\times 10^{-3}$)
s_{11}	12.8	4.6	s_{11}	9.7	0.3
s_{22}	16.0	4.6	s_{22}	3.1	2.1
s_{12}	4.3	1.0	s_{12}	9.8	2.4

TABLE III

TEST STRUCTURE AND DEVICE GEOMETRIES

Tech./Device	W_E/l_G (μm)	l_E/W_F (μm)	N_E/N_F -	l_1 (μm)	l_2 (μm)
90 nm (n-FET)	0.1	1	80	34.935	34.555
130 nm (n-FET)	0.13	1	80	43.83	45.225
HBT [6]/ [13]	0.17/0.13	2.5	3	44.91	42.335

validate the new de-embedding technique. The geometries of the devices are summarized in Table III. All the test structures employ a M1 ground shield with abundant substrate PTAPs to reduce the substrate loss, as indicated by the shaded region in Fig. 2. The ground planes are slotted to comply with the metal density rules in nano-scale CMOS technologies.

S-parameters and noise parameters were measured on-wafer using a Wiltron 360B VNA, a Focus Microwaves tuner and a HP8971C noise figure test set. The open-short technique [14], the transmission line-based technique in [2] and the proposed technique were used to de-embed measured noise parameters. The measurement results summarized in Figs. 8-11 indicate that there is negligible difference between the three techniques for all noise parameters of SiGe HBTs and n-MOSFETs up to 26 GHz. This is expected, showing that the new technique agrees with previously published ones at low frequencies while consuming less silicon area. Note that the same pair of transmission lines is used to de-embed both the 130 nm MOSFETs and SiGe HBTs. The difference between the open-short technique and the new technique is expected to increase with frequency, since the lumped-element approximation will gradually fail as distributive effects become important.

Another observation is that the differences between the raw data and the de-embedded results are smaller for the 90 nm MOSFETs (Figs. 12-13) than for the 130 nm HBTs and MOSFETs (Figs. 8-11). In the 90 nm CMOS test chip, a metal 1 ground plane extends throughout the test structure, including under the high speed signal pads. In contrast, the signal pads in the 130 nm designs do not have a metal 1 ground shield directly underneath. This introduces extra losses, which translate into a higher measured noise figure of the test structure before de-embedding. While this loss can be de-embedded, measurement accuracy improves when the parasitic losses are minimized.

The importance of employing a ground plane is more evident by comparing the de-embedded NF_{MIN} of two generations of SiGe HBTs with exactly the same interconnect and pad layouts. Shown in Fig. 14 are the de-embedded NF_{MIN} data for two generations of SiGe HBTs [6], [13]. The NF_{MIN} of the newer generation HBT, [13] remains below 0.6 dB up to 22 GHz but exhibits significant fluctuations after the pad and interconnect losses are de-embedded due to a relatively larger contribution from the parasitics to the measured noise figure.

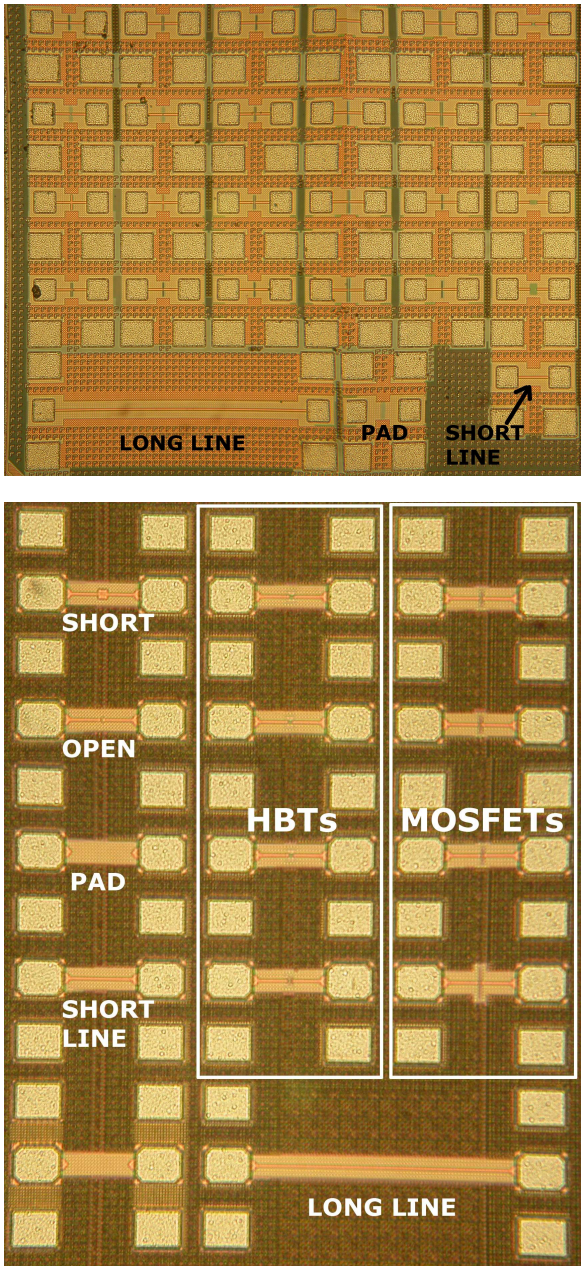

Fig. 7. Die photos of 90 nm CMOS (top) and 130 nm BiCMOS (bottom) test structures. Note that only one pair of transmission lines is necessary in each technology.

Finally, Fig. 14 confirms that the optimum noise bias of an n-MOSFET remains constant across frequencies, consistent with the results reported in [15]. The minimum noise bias of the 150 GHz SiGe HBT in [6] shifts to higher current densities with increasing frequency. However, this trend is drowned in the relatively larger scatter in NF_{MIN} data for the 230 GHz SiGe HBT in [13] due to the aforementioned parasitic losses and due to the device noise figure being lower than 1 dB.

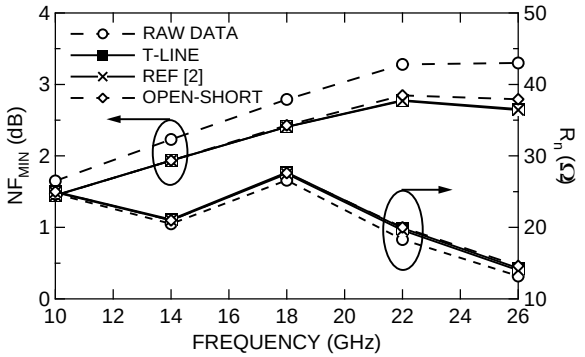

Fig. 8. NF_{MIN} and R_n of the 130 nm n-FET. $J_D = 0.15\mathrm{mA}/\mu\mathrm{m}$ and V_{DS}=1 V

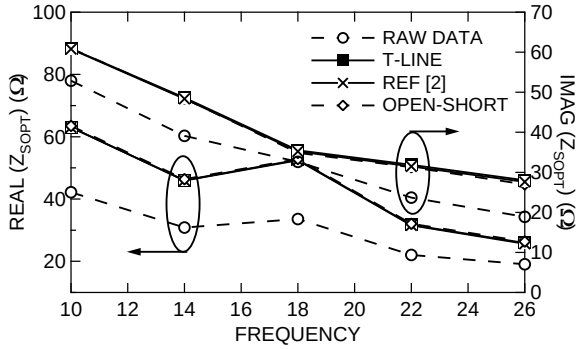

Fig. 9. Z_{SOPT} of the 130 nm n-FET. $J_D = 0.15\mathrm{mA}/\mu\mathrm{m}$ and V_{DS}=1 V

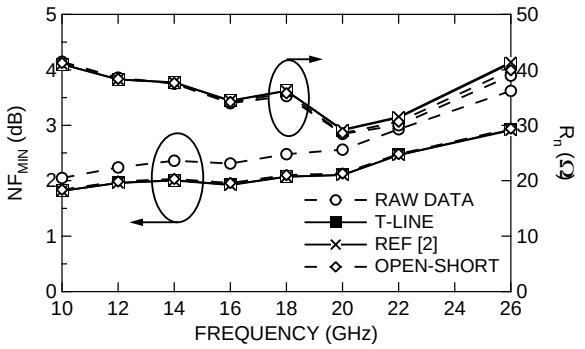

Fig. 10. NF_{MIN} and R_n of the SiGe HBT [6]. $I_C = 1\mathrm{mA}$ and V_{CE}=1 V

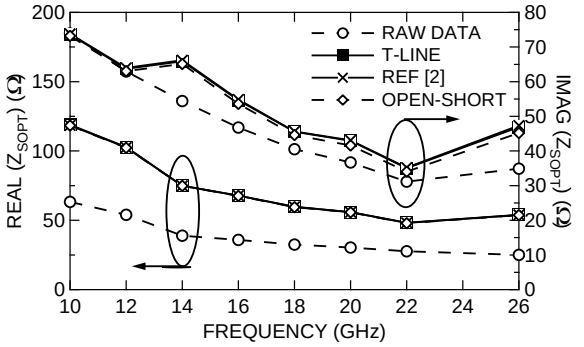

Fig. 11. Z_{SOPT} of the SiGe HBT [6]. $I_C = 1\mathrm{mA}$ and V_{CE}=1 V

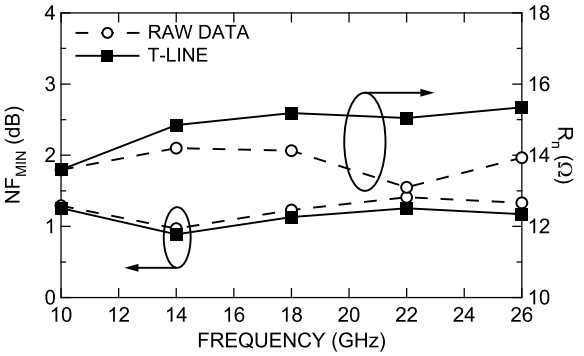

Fig. 12. NF_{MIN} and R_n of the 90 nm n-FET. $J_D = 0.15\mathrm{mA}/\mu\mathrm{m}$ and V_{DS}=0.7 V

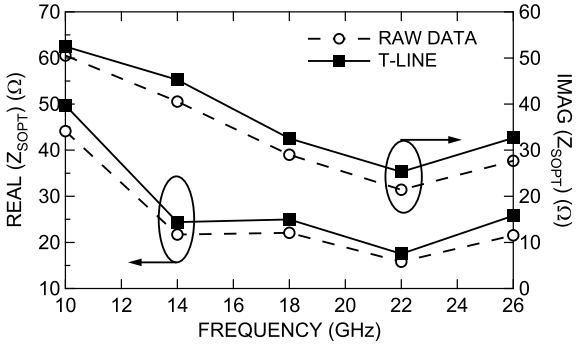

Fig. 13. Z_{SOPT} of the 90 nm n-FET. $J_D = 0.15\mathrm{mA}/\mu\mathrm{m}$ and V_{DS}=0.7 V

IV. Conclusions

A transmission line de-embedding technique was extended to de-embed the noise parameters of FETs and HBTs. Its accuracy was assessed using electromagnetic simulations and tested experimentally on 90 nm and 130 nm n-MOSFETs and on 150 GHz and 230 GHz SiGe HBTs from two generations of SiGe BiCMOS processes. Measurement results indicate that this technique agrees with existing ones up to 26 GHz, while consuming less silicon area and requiring fewer dummy test structures and fewer S-parameter measurements. Furthermore, compared to existing lumped element-based de-embedding techniques, because of its distributed nature, its accuracy is expected to be better at higher frequencies. Finally, the importance of minimizing the parasitic losses of the test structures for accurate measurements was also demonstrated.

Acknowledgements

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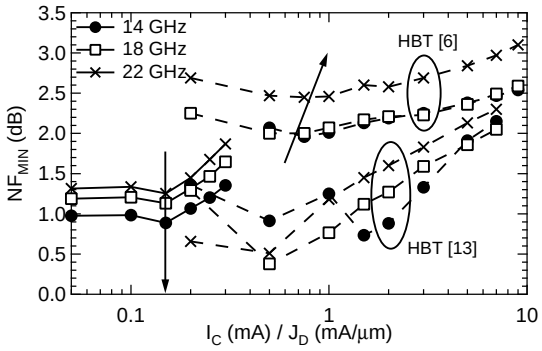

Fig. 14. NF_{MIN} vs. Bias for a 90 nm n-MOSFET (solid lines), a 130 nm SiGe BiCMOS HBT (dashed lines) [6] and a scaled 130 nm-based SiGe HBT (dashed lines) [13].

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