A 3-V Fully Differential Distributed Limiting Driver for 40-Gb/s Optical Transmission Systems

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***Abstract*—A fully differential 40-Gb/s electro-absorption modulator driver is presented. Based on a distributed limiting architecture, the circuit can supply up to 3.0-V_{pp} (peak-to-peak) per side in a 50-Ω load at data rates as high as 44 Gb/s. Both the input and the output are internally matched to 50 Ω and exhibit return loss of better than 10 dB up to 50 GHz. Additional features of the driver include the use of a single −5.2-V supply, output swing control (1.7–3.0-V_{pp} per side), dc output offset control (−0.15 V to −1.1 V), and pulsewidth control (30% to 66%). The driver architecture was optimized based on a comprehensive analytical derivation of the frequency response of cascaded source-coupled field-effect transistor logic blocks using both single and double source-follower topologies.**

***Index Terms*—Analog integrated circuits, differential amplifiers, high-speed integrated circuits, integrated circuit design, modulator driver, optical fiber communication, optical transmitters, source-coupled FET logic (SCFL).**

I. Introduction

HIGH-PERFORMANCE low-cost physical layer integrated circuits are essential for the successful implementation of next-generation 40-Gb/s optical communication systems. To realize an advantage over current wavelength-division-multiplexing (WDM) technology, these data rates must be achieved at the single-channel level. This prerequisite imposes significant technological demands on the front-end electro-optical interface (EOI) components.

Modulator drivers are a case in point. Not only must they operate at the high data rates, but they must deliver high voltage levels as well. For conventional Mach–Zehnder (MZ) or electro-absorption (EA) devices to achieve adequate extinction ratios and, thus, reach, these modulators must be driven by signals having a swing of at least 3–5 V_{pp} (peak-to-peak) per side. For 40-Gb/s driver applications, the only devices that have so far demonstrated the requisite characteristics are GaAs pseudomorphic high electron mobility transistors (pHEMTs) and InP double heterojunction bipolar transistors (DHBTs) [1]. SiGe HBTs with f_T values beyond 210 GHz have also been suggested, due to their reproducibility, high yield, and low cost [2]–[4]. However, there are significant concerns regarding their long-term reliability because they exhibit base–emitter (BV_{CEO}) and base–collector (BV_{CBO}) breakdown voltages lower than 2 and 6 V, respectively. They also operate at high current densities of 6 mA/μm^2 or more and suffer from significant self-heating at peak f_T bias [4]. In the case of an output stage having 3 V_{pp}, the SiGe HBT would be biased beyond BV_{CEO}, an operating region in which reliability is not guaranteed by manufacturers.

To date, almost all of the reported 40-Gb/s modulator drivers are based on AlGaAs–InGaAs pHEMTs with gate lengths in the range of 0.1 to 0.2 μm [5], [6]. In spite of its low f_T of approximately 100 GHz, this technology is by far the most attractive for this application. Not only does it have a high breakdown voltage of 6 V and an f_{MAX} of approximately 200 GHz, it has proven yield and reliability, as well as the capacity to be manufactured on 6-in wafers. To overcome the f_T limitation, however, the output stage of the driver must be based on a distributed amplifier topology, possibly with cascode gain stages. This will extend the high-frequency performance of the device, ensure good broad-band input/output impedance matching, and also achieve the required output swing.

In this paper, the first full-featured differential GaAs pHEMT modulator driver is presented. It consists of a lumped predriver circuit followed by a five-stage distributed amplifier (DA). Compared to previously reported 40-Gb/s drivers, the latter section of the present design is based on a differential distributed limiting architecture, rather than the more conventional single-ended linear approach. As a result, the circuit can significantly exceed its small-signal bandwidth when operated under large-signal conditions. The limiting architecture also simplifies the inclusion of output swing control, dc output offset control, and pulsewidth control.

II. Device Modeling

Unlike conventional linear drivers, which are based on a relatively small number of device geometries operated in saturation, the differential limiting architecture calls for a nonlinear device model that scales accurately over a wide range of gate widths and bias levels. In order to develop a realistic specification for the driver's performance, it should scale with temperature as well. To this end, a fully scalable nonlinear model was developed using Agilent's EEHEMT implementation. The nominal model values were derived from S-parameters and dc I–V curves that were measured over five different gate widths and using conventional extraction techniques for both the extrinsic and intrinsic circuit elements. By carefully adjusting the model parameters based on the five extractions, it is possible to obtain good agreement over all of the measured gate geometries.

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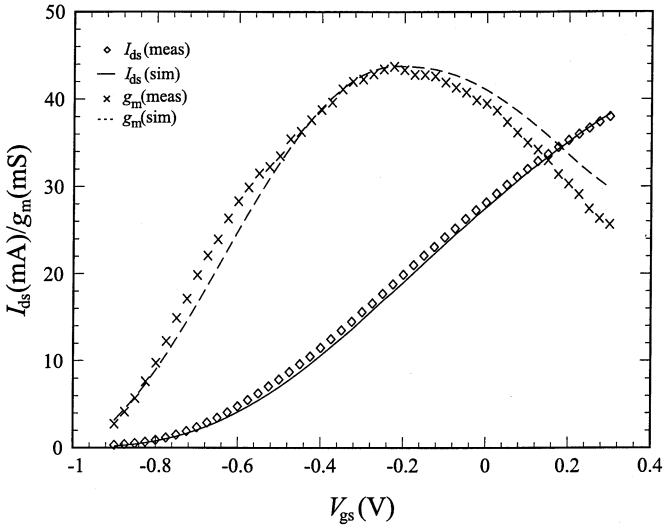

Fig. 1. Measured versus simulated drain current and transconductance for a 2×40 μm GaAs pHEMT biased at $V_{ds} = 2.5$ V.

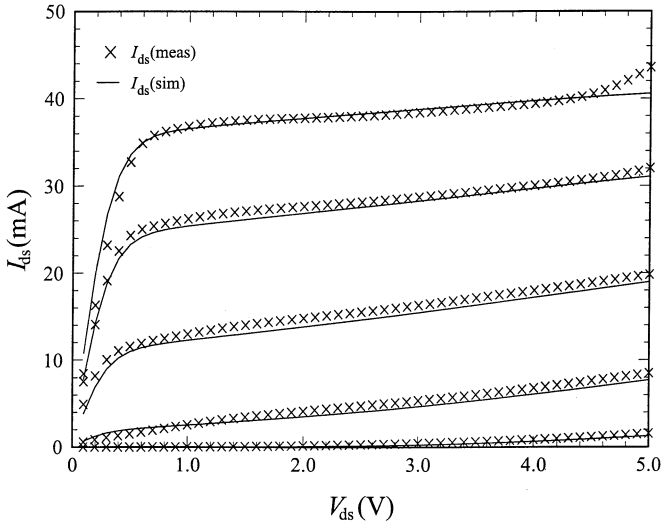

Fig. 2. Measured versus simulated dc output characteristics for a 2×40 μm GaAs pHEMT.

As an example of the quality of the extracted model, Figs. 1 and 2 present measured versus simulated dc characteristics for a transistor having a 2×40 μm gate geometry. By scaling the model parameters with finger width and number of fingers, a similar fit can be obtained for all five gate geometries. Fig. 3 compares the measured and simulated f_T–I_{ds} characteristics at $V_{ds} = 2.5$ V for different transistor sizes, while peak f_T values are presented in Fig. 4 as a function of gate width and temperature for $V_{ds} = 1.5$ V and $V_{gs} = -0.1$ V. Over the entire range, the measured and modeled peak f_T values are no more than 10% apart. The temperature dependence in the model has been extracted empirically from device measurements made at 18 °C and 100 °C. Table I summarizes the main scalable model parameters that characterize the small-signal equivalent circuit of the transistor.

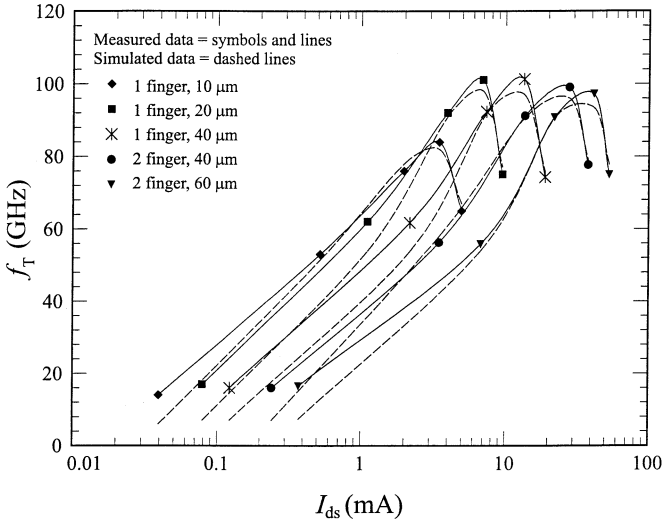

Fig. 3. Measured versus simulated f_T-I_{ds} characteristics of 1×10 μm, 1×20 μm, 1×40 μm, 2×40 μm, and 2×60 μm GaAs pHEMTs at 18 °C and $V_{ds} = 2.5$ V.

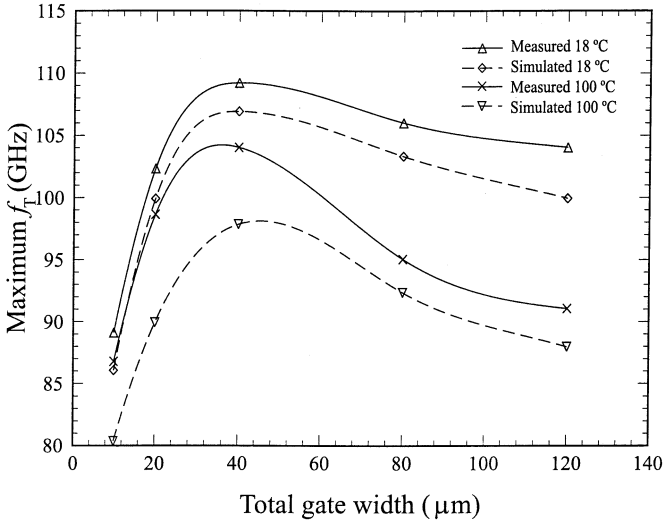

Fig. 4. Measured and simulated maximum f_T values versus total gate width and temperature for $V_{ds} = 1.5$ V and $V_{gs} = -0.1$ V.

III. Circuit Design

A. General Architecture

A block diagram of the differential limiting driver is shown in Fig. 5. It includes three gain blocks, namely, a lumped input amplifier, a lumped middle-stage amplifier, and a distributed output amplifier block, all of which operate from a single −5.2 V supply. The lumped amplifier blocks and the distributed amplifier sections all consist of a double source-follower stage with level-shifting diodes and a differential inverter. To enable the modulator to achieve its optimal performance, the driver also includes variable output amplitude (VOA), variable EA modulator offset (VEA), and adjustable duty-cycle distortion (DCD) or pulsewidth control.

The input stage features on-chip 50-Ω resistors to provide good input match and is self-biased at a level of −4 V. For an input signal of 0.5 V_{pp} per side, this stage provides an output swing of 1.0 V_{pp} per side. This signal is then amplified and

TABLE I
0.15-μm GaAs pHEMT SMALL-SIGNAL MODEL PARAMETERS

I_{ds}/mm	g_m/mm	g_{ds}/mm	C_{gs}/mm	C_{gd}/mm	C_{ds}/mm	C_{sb}/mm
200 mA	530 mS	62.5 mS	940 fF	90 fF	72.6 fF	82.5 fF

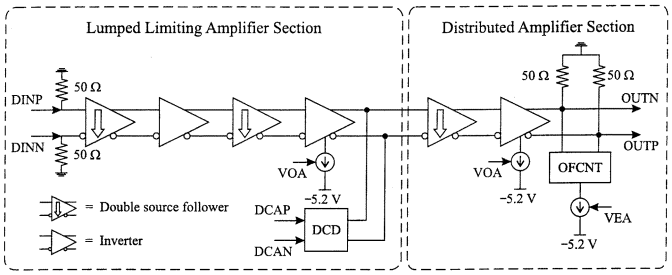

Fig. 5. Block diagram of the 40-Gb/s EA modulator driver illustrating the lumped and distributed sections.

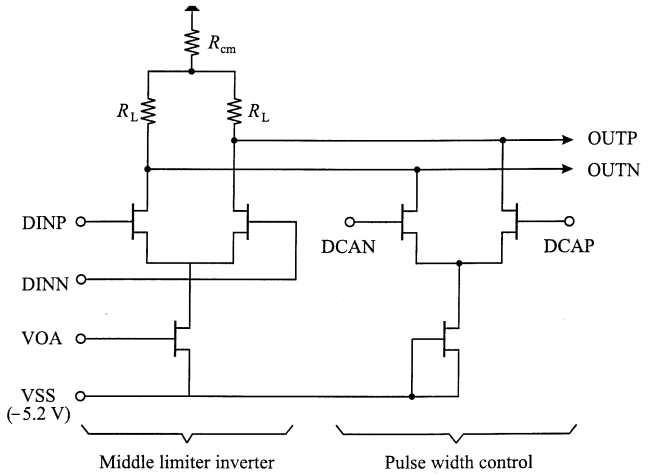

Fig. 6. Middle-stage inverter showing pulsewidth and output amplitude control function implementation.

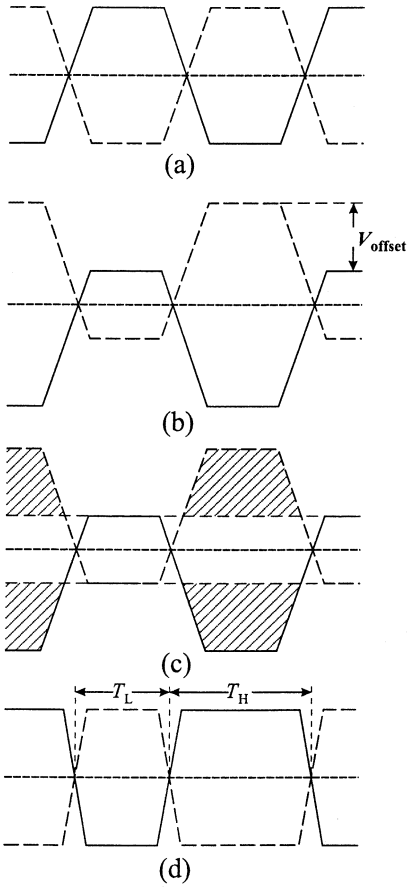

Fig. 7. Pulsewidth control function signal flow. (a) Signal at the input of the middle limiter inverter. (b) Signal at the output of the middle limiter inverter after applying a dc offset through the DCAP and DCAN control inputs. (c) Illustration of the amplitude limiting function of the next stage. (d) Resulting signal with modified pulsewidth at the output of the next limiting stage.

limited to 1.4 V_{pp} per side by the middle stage. The distributed amplifier has an overall gain of approximately 7 dB per side and limits the output swing to a maximum of 3 V_{pp} per side.

B. Middle-Stage Amplifier Block

The schematic for the middle-stage amplifier block is shown in Fig. 6. To avoid any reflections with the DA, the load resistors R_L are matched to the characteristic impedance of the DA's input transmission lines, which is greater than 50 Ω. The common-mode resistor R_{cm} is used to set the dc input level for the DA. The block also includes the elements required for varying the output amplitude and pulsewidth. The former is achieved by adjusting the level supplied to the gate of the inverter current source via the VOA input. The pulsewidth control feature is implemented using a second differential pair connected in parallel with the middle-stage inverter. By default, the DCAP and DCAN pads are biased at the same level and cause the differential pair to sink equivalent amounts of current. As shown in Fig. 7(a) and (b), unbalancing them will introduce a dc offset V_{offset} between the middle-stage output signals. If the two signals are then hard-limited, the effect is to lengthen the high pulse in relation to the low pulse (or vice versa), as illustrated in Fig. 7(c) and (d). The dc offset and pulsewidth variation Δt can be expressed as

$$V_{\text{offset}} = \Delta I_{\text{pwc}} R_L \tag{1}$$

$$\Delta t = \frac{V_{\text{offset}}}{2\text{SL}} \tag{2}$$

where ΔI_{pwc} is the difference in the currents sunk by the two branches of the second differential pair and SL is the slope of the rising and falling edges of the signal pulse. This pulsewidth control scheme only works if the rise and fall times are commensurate with the pulse half period and if it is applied between two limiting circuits, which in this case are the middle-stage and the DA.

C. Distributed Amplifier Block

Although the 0.1–0.2 μm gate-length GaAs pHEMT has a gate-to-drain breakdown voltage of approximately −6 V, its f_T

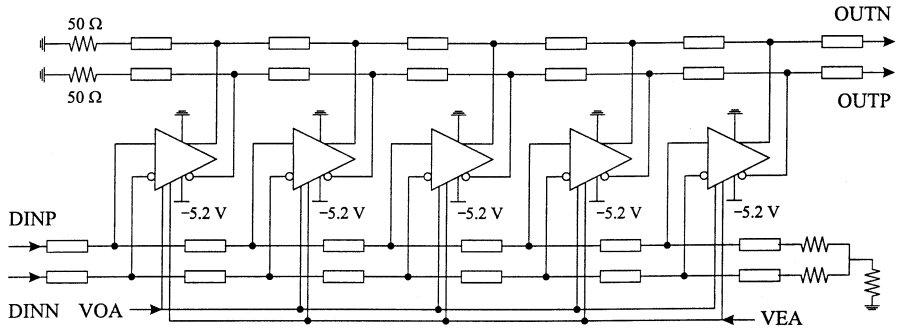

Fig. 8. Block diagram of the distributed amplifier section.

of 100–110 GHz and maximum available gain (MAG) of 15 dB at 50 GHz make it, at best, a marginal device for 40-Gb/s applications. For a dc-coupled circuit matched to 50 Ω and having an output swing of 3 V_{pp} per side, the required modulation current is $I_T = 120\ \mathrm{mA_{pp}}$. Although it is possible to achieve this specification using a lumped output stage at 10 Gb/s [7], a simple analytical derivation indicates that this is not so at 40 Gb/s. Based on the model parameters from Table I, the size of the transistor (W_T) required to switch 120 $\mathrm{mA_{pp}}$ into the on- and off-chip 50-Ω loads is

$$W_T = \frac{I_T}{2I_{ds}/\mathrm{mm}} = 450\ \mu\mathrm{m}. \tag{3}$$

Summing the transistor's parasitic capacitances C_{ds} and C_{db}, the on-chip 50-Ω load resistor's capacitance C_{rb}, the interconnect capacitance C_W, and the pad capacitance C_{pad} gives a total output load capacitance C_L of

$$C_L = C_{ds} + C_{db} + C_{rb} + C_W + C_{pad} \approx 270\ \mathrm{fF} \tag{4}$$

and a 3-dB bandwidth of

$$f_{3dB} = \frac{1}{\pi R_L C_L} = 23\ \mathrm{GHz}. \tag{5}$$

It should be noted that this output pole does not include the added capacitance required to implement the dc output offset control function.

One solution to this problem is to use a distributed amplifier configuration. Not only will this mitigate the size-versus-speed constraint, but it also has the added benefit of excellent output return loss. To extend the bandwidth further still, the distributed amplifier block is designed to operate in a limiting mode. This allows the driver to accommodate data rates significantly beyond that predicted by its small-signal bandwidth. Such an approach has proved successful for 10-Gb/s drivers [8].

The block diagram of the five-stage differential distributed limiting amplifier is shown in Fig. 8, and the adjustable output amplitude and dc offset control elements of each stage are shown in Fig. 9. By distributing the elements of the latter control feature in each stage of the DA and by implementing it with high-impedance cascoded transistors, the parasitic capacitance introduced is both minimized and absorbed into the artificial output transmission lines. The output level is directly affected by the amount of current that the control transistors draw through the DA loads and can be varied by changing the level applied to the VEA pad. The adjustable output amplitude

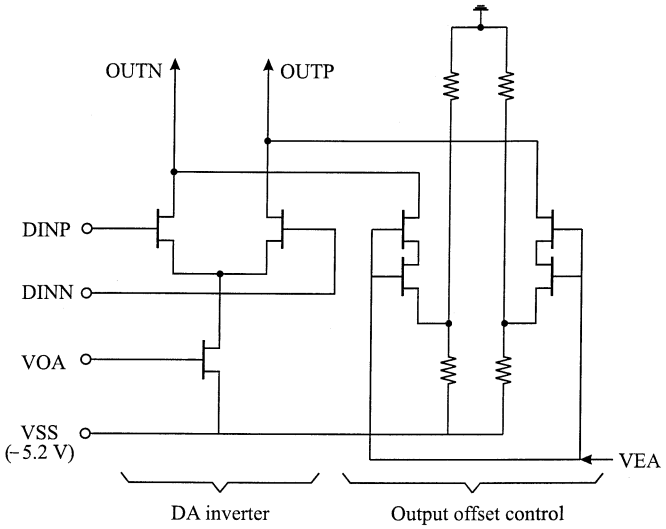

Fig. 9. Distributed amplifier inverting stage showing the output offset and amplitude control function implementations.

is controlled from the VOA pad and operates on the same principle as, and in conjunction with, the middle-stage amplitude control feature. Both techniques have been applied previously for 10-Gb/s EA modulator drivers [9].

D. Choice of Gain-Stage Topology

Industry practice has demonstrated that if the (bipolar) transistor cutoff frequency is at least four times higher than the bit rate, it is possible to achieve adequate bandwidth and input impedance with a chain of basic gain blocks consisting of a single source/emitter follower and an inverter stage (SSF-INV). By appropriately scaling the size of the transistor and tail current in each gain block from the output to the input of the amplifier, the required output swing and bit rate can be obtained with the minimum possible power dissipation. In cases where the f_T of the process is considerably less than four times the bit rate or where parasitic capacitance to ground is expected to be a major concern, additional source/emitter-follower buffering must be introduced in order to provide adequate compensation.

Depletion-mode pHEMTs, such as the ones used in the present design, further complicate the problem because they require level-shifting diodes to provide headroom for the large signal swings at the inverter outputs. In order to lessen their impact on the bandwidth of the gain block, high-frequency bypass capacitors must be included in parallel. Since both they

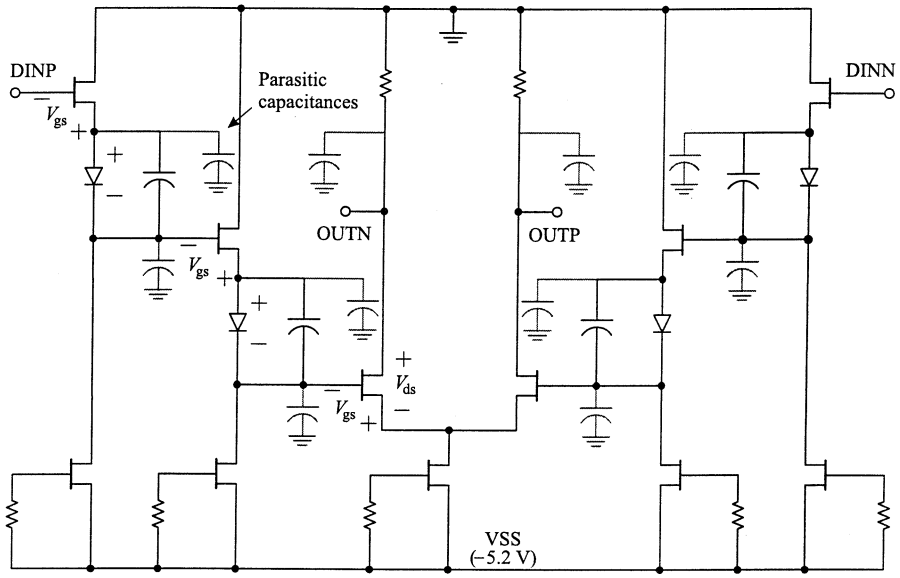

Fig. 10. Basic DSF-INV gain block with ac-bypassed level-shifting diodes. The parasitic capacitances to ground arising from the transistor terminals, level-shifting diodes, and bypass capacitors are illustrated.

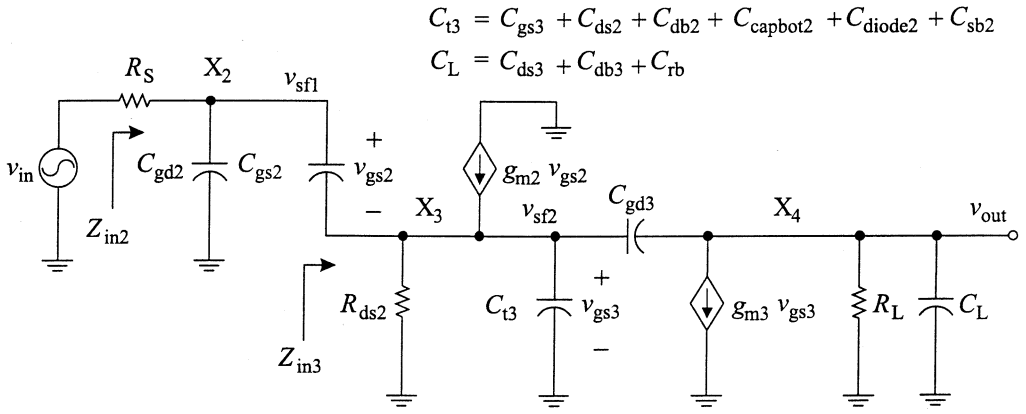

Fig. 11. Small-signal equivalent circuit used in the analytical derivation of the frequency response of a SSF-INV stage.

and the diodes introduce parasitic capacitance to ground, their relative sizes and distribution between source follower stages must be carefully considered if there is to be any bandwidth improvement from adding extra buffering. When the circuit is implemented on a very thin 28-μm-thick GaAs substrate, such as in the present design, the parasitics are such that a double source-follower inverter (DSF-INV) topology becomes mandatory. This arrangement is shown in Fig. 10 along with the associated diode and capacitance elements.

An analytical derivation of the frequency response of both the SSF-INV and DSF-INV gain blocks is presented in the Appendix. It demonstrates that, with the available pHEMT technology, the DSF-INV topology is optimal for meeting the output swing and bit-rate target with the minimum possible power dissipation. It should also be noted that a faster cascode inverter implementation is not feasible given the supply voltage of -5.2 V and the 3-V_{pp} output swing requirement.

The transfer function of the SSF-INV is obtained by analyzing the equivalent circuit shown in Fig. 11. It includes all those components that have a significant effect on the bandwidth of the overall response, namely, the transistors' gate-to-source, gate-to-drain, source-to-bulk, and drain-to-bulk capacitance (C_{gs}, C_{gd}, C_{sb}, and C_{db}, respectively), the final load capacitance C_L, the finite impedance of the tail transistors (R_{ds} and C_{ds}/C_{db}), and all of the bulk capacitance arising from the diodes C_{diode} and bypass capacitors used to shunt them C_{capbot}. To simplify the notation, all of the capacitances at the source follower outputs are summed and represented as a total value C_{tn}. The exact value of the total capacitance is dependent on several factors, namely, the number of level-shifting diodes, the size of the bypass capacitor, and the size of the three transistors that are connected to the common node. It should also be noted that the path through the diodes is considered an ideal short-circuit at high frequency, hence, there is no associated series resistance or capacitance. This assumption is valid because the bypass capacitors are large, being in the range of 2–4 pF.

In lieu of exact expressions for the poles and zeros, which are overly complex and largely uninsightful, Figs. 12 and 13 and Table II are provided to explain the operation of the circuit. Fig. 12 illustrates how the bandwidth varies as a function of the inverter to source-follower gate-width scaling, which is denoted by the parameter $p = W_3/W_2$. Clearly, the optimum bandwidth

TABLE II
POLES AND ZEROS FOR THE SSF-INV WITH SOURCE-FOLLOWER SCALING

Stage	*p=0.75*		*p=1*		*p=2*		*p=3*	
	poles (GHz)	zeros (GHz)	poles (GHz)	zeros (GHz)	poles (GHz)	zeros (GHz)	poles (GHz)	zeros (GHz)
Inverter	$\|p_1\|$ =65.2	$\|z_1\|$ =937	$\|p_1\|$ =65.2	$\|z_1\|$ =937	$\|p_1\|$ =65.2	$\|z_1\|$ =937	$\|p_1\|$ =65.2	$\|z_1\|$ =937
2nd SF	$\|p_2\|$ =72.5	$\|z_2\|$ =89.7	$\|p_2\|$ =73.4	$\|z_2\|$ =89.7	$\|p_2\|$ =75.1	$\|z_2\|$ =89.7	$\|p_2\|$ =75.8	$\|z_2\|$ =89.7
	$\|p_3\|$ =31.5	$\|z_3\|$ =65.2	$\|p_3\|$ =28.3	$\|z_3\|$ =65.2	$\|p_3\|$ =20.3	$\|z_3\|$ =65.2	$\|p_3\|$ =15.9	$\|z_3\|$ =65.2
IP VD	$\|p_4\|$ =71.5	$\|z_4\|$ =72.5	$\|p_4\|$ =72.4	$\|z_4\|$ =73.4	$\|p_4\|$ =74.3	$\|z_4\|$ =75.1	$\|p_4\|$ =75.1	$\|z_4\|$ =75.8
	$\|p_5\|$ =19.2	$\|z_5\|$ =31.5	$\|p_5\|$ =20.6	$\|z_5\|$ =28.3	$\|p_5\|$ =23.5	$\|z_5\|$ =20.3	$\|p_5\|$ =24.7	$\|z_5\|$ =15.9
	$\|p_6\|$ =19.2		$\|p_6\|$ =20.6		$\|p_6\|$ =23.5		$\|p_6\|$ =24.7	

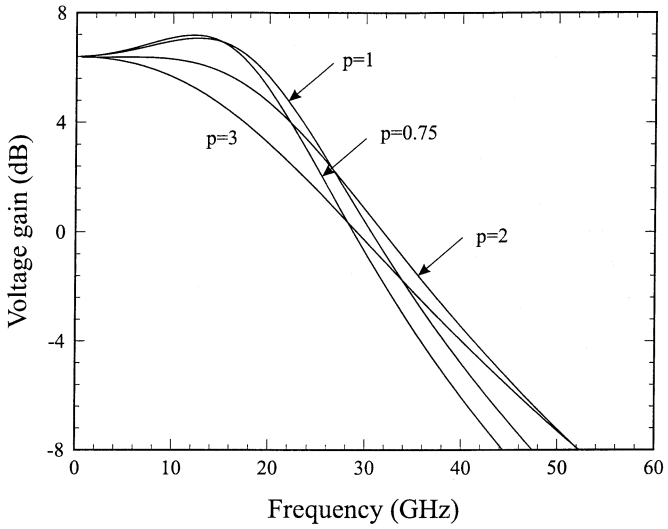

Fig. 12. Voltage gain of the SSF-INV stage as a function of frequency and of the scaling ratio p between the size of the transistors in the inverter and the source follower.

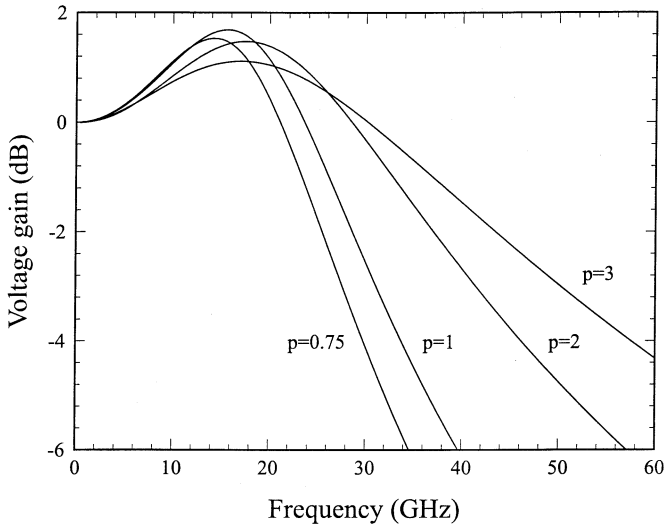

Fig. 13. Transfer function of the input voltage divider formed by the signal source impedance and the input impedance of the SSF-INV stage as a function of the scaling ratio p between the size of the transistors in the inverter and the source follower.

occurs for values of p approaching 1. The inverter in the present example is based on the middle-stage amplifier and is scaled such that it can deliver 1.4 V into a load slightly greater than 50 Ω. Based on the transistor characteristics given in Table I, the value of $C_{\rm L}$ is 65 fF and $C_{\rm t3}$ varies between 185 and 320 fF over the full range of p. This latter variation reflects the fact that the tail transistors, diodes, and bypass capacitors are all assumed to scale with their respective source-follower transistor.

Fig. 13 shows the transfer characteristic of the input voltage divider formed between R_S and $Z_{\rm in2}$. Owing to the negative real component of the source follower's input impedance, the gain profile of this portion of the circuit exhibits a considerable amount of peaking. Table II presents the complete set of poles and zeros for each of the four values of p plotted in Fig. 13. Close inspection of the table reveals that z_1, z_2, and p_2 are all too high to be significant, and that $p_1 = z_3$, $p_2 = z_4$, $p_3 = z_5$ and, consequently, cancel. Thus, the overall response of the SSF-INV is defined almost entirely by the poles p_5 and p_6. Since p_5 and p_6 form a complex pair, the overall bandwidth of the SSF-INV is dependent not only on their magnitude, but on their associated damping coefficient ζ as well. In spite of the bandwidth extension afforded by the SSF-INV, it is clear from Fig. 12 that, irrespective of the scaling coefficient p, it is not possible to achieve sufficient bandwidth for 40 Gb/s using this technology and this configuration.

The solution is to switch to a DSF-INV topology, which is represented by the equivalent model in Fig. 14 and analyzed in the Appendix. Like the SSF-INV, many of the poles and zeros in the transfer function either cancel each other or are nonsignificant. The resulting approximation, which is very nearly exact, consists of only the complex poles p_8 and p_9 and the real pole p_{10}.

To illustrate the effect of gate-width scaling, Figs. 15 and 16 are presented along with their associated poles and zeros in Tables III and IV. In the first instance, Fig. 15 and Table III illustrate the response when the second source follower has the same geometry $(p = 1)$ as the inverter and the first source follower is scaled by an amount $k = W_2/W_1$. From Fig. 15, the widest bandwidth of 41 GHz is achieved for $k = 2$. The degradation both above and below this value can be explained in terms of the three critical poles identified previously. Referring to Table III, p_8 and p_9 increase as k is decreased, which means that the peak introduced by the negative real component of the source fol-

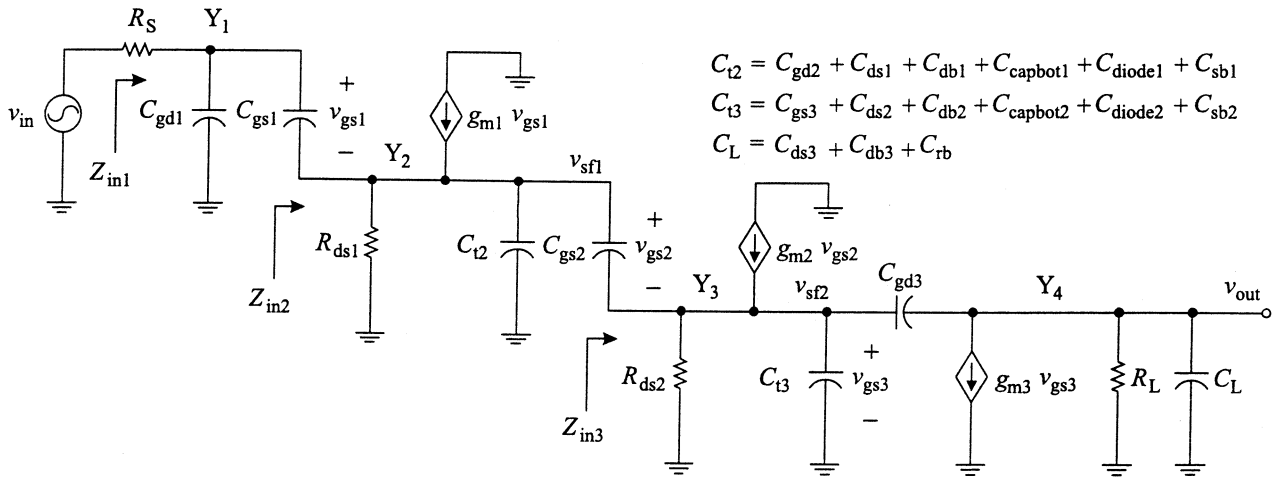

Fig. 14. Small-signal equivalent circuit used in the analytical derivation of the frequency response of a DSF-INV stage.

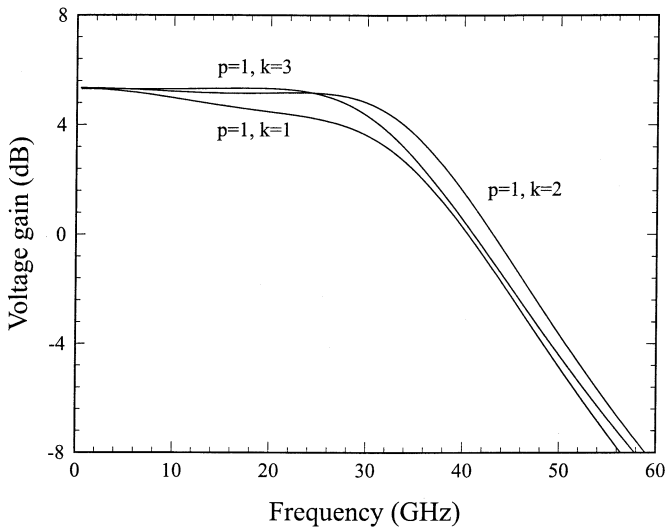

Fig. 15. Voltage gain of the DSF-INV stage as a function of frequency and of the scaling ratio k between the size of the transistors in the second and first source-follower stages. The scaling ratio p between the size of the transistors in the inverter and in the second source follower remains constant.

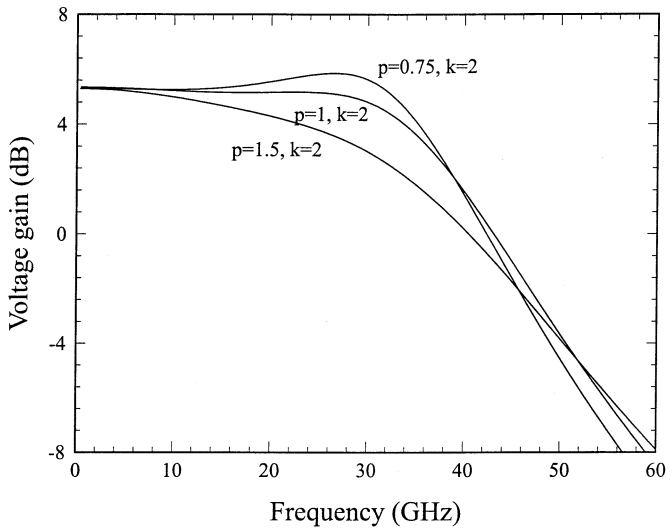

Fig. 16. Voltage gain of the DSF-INV stage as a function of frequency and of the scaling ratio p between the size of the transistors in the inverter and in the second source follower. The scaling ratio k between the size of the transistors in the second and first source follower stages remains constant.

lower's input impedance moves up in frequency. At the same time, the real pole p_{10} decreases. Since p_8 and p_9 increase more slowly than p_{10} decreases with k, there is an optimum point at which the bandwidth is maximized.

The effect of varying the source-follower geometries jointly with respect to the inverter is presented in Fig. 16 and Table IV. In this case, $p = W_3/W_2$, $k = 2$, and the optimal small-signal performance is achieved for $p = 1$ and $k = 2$. The explanation, in terms of the poles and zeros of Table IV, is much the same as above. The reason that the transmission response is more sensitive to variations in p compared to k is because the level-shifting diodes have been deployed entirely at the output of the second source follower. Consequently, any variation in p will affect their size and thus the amount of parasitic capacitance that is introduced. Although not immediately obvious, it turns out that this approach has a significant advantage over distributing the diodes between the outputs of both the first and second stages. By minimizing the total capacitance at the output of the first source follower stage, the critical poles of the circuit, p_8 and p_9, are maximized for only a modest reduction in p_{10}. In other words, the additional source follower increases the impedance seen by the preceding inverter, reduces its capacitive loading and, therefore, regains most of the bandwidth that is lost due to the diodes and bypass capacitors.

As a final remark, small-signal bandwidth is an important figure of merit upon which to base broadband amplifier design, even if it cannot be directly applied to a limiting architecture. By carefully maximizing it while minimizing dc supply current, the amplifier is guaranteed to have good overall large-signal performance.

IV. Fabrication

The die, shown in Fig. 17, has dimensions of 1.95×3.99 mm^2 and was fabricated by Fujitsu Quantum Devices, Ltd., using a 0.15-μm AlGaAs–InGaAs pHEMT process. The substrate height is 28 μm, and with an additional 32 μm of backside metal, the IC has a total thickness of 60 μm.

TABLE III
POLES AND ZEROS FOR THE DSF-INV WITH SOURCE FOLLOWER SCALING ONLY

Stage	*p=1, k=1*		*p=1, k=2*		*p=1, k=3*	
	poles (GHz)	zeros (GHz)	poles (GHz)	zeros (GHz)	poles (GHz)	zeros (GHz)
Inverter	$\|p_1\|$ =65.2	$\|z_1\|$ =937	$\|p_1\|$ =65.2	$\|z_1\|$ =937	$\|p_1\|$ =65.2	$\|z_1\|$ =937
2nd SF	$\|p_2\|$ =73.4	$\|z_2\|$ =89.7	$\|p_2\|$ =73.4	$\|z_2\|$ =89.7	$\|p_2\|$ =73.4	$\|z_2\|$ =89.7
	$\|p_3\|$ =28.3	$\|z_3\|$ =65.2	$\|p_3\|$ =28.3	$\|z_3\|$ =65.2	$\|p_3\|$ =28.3	$\|z_3\|$ =65.2
1st SF	$\|p_4\|$ =72.3	$\|z_4\|$ =89.7	$\|p_4\|$ =72.4	$\|z_4\|$ =89.7	$\|p_4\|$ =72.5	$\|z_4\|$ =89.7
	$\|p_5\|$ =38.7	$\|z_5\|$ =73.4	$\|p_5\|$ =32.6	$\|z_5\|$ =73.4	$\|p_5\|$ =28.8	$\|z_5\|$ =73.4
	$\|p_6\|$ =38.7	$\|z_6\|$ =28.3	$\|p_6\|$ =32.6	$\|z_6\|$ =28.3	$\|p_6\|$ =28.8	$\|z_6\|$ =28.3
IP VD	$\|p_7\|$ =72.5	$\|z_7\|$ =72.3	$\|p_7\|$ =72.6	$\|z_7\|$ =72.4	$\|p_7\|$ =72.6	$\|z_7\|$ =72.5
	$\|p_8\|$ =36.5	$\|z_8\|$ =38.7	$\|p_8\|$ =36.3	$\|z_8\|$ =32.6	$\|p_8\|$ =34.4	$\|z_8\|$ =28.8
	$\|p_9\|$ =36.5	$\|z_9\|$ =38.7	$\|p_9\|$ =36.3	$\|z_9\|$ =32.6	$\|p_9\|$ =34.4	$\|z_9\|$ =28.8
	$\|p_{10}\|$ =22.3		$\|p_{10}\|$ =25.7		$\|p_{10}\|$ =29.9	

TABLE IV
POLES AND ZEROS FOR THE DSF-INV WITH SOURCE-FOLLOWER–INVERTER SCALING

Stage	*p=0.75, k=2*		*p=1, k=2*		*p=1.5, k=2*	
	poles (GHz)	zeros (GHz)	poles (GHz)	zeros (GHz)	poles (GHz)	zeros (GHz)
Inverter	$\|p_1\|$ =65.2	$\|z_1\|$ =937	$\|p_1\|$ =65.2	$\|z_1\|$ =937	$\|p_1\|$ =65.2	$\|z_1\|$ =937
2nd SF	$\|p_2\|$ =72.4	$\|z_2\|$ =89.7	$\|p_2\|$ =73.4	$\|z_2\|$ =89.7	$\|p_2\|$ =73.4	$\|z_2\|$ =89.7
	$\|p_3\|$ =30.6	$\|z_3\|$ =65.2	$\|p_3\|$ =28.3	$\|z_3\|$ =65.2	$\|p_3\|$ =28.3	$\|z_3\|$ =65.2
1st SF	$\|p_4\|$ =71.4	$\|z_4\|$ =89.7	$\|p_4\|$ =72.4	$\|z_4\|$ =89.7	$\|p_4\|$ =73.9	$\|z_4\|$ =89.7
	$\|p_5\|$ =33.8	$\|z_5\|$ =72.4	$\|p_5\|$ =32.6	$\|z_5\|$ =73.4	$\|p_5\|$ =30.9	$\|z_5\|$ =74.7
	$\|p_6\|$ =33.8	$\|z_6\|$ =30.6	$\|p_6\|$ =32.6	$\|z_6\|$ =28.3	$\|p_6\|$ =30.9	$\|z_6\|$ =24.9
IP VD	$\|p_7\|$ =71.5	$\|z_7\|$ =71.4	$\|p_7\|$ =72.6	$\|z_7\|$ =72.4	$\|p_7\|$ =74.0	$\|z_7\|$ =73.9
	$\|p_8\|$ =33.6	$\|z_8\|$ =33.8	$\|p_8\|$ =36.3	$\|z_8\|$ =32.6	$\|p_8\|$ =40.7	$\|z_8\|$ =30.9
	$\|p_9\|$ =33.6	$\|z_9\|$ =33.8	$\|p_9\|$ =36.3	$\|z_9\|$ =32.6	$\|p_9\|$ =40.7	$\|z_9\|$ =30.9
	$\|p_{10}\|$ =24.5		$\|p_{10}\|$ =25.7		$\|p_{10}\|$ =27.1	

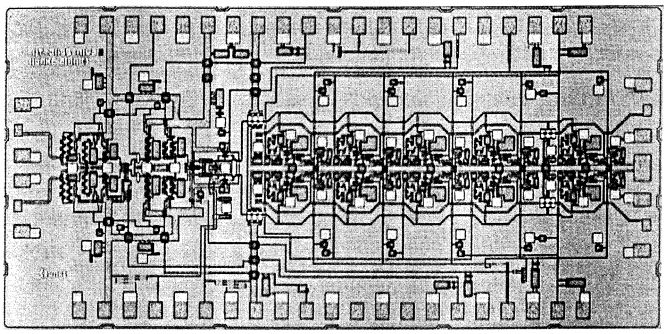

Fig. 17. Microphotograph of the EA modulator driver IC.

The process features one metal layer, an underpass layer, through-wafer vias, interdigital pHEMTs and Schottky diodes, epitaxial resistors, and MIM capacitors. The circuit itself has 240 transistors and includes on-chip bias decoupling filters.

V. MEASUREMENT RESULTS

The driver circuit was measured as a bare die using an Anritsu MP1801A 43.5-Gb/s multiplexer (MUX) and an Agilent 86 100A oscilloscope with 83 484A 50-GHz sampling heads. High-speed interconnections to and from the die were made via 65-GHz GGB wedge probes and 12–in 2.4–mm cables. In order to assess the characteristics of the test setup, preliminary measurements were performed on it without the device under test (DUT) connected. From the eye diagram shown in Fig. 18, the total jitter arising from the measurement resolution of the scope (1 $\mathrm{ps_{rms}}$), the dispersion of the high-speed interconnect and the MUX's clock jitter sum to 6.7 $\mathrm{ps_{pp}}$. The 12-ps 20%–80% rise/fall time that is also evident is partly due to the MUX output, but based on the S-parameters of the setup on its own, it is also as a result of the 16-GHz measurement bandwidth.

The driver consumes 2.8 W and exhibits an overall small-signal gain of 16 dB per side when it is dc coupled to an EA modulator and external load. Fig. 19 shows that the measured and simulated single-ended input and output return loss are in excellent agreement and that they are both better than 10 dB from 0 to 50 GHz. Although not shown, the die exhibits 60-dB isolation up to 35 GHz, and when tested with mismatched loads, offers no evidence of instability. Simulations also suggest a differential output return loss of 15 dB up to 50 GHz. Figs. 20 and 21 present the measured 40- and 44-Gb/s eye diagrams for a

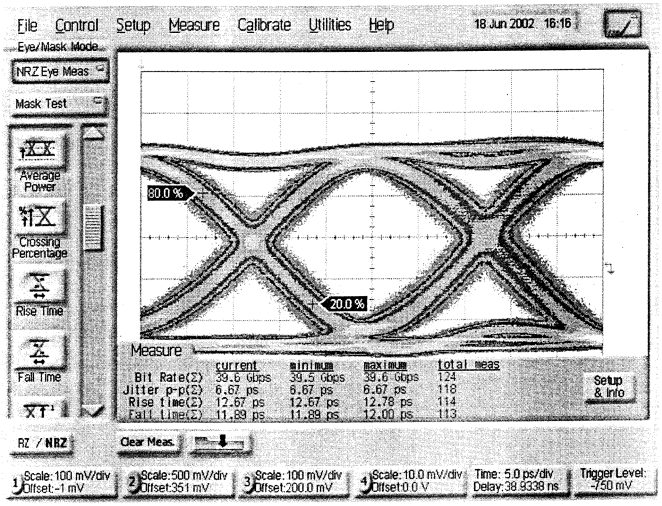

Fig. 18. Measured 40-Gb/s eye diagram with a $2^{31}-1$ pattern for the test setup without DUT.

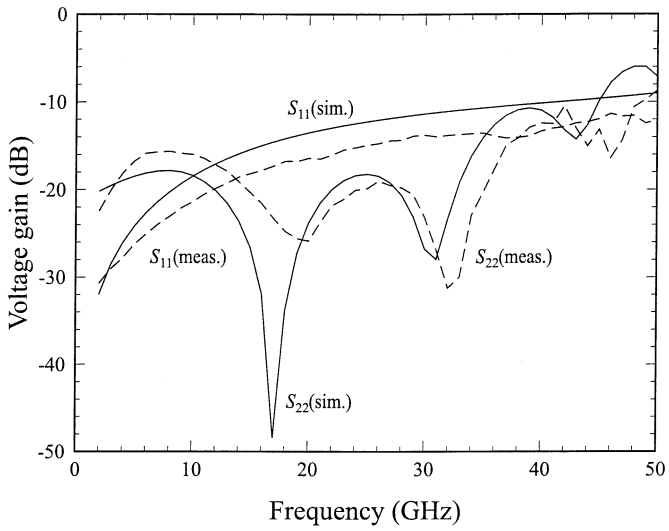

Fig. 19. Measured versus simulated input and output return loss at 18 °C.

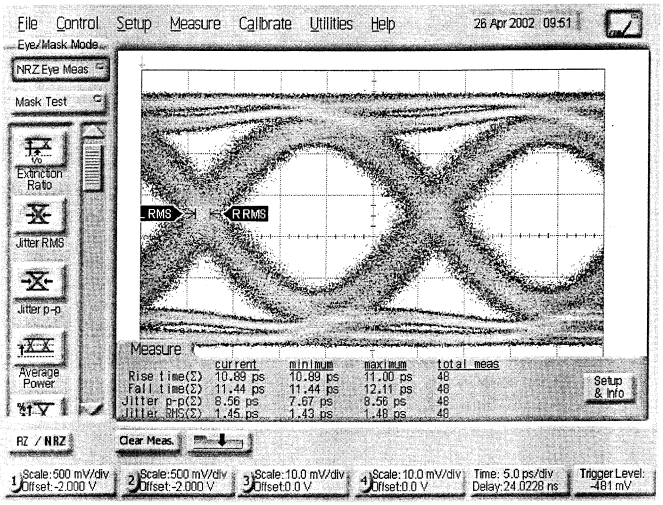

Fig. 20. Measured 40-Gb/s eye diagram with a $2^{31}-1$ pattern showing the maximum 3 V_{pp} output swing per side.

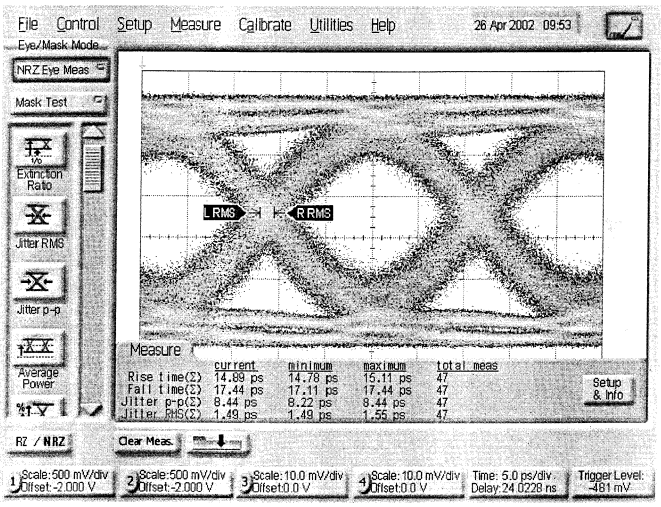

Fig. 21. Measured 44-Gb/s eye diagram with a $2^{31}-1$ pattern showing 3 V_{pp} output swing per side.

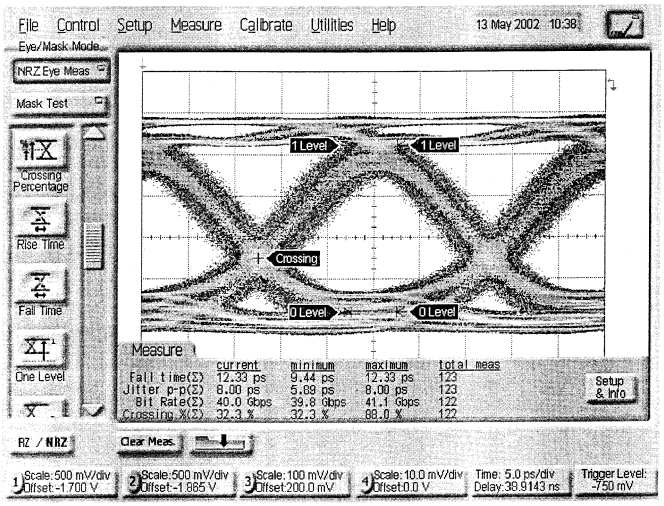

Fig. 22. Measured 40-Gb/s eye diagram with a $2^{31}-1$ pattern showing the eye crossing at 30% (pulsewidth control).

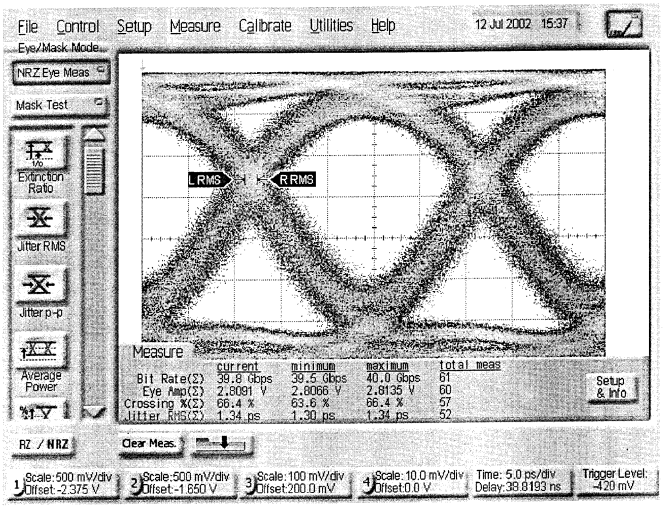

Fig. 23. Measured 40-Gb/s eye diagram with a $2^{31}-1$ pattern showing the eye crossing at 66% (pulsewidth control).

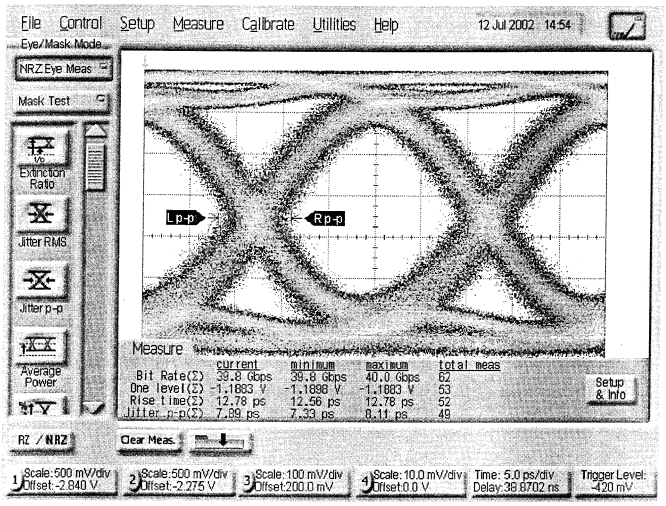

Fig. 24. Measured 40-Gb/s eye diagram with a $2^{31}-1$ pattern showing the maximum output dc offset level of -1.1 V.

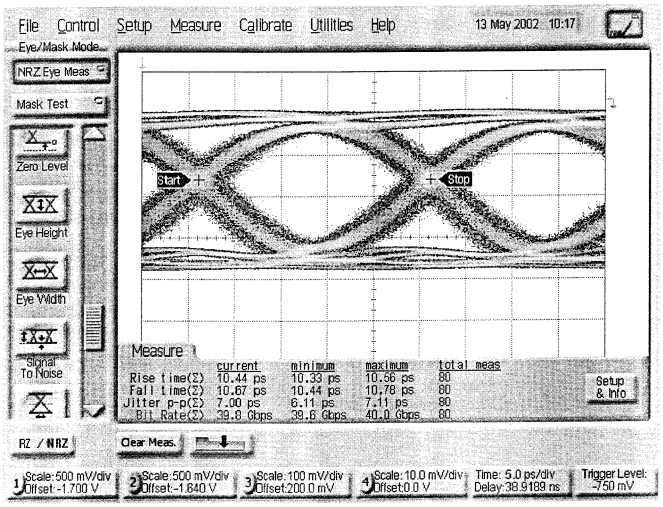

Fig. 25. Measured 40-Gb/s eye diagram with a $2^{31}-1$ pattern showing the minimum 1.7 V_{pp} output swing per side.

$2^{31}-1$ PRBS pattern. In both cases, the output swing is 3.0 V_{pp} per side for a differential input signal having 0.7 V_{pp} per side. As noted above, much of the jitter present can be traced to the clock signal that is used to synchronize the oscilloscope and the uncompensated dispersion of the high-speed interconnection. The eye closure is partly the result of the limited measurement bandwidth. Since only the output cable and probe heads matter in this regard, it will be somewhat better than the 16 GHz stated previously.

Figs. 22–25 demonstrate the EA driver control functions in operation for a differential input signal having a $2^{31}-1$ bit pattern and 0.7 V_{pp} per side. From Figs. 22 and 23, the duty-cycle control function is shown to vary between 30% and 66%. The maximum dc offset, which is defined as the level of a logic "1" output, is shown in Fig. 24 to be -1.1 V. This contrasts with all previous eye diagram plots, which have the minimum offset of -0.15 V. As an illustration of the output swing control, Fig. 25 depicts the measured eye diagram in the case of the minimum output swing of 1.7 V_{pp}. In both of the preceding instances, the control values can be varied smoothly between their two extremes.

VI. Conclusion

A differential distributed limiting EA modulator driver IC using 0.15-μm GaAs pHEMTs has been designed and fabricated for optical transmission systems operating at data rates in the 39.8–42.8-Gb/s range. The IC achieves 3 V_{pp} per side and features output swing control, dc offset control, and pulsewidth control. Both the circuit topology and design are based on a comprehensive analytical derivation of the frequency response of SSF-INV and DSF-INV gain blocks. The final implementation at both the gain block and die level is further optimized by means of a fully scalable nonlinear device model. Although GaAs pHEMT technology is emphasized in this paper, the principles and equations presented here can be applied to the design of many other high-speed digital circuits and logic topologies, including HBT and MOSFET common-mode logic.

Appendix
Derivation of the SSF-INV and DSF-INV Frequency Response

The derivation of the SSF-INV frequency response starts at the output, which in this context is a common-source gain block having zero source resistance (which is assumed to be incorporated into the previous stage). To determine its transfer function, KCL equations are formed at points X_3 and X_4 in Fig. 11 and the results equated to obtain

$$A_{\text{inv}} = -\frac{g_{m3}R_{\text{L}}\left(1 - s\frac{C_{\text{gd3}}}{g_{\text{m3}}}\right)}{1 + sR_{\text{L}}(C_{\text{L}} + C_{\text{gd3}})} \tag{A1}$$

where C_{L} includes the drain-to-bulk C_{db} and drain-to-source C_{ds} capacitance of the inverter transistor, as well as the parasitic capacitance to ground associated with the load resistance C_{rb}. A similar procedure is then followed to derive the input impedance

$$Z_{\text{in3}} = \frac{R_{\text{ds2}}[1 + sR_{\text{L}}(C_{\text{L}} + C_{\text{gd3}})]}{1 + as + bs^2} \tag{A2}$$

and the coefficients in the denominator are given by

$$a = R_{\text{ds2}}(C_{\text{t3}} + C'_{\text{gd3}}) + R_{\text{L}}(C_{\text{L}} + C_{\text{gd3}}) \tag{A3}$$

$$b = R_{\text{ds2}}R_{\text{L}}(C_{\text{t3}} + C_{\text{gd3}})(C_{\text{L}} + C_{\text{gd3}}). \tag{A4}$$

To simply the expressions, all the terms associated with the Miller effect are incorporated into C'_{gd3} as follows:

$$C'_{\text{gd3}} = C_{\text{gd3}}(1 + g_{\text{m3}}R_{\text{L}}). \tag{A5}$$

It should be noted that the Miller approximation is not applied in the calculation of Z_{in3}. Although it does simplify (A2), it overstates the bandwidth and does little to make the subsequent expressions for this multistage amplifier any less complicated.

The determination of the transfer function of the second source follower involves forming the KCL equation at X_3 and equating it to the expression for the voltage drop between X_2

and X_3. From (A2), the load is Z_{in3}, which gives a transfer function of

$$A_{sf2} = \frac{g_{m2} Z_{in3} \left(1 + s\frac{C_{gs2}}{g_{m2}}\right)}{1 + g_{m2} Z_{in3} \left(1 + s\frac{C_{gs2}}{g_{m2}}\right)}. \tag{A6}$$

The complete input impedance for the source follower is now calculated in two steps. In the first instance, the KCL equation at node X_3 is used to determine the equivalent impedance seen looking into the gate of the source follower's transistor. This expression is then combined in parallel with the transistors' gate-to-drain capacitance C_{gd2} to yield

$$Z_{in2} = \frac{1}{sC_{gd2}} \left\| \frac{1 + g_{m2} Z_{in3} \left(1 + s\frac{C_{gs2}}{g_{m2}}\right)}{sC_{gs2}}. \right. \tag{A7}$$

Although it is possible to expand this expression, the result does not provide much insight. Moreover, as the analysis continues toward the overall input of the circuit, the equations only get more complicated.

Having determined the input impedance to the source follower, the input voltage divider has a transfer function of

$$A_{vd} = \frac{Z_{in2}}{R_S + Z_{in2}} \tag{A8}$$

where in the general case, R_S should be replaced with Z_S, the output impedance of the preceding inverter stage.

When all of the terms are combined, the result is a complete SSF-INV transfer function consisting of six poles and five zeros

$$A_v = A_{vd} A_{sf2} A_{inv} = A_0 \frac{\prod_{i=1}^{5} \left(1 - \frac{s}{z_i}\right)}{\prod_{i=1}^{6} \left(1 - \frac{s}{p_i}\right)} \tag{A9}$$

where the dc gain term is given by

$$A_0 = -\frac{g_{m3} R_L}{1 + \frac{1}{g_{m2} R_{ds2}}}. \tag{A10}$$

Up to (A6), the derivation for the DSF-INV is exactly the same as that of the SSF-INV. It diverges at (A7) because the input to the second source follower now includes the tail impedance of the first source follower in addition to the capacitance introduced by any of the level-shifting diodes that may be connected between the first and second stages. Consequently, the input impedance becomes

$$Z_{in2} = R_{ds1} \left\| \frac{1}{sC_{t2}} \right\| \frac{1 + g_{m2} Z_{in3} \left(1 + s\frac{C_{gs2}}{g_{m2}}\right)}{sC_{gs2}}. \tag{A11}$$

Equating the KCL equation at Y_2 in Fig. 14 with the voltage expression from Y_2 to Y_1, the first source-follower transfer function is

$$A_{sf1} = \frac{g_{m1} Z_{in2} \left(1 + s\frac{C_{gs1}}{g_{m1}}\right)}{1 + g_{m1} Z_{in2} \left(1 + s\frac{C_{gs1}}{g_{m1}}\right)}. \tag{A12}$$

In a procedure similar to that followed in the derivation of (A7), the input impedance of the first source follower is given by

$$Z_{in1} = \frac{1}{sC_{gd1}} \left\| \frac{1 + g_{m1} Z_{in2} \left(1 + s\frac{C_{gs1}}{g_{m1}}\right)}{sC_{gs1}} \right. \tag{A13}$$

and permits the determination of the response of the DSF-INV's input voltage divider

$$A_{vd} = \frac{Z_{in1}}{R_S + Z_{in1}}. \tag{A14}$$

Combining all of the individual gain terms, the overall transfer function for the DSF-INV consists of a dc gain term, ten poles, and nine zeros

$$A_v = A_{vd} A_{sf1} A_{sf2} A_{inv} = A_0 \frac{\prod_{i=1}^{9} \left(1 - \frac{s}{z_i}\right)}{\prod_{i=1}^{10} \left(1 - \frac{s}{p_i}\right)} \tag{A15}$$

where the familiar expression for the dc gain has been singled out as

$$A_0 = -\frac{g_{m3} R_L}{\left(1 + \frac{1}{g_{m1} R_{ds1}}\right)\left(1 + \frac{1}{g_{m2} R_{ds2}}\right)}. \tag{A16}$$

When all of the terms in (A9) and (A15) are expanded, it becomes possible to solve the resulting polynomial expressions to arrive at the complete set of poles and zeros presented in Tables II–IV.

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REFERENCES

[1] Y. Baeyens, G. Georgiou, J. Weiner, V. Houtsma, P. Paschke, Q. Lee, A. Leven, R. Kopf, J. Frackoviak, C. Chen, C. T. Liu, and Y. K. Chen, "InP D-HBT ICs for 40 Gb/s and higher bitrate lightwave transceivers," in *IEEE GaAs IC Symp. Dig.*, Baltimore, MD, Oct. 2001, pp. 125–128.

[2] G. Freeman, Y. Kwark, M. Meghelli, S. Zier, A. Rylyakov, M. Sorna, T. Tanji, O. Schreiver, K. Walter, J. Rieh, B. Jagannathan, A. Joseph, and S. Subbanna, "40 Gbit/sec circuits built from a 120 GHz f_T SiGe technology," in *IEEE GaAs IC Symp. Dig.*, Baltimore, MD, Oct. 2001, pp. 89–92.

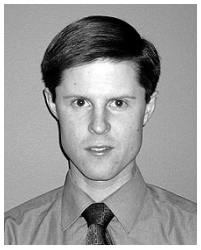
[3] M. Racanelli, K. Schuegraf, A. Kalburge, A. Kar-Roy, B. Shen, C. Hu, D. Chapek, D. Howard, D. Quon, F. Wang, G. U'ren, L. Lao, H. Tu, J. Zheng, J. Zhang, K. Bell, K. Yin, P. Joshi, S. Akhtar, S. Vo, T. Lee, W. Shi, and P. Kempf, "Ultra high speed SiGe NPN for advanced BiCMOS technology," in *IEDM Tech. Dig.*, Washington, DC, Dec. 2001, pp. 336–339.

[4] A. Joseph, D. Coolbaugh, D. Harame, G. Freeman, S. Subbanna, M. Doherty, J. Dunn, C. Dickey, D. Greenberg, R. Groves, M. Meghelli, A. Rylyakov, M. Sorna, O. Schreiber, D. Herman, and T. Tanji, "0.13 μm 210 GHz f_T SiGe HBTs—Expanding the horizons of SiGe BiCMOS," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, San Francisco, CA, Feb. 2002, pp. 180–181.

[5] D. Streit, R. Lai, A. Gutierrez-Aitken, M. Siddiqui, B. Allen, A. Chau, W. Beale, and A. Oki, "InP and GaAs components for 40 GBPS applications," in *IEEE GaAs IC Symp. Dig.*, Baltimore, MD, Oct. 2001, pp. 247–250.

[6] H. Shigematsu, N. Yoshida, M. Sato, N. Hara, T. Hirose, and Y. Watanabe, "45-GHz distributed amplifier with a linear 6-V_{p-p} output for a 40-Gb/s $LiNbO_3$ modulator driver circuit," in *IEEE GaAs IC Symp. Dig.*, Baltimore, MD, Oct. 2001, pp. 137–140.

[7] M. Miyashita, N. Yoshida, Y. Kojima, T. Kitano, N. Higashisaka, J. Nakagawa, T. Takagi, and M. Otsubo, "An AlGaAs/InGaAs pseudomorphic HEMT modulator driver IC with low power dissipation for 10-Gb/s optical transmission systems," *IEEE Trans. Microwave Theory Tech.*, vol. 45, pp. 1058–1064, July 1997.
[8] T. Y. K. Wong, A. P. Freundorfer, B. C. Beggs, and J. E. Sitch, "A 10-Gb/s AlGaAs–GaAs HBT high power fully differential limiting distributed amplifier for III-V Mach–Zehnder modulator," *IEEE J. Solid-State Circuits*, vol. 31, pp. 1388–1393, Oct. 1996.
[9] M. Miyashita, K. Yamamoto, K. Andoh, N. Okada, K. Motoshima, and A. Takemoto, "A 10-Gb/s AlGaAs/InGaAs pHEMT distributed EA driver with a D-flip-flop for optical fiber links," in *IEEE GaAs IC Symp. Dig.*, Seattle, WA, Nov. 2000, pp. 205–208.



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From 1984 to 1991, he worked in research and development and in academia in Bucharest, designing and lecturing on microwave semiconductor devices and microwave integrated circuits. From 1994 to 2000, he was with Nortel Networks, Ottawa, Canada, where he was responsible for projects in high-frequency characterization and statistical scalable compact model development for Si, SiGe, and III-V heterostructure devices. He led the modeling infrastructure development for, and was involved in the prototyping of, wireless and broad-band fiber optics transceivers in emerging semiconductor technologies. In April 2000, he cofounded Quake Technologies, Ottawa, a fabless semiconductor company focusing on the design and fabrication of 10- and 40-Gb/s physical layer ICs. As Chief Technology Officer of Quake, he coordinated the access and characterization of Si, SiGe, GaAs, and InP technologies, high-frequency package design, and electro-optical interface product development. In September 2002, he joined the Department of Electrical and Computer Engineering, University of Toronto, as an Associate Professor. He has authored or coauthored more than 30 refereed and invited technical papers spanning the simulation, modeling, design, and fabrication of GaAs-, InP-, and Si-based heterostructure devices and circuits and holds two U.S. patents in these areas. His research and teaching interests focus on the modeling and characterization of very deep-submicron semiconductor devices and on novel design techniques and low-voltage low-power topologies for wireless, optical fiber, and wireline data communication physical layer ICs in the 10–100-GHz range.

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