A Scalable High-Frequency Noise Model for Bipolar Transistors with Application to Optimal Transistor Sizing for Low-Noise Amplifier Design

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***Abstract*—Fully scalable, analytical HF noise parameter equations for bipolar transistors are presented and experimentally tested on high-speed Si and SiGe technologies. A technique for extracting the complete set of transistor noise parameters from Y parameter measurements only is developed and verified. Finally, the noise equations are coupled with scalable variants of the HICUM and SPICE-Gummel–Poon models and are employed in the design of tuned low noise amplifiers (LNA's) in the 1.9-, 2.4-, and 5.8-GHz bands.**

***Index Terms*—Bipolar transistor, compact modeling, low noise, low-noise amplifier, low-noise transistor design, noise figure, noise matching, noise measurements, radio-frequency integrated circuit design, SiGe heterojunction bipolar transistor.**

I. Introduction

The recent boom in wireless consumer applications has emphasized the requirement for low-cost, highly integrated RF parts. Steady improvement in transistor performance and desire for higher level of integration have led to the increased application of silicon technology. Since substrate and interconnect losses are significantly higher in Si than in GaAs, Si RF circuit design should target the optimization of the size of transistors in order to simplify matching, rather than design the matching circuit around a given transistor. Such an approach requires a physically based, scalable compact model for bipolar transistors [1], as well as accurate, closed-form noise parameter equations, suitable for circuit design.

In the first part, expressions for the four noise parameters of a bipolar transistor are derived. The accuracy of these equations is investigated using SPICE-Gummel–Poon (SGP) modeled and measured transistor noise data. Next, a technique is presented for extracting the complete set of noise parameters from measured Y parameters only. It avoids the inaccuracy of on-wafer noise parameter measurements which is especially severe for small geometry devices or devices biased in the sub-mA range. Finally, scalable variants of the SGP and HICUM models [2], in conjunction with the new noise parameter equations, are applied in the design of tuned low-noise amplifiers (LNA's) in the 2–6 GHz band.

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II. Noise Parameter Equations and Measurements

A. Theoretical Background

Equations (1)–(3) define the noise resistance R_n, optimum source admittance $Y_{\rm sop}$, and minimum noise figure $F_{\rm MIN}$ of a two-port with respect to its noise correlation matrix entries C_{A11}, C_{A12}, and C_{A22} [3]–[4]. The latter, in turn, are expressed in (4)–(6) as functions of the input-referred noise voltage v_n^2 and noise current i_n^2 sources of the two-port, as well as of the Y parameters of the noise-free two-port

$$R_n = C_{A11} \tag{1}$$

$$Y_{\rm sop} = G_{\rm SOP} + jB_{\rm SOP} = \sqrt{\frac{C_{A22}}{C_{A11}} - \left(\frac{{\rm Im}\{C_{A12}\}}{C_{A11}}\right)^2} + j\frac{{\rm Im}\{C_{A12}\}}{C_{A11}} \tag{2}$$

$$F_{\rm MIN} = 1 + 2({\rm Re}\{C_{A12}\} + C_{A11}G_{\rm sop}) \tag{3}$$

$$C_{A11} = \frac{\langle v_n^2\rangle}{4kT\Delta f} = \frac{\langle i_c^2\rangle}{4kT\Delta f|Y_{21}|^2} + (r_E + r_B) \tag{4}$$

$$C_{A21} = C_{A12}^* = \frac{\langle v_n^* i_n\rangle}{4kT\Delta f} = \frac{Y_{11}\cdot\langle i_c^2\rangle}{4kT\Delta f|Y_{21}|^2} \tag{5}$$

$$C_{A22} = \frac{\langle i_n^2\rangle}{4kT\Delta f} = \frac{|Y_{11}|^2\cdot\langle i_c^2\rangle}{4kT\Delta f|Y_{21}|^2} + \frac{\langle i_b^2\rangle}{4kT\Delta f}. \tag{6}$$

Equation (3) is a recast of the original formula in [3]. Fig. 1 illustrates the simplified small-signal and noise equivalent circuit and the two-step approach used in the derivation of the noise parameters in the case of a bipolar transistor. The noise current sources i_B^2, i_C^2 represent the internal shot noise sources of the bipolar transistor. After substituting (4)–(6) into (1)–(3), (7)–(9) are obtained which describe the bipolar transistor noise parameters as functions of the internal shot noise current sources, transistor Y parameters, series emitter resistance r_E, and total base resistance r_B in a manner similar to that employed for GaAs MESFET's [5]. The bias current

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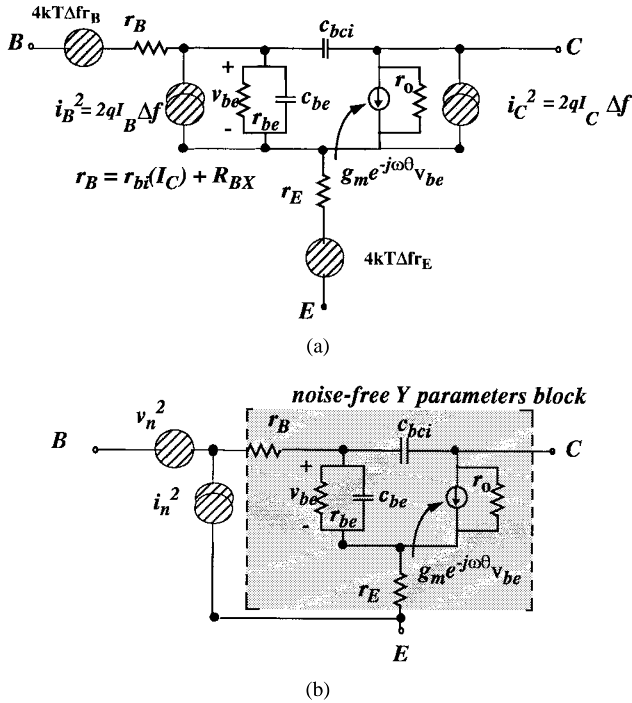

Fig. 1. (a) Small signal and noise equivalent circuit used in the bipolar transistor noise parameter derivation. It features the uncorrelated shot-noise currents i_B^2 and i_C^2. (b) The equivalent input-referred noise model with correlated noise sources i_n^2, v_n^2, and noise-free Y parameters block.

dependence of the noise parameters appears in explicit form via the I_B and I_C terms, and also implicitly in r_B and in the Y parameters. V_T represents the thermal voltage. In the derivation of (7)–(9) it is assumed that the base and collector noise currents are uncorrelated. This is equivalent to neglecting the imaginary part of the transconductance $g_m e^{-j\omega\theta}$, a reasonable simplification up to frequencies approaching $f_T/2$ [6]. θ is the transconductance delay, typically 40–60% of the transit time [7]. Despite this assumption, the input-referred noise sources v_n^2 and i_n^2 remain correlated and are modeled accordingly [see (8) and (9) at the bottom of the page]

$$R_n = \frac{I_C}{2V_T|Y_{21}|^2} + (r_E + r_B). \tag{7}$$

Similarly, Si MOSFET noise parameters can be obtained by making the following substitutions in (7)–(9):

$$\left(\frac{I_C}{2V_T} \rightarrow \frac{2}{3}g_m\right); (I_B \rightarrow 0); (r_E + r_B) \rightarrow (R_S + R_G).$$

For the bias currents and frequency range used in wireless design, the bipolar transistor noise parameter equations can be recast in easy-to-interpret formats (10)–(13). These can be employed to tailor the device size—typically only the emitter length l_E—to achieve optimal low-noise matching at the desired frequency and input impedance. As indicated by (10) and (11), the noise resistance and optimum noise admittance scale as l_E^{-1} and l_E, respectively. Alternatively, the real part of the optimum noise impedance R_{SOP}, given by (12), scales as l_E^{-1} and decreases with increasing frequency, f

$$R_n \cong \frac{n^2 V_T}{2I_C} + (r_E + r_B) \sim l_E^{-1} \tag{10}$$

$$Y_{\mathrm{sop}} \cong \frac{f}{f_T R_n} \times \left\{\sqrt{\frac{I_C}{2V_T}(r_E + r_B)\left(1 + \frac{f_T^2}{\beta_0 f^2}\right) + \frac{n^2 f_T^2}{4\beta_0 f^2}} - j\frac{n}{2}\right\} \sim l_E \tag{11}$$

$$R_{\mathrm{sop}} \cong \frac{R_n f_T}{f} \times \frac{\sqrt{\frac{I_C}{2V_T}(r_E + r_B)\left(1 + \frac{f_T^2}{\beta_0 f^2}\right) + \frac{n^2 f_T^2}{4\beta_0 f^2}}}{\frac{I_C}{2V_T}(r_E + r_B)\left(1 + \frac{f_T^2}{\beta_0 f^2}\right) + \frac{n^2}{4}\left(1 + \frac{f_T^2}{\beta_0 f^2}\right)} = Z_0 \tag{12}$$

where β_0 is the dc current gain. n is the collector current ideality factor, approximately equal to one, except under high current injection bias when its value can exceed 1.2. As long as the length-to-width ratio (l_E/w_E) of the emitter stripe is larger than ten, F_{MIN} remains invariant to changes in emitter length and increases almost linearly with frequency

$$F_{\mathrm{MIN}} \cong 1 + \frac{n}{\beta_0} + \frac{f}{f_T} \times \sqrt{\frac{2I_C}{V_T}(r_E + r_B)\left(1 + \frac{f_T^2}{\beta_0 f^2}\right) + \frac{n^2 f_T^2}{\beta_0 f^2}}. \tag{13}$$

All noise parameters are nonlinear functions of emitter width w_E via the $I_C(r_E + r_B)$ term.

B. Experimental Validation

In order to verify the noise parameter equations, automated noise parameter measurements were carried out in the 2–6 GHz range using an NP5 on-wafer measurement system from ATN Microwave Inc. Devices with variable widths, lengths, and with single- or multi-stripe geometries have been investigated in three technologies: 1) a single-poly BiCMOS

$$Y_{\mathrm{sop}} = \sqrt{\frac{I_B|Y_{21}|^2 + I_C|Y_{11}|^2}{2V_T|Y_{21}|^2(r_E + r_B) + I_C} - \left(\frac{I_C\ \mathrm{Im}\{Y_{11}\}}{2V_T|Y_{21}|^2(r_E + r_B) + I_C}\right)^2} - j\frac{I_C \mathrm{Im}\{Y_{11}\}}{2V_T|Y_{21}|^2(r_E + r_B) + I_C} \tag{8}$$

$$F_{\mathrm{MIN}} = 1 + \frac{I_C}{V_T|Y_{21}|^2}\left(\mathrm{Re}\{Y_{11}\} + \sqrt{\left[1 + \frac{2V_T|Y_{21}|^2(r_E + r_B)}{I_C}\right]\left[|Y_{11}|^2 + \frac{I_B|Y_{21}|^2}{I_C}\right] - (\mathrm{Im}\{Y_{11}\})^2}\right) \tag{9}$$

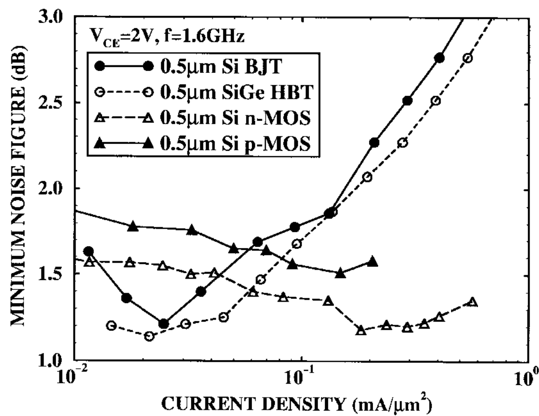

Fig. 2. ATN-NP5, on-wafer measured minimum noise figure as a function of drain/collector current density for state-of-the-art Si MOSFET's, Si BJT's, and SiGe HBT's with 0.5-μm minimum feature size. All measurements were performed at 1.6 GHz. The unit gate finger width of the multifinger MOSFET's is 10 μm. The series and parallel parasitics associated with probing pads were not de-embedded. The drain current density in MOSFET's is obtained as $I_D/(W*L)$.

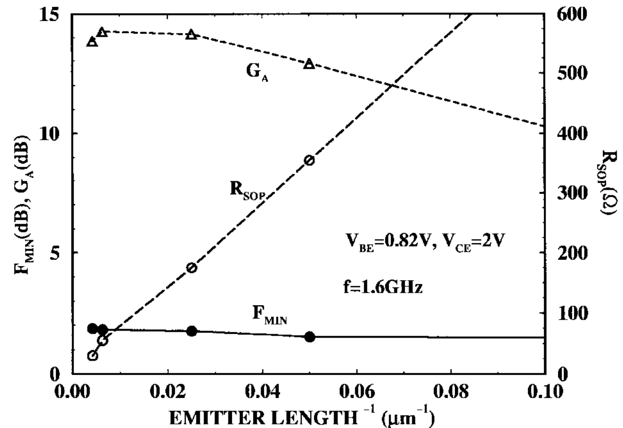

Fig. 3. ATN-NP5 on-wafer measured minimum noise figure $F_{\rm MIN}$, optimum noise resistance $R_{\rm SOP}$, and associated gain G_A, as functions of emitter length for NT25 Si BJT's with 0.5-μm emitter width biased at the minimum noise current density. All measurements were performed at 1.6 GHz. The series and parallel parasitics associated with probing pads were not de-embedded. Their contribution becomes comparable to the series base and emitter resistances of the transistor as the emitter length increases.

npn; 2) NT25, Northern Telecom's self-aligned, double-poly, implanted-base, Si npn, and 3) IBM's self-aligned, double-poly SiGe heterojunction bipolar transistor (HBT) [8]. The peak cutoff frequencies at $V_{\rm CE} = 2$ V are 20, 26, and 45 GHz, respectively, while typical $f_{\rm MAX}$ values are 27, 47, and 65 GHz, respectively. In the case of the first two technologies, which do not feature trench isolation, $f_{\rm MAX}$ is a function of emitter length and decreases for shrinking emitter length-to-width ratios as a result of the lack of scaling in the collector-substrate capacitance.

Fig. 2 presents the measured minimum noise figure at 1.6 GHz as a function of drain/collector current density for 0.5-μm Si MOSFET's, Si bipolar junction transistors (BJT's), and SiGe HBT's. In the case of Si MOSFET's, dominated by thermal noise, minimum noise is achieved at large current densities, corresponding to the peak f_T current density. Despite smaller f_T values (18–20 GHz) [9], n-MOSFET noise is as low as that of SiGe HBT's. However, in MOSFET's minimum noise can only be achieved by compromising low-power consumption. In contrast, because of the interplay between thermal noise (from r_E and r_B), prevailing at low current densities, and shot noise, dominating at high current densities, bipolar transistors show an optimum noise current density ten times smaller than the peak f_T current density. Bipolar transistors have the benefit of concomitant low-noise and low-power operation. This advantage may diminish as MOSFET gate lengths continue to shrink [10]. Figs. 3 and 4 illustrate the measured emitter length and emitter width dependencies of the noise parameters of the NT25 Si BJT's. Both plots follow closely the predictions of the simplified noise parameter equations (10)–(13).

While noise parameters are available from the postprocessor of microwave circuit simulators such as HP-EESOF's LIBRA, only equivalent noise voltages and currents can be modeled directly using SPICE-like simulators. To circumvent this problem, (7)–(9) were included in an HSPICE deck and, in conjunction with the MEASURE statement, were employed

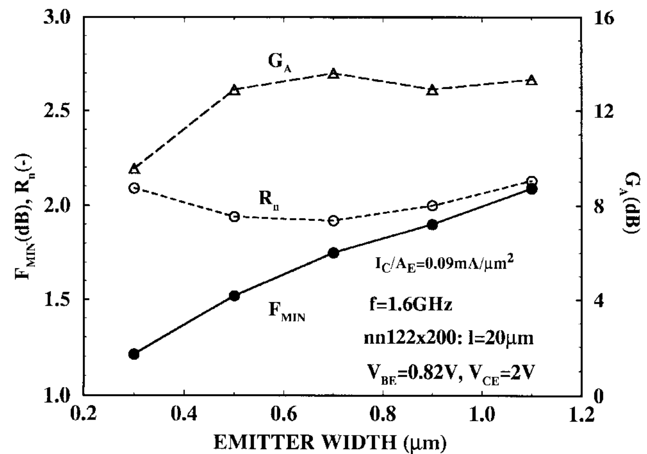

Fig. 4. ATN-NP5 on-wafer measured minimum noise figure $F_{\rm MIN}$, normalized (to 50 Ω) noise resistance R_n, and associated gain G_A, as a functions of emitter width for NT25 Si BJT's with single-stripe 20-μm long emitters, two base, and two collector contacts, biased at the minimum noise current density. The series and parallel parasitics associated with probing pads were not de-embedded. The label nn122x200 represents the standard NT25 npn nomenclature, where the first digit represents the number of emitter stripes (one), the second digit describes the number of base metal contacts (two) and the third digit stands for the number of collector contacts (two). x describes the variable emitter width, whereas 200 stands for the emitter stripe length in tenths of micrometers (i.e., 20 μm in this case).

to simultaneously compute $F_{\rm MIN}, f_T, f_{\rm MAX}, R_n,$ and $Y_{\rm sop}$ as functions of I_C in a single simulation run. The role of the simulator is to provide accurate, nonapproximated Y parameters and $r_B(I_C)$ characteristics. The HSPICE-calculated noise parameters were found to agree within 0.25 dB, up to 10 GHz, with those generated by LIBRA.

Measured and SGP-modeled $F_{\rm MIN}$, associated power gain G_A, f_T, and $f_{\rm MAX}$ are compared in Fig. 5 as functions of the collector current for a 0.65 × 25 μm^2 single-poly bipolar transistor. The agreement is well within the typical on-wafer noise measurement error. The minimum noise current density is almost independent of $V_{\rm CE}$ and emitter length but increases

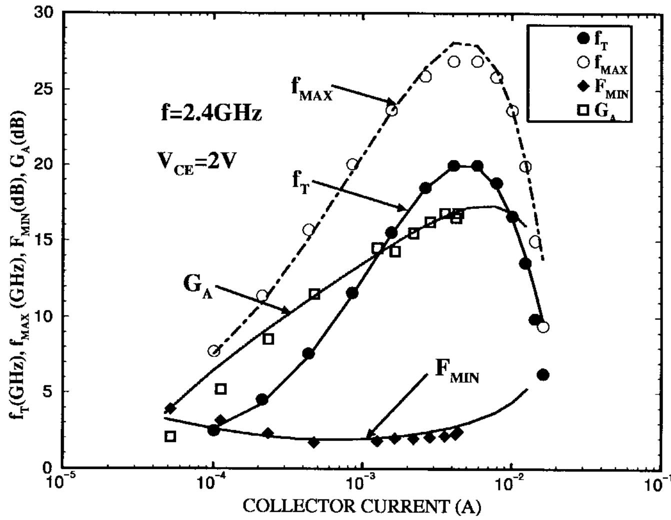

Fig. 5. Measured (symbols) and SGP-modeled (lines) $F_{\rm MIN}$, f_T, $f_{\rm MAX}$, G_A versus I_C characteristics for a 0.65 × 25 μm^2 single-poly BiCMOS npn.

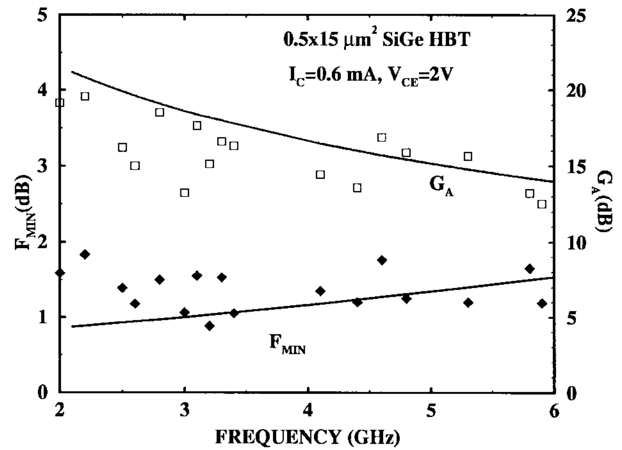

Fig. 6. Measured (symbols) and SGP-modeled (lines) $F_{\rm MIN}, G_A$ versus frequency characteristics for a 0.5 × 15 μm^2 double-poly SiGe HBT at minimum noise bias.

weakly with frequency. It is typically six to ten times smaller than the peak f_T current density. The simulation results were obtained with a set of SGP model parameters extracted from dc and S parameter measurements on the modeled device. No fitting of the noise measurement data was performed, thus confirming the accuracy of (7)–(9).

The measured and modeled frequency dependence of the noise parameters is plotted in Fig. 6 for a 0.5 × 15 μm^2 SiGe HBT biased close to the minimum noise current density J_C. The rate of $F_{\rm MIN}$ degradation with frequency is inversely proportional to f_T, highlighting the requirement for transistors with large cutoff frequencies if low noise operation at high frequency is desired. The scatter in the measured data is due to the fact that the current NP5 system is unable to provide a controlled number of high impedance source states in a specified region of the Smith chart, as required by a small device with typical optimum source reflection coefficients larger than 0.8. In general, noise parameter measurements are not sufficiently accurate to provide a reliable extraction of the base resistance. As described in the next section, this can be more readily achieved from Z parameter measurements.

III. Extraction of Transistor Noise Parameters from Y Parameter Measurements

Since noise-specific parameters are not present in (7)–(9), it follows that noise measurements are not necessary to obtain the transistor noise parameters. This remains valid even if correlation between the base and collector noise currents is considered [6]. Consequently, we propose to use (7)–(9) to determine the noise parameters of the transistor $F_{\rm MIN}$, $R_n, Y_{\rm sop}$, from measured Y parameters *only*, eliminating the need for lengthy and "noisy" on-wafer noise measurements. Such a possibility of measuring the 50-Ω noise figure has been suggested earlier [11]. Here, it is extended to the complete set of noise parameters and it is verified in experiments. r_E and $r_B(I_C)$, which are needed in addition to the Y parameters, are obtained as follows. r_E is determined from the frequency and collector current dependencies of the real part of the measured $Z_{12}(f, I_C)$ characteristics, at low $V_{\rm CE}$ bias (<1 V) in order to avoid self-heating effects. First the real part of $Z_{12}(I_C)$ is averaged over the 0.1 GHz . . . 1 GHz range for each bias point I_C. Then r_E is extracted by linear interpolation from the y-axis intercept of the averaged $\text{Re}\{Z_{12}\}$ versus $1/I_C$ curve [12]. Similarly, the collector current-dependent base resistance $r_B(I_C)$ is obtained from the real part of $(Z_{11} - Z_{12})$, averaged at frequencies below 1 GHz, where the impact of the substrate resistance is negligible. No model-related assumptions are made during the extraction about the shape of the $r_B(I_C)$ characteristics. An ac-measured, model-independent, and noise-relevant $r_B(I_C)$ is thus plugged in (7)–(9) to obtain the measured noise parameters.

This technique was implemented in HP-EESOF's device characterization software package, ICCAP, and provides f_T, $f_{\rm MAX}, F_{\rm MIN}, R_n$, $Y_{\rm sop}$, and G_A data from the same routine set of measured Y parameters. It also elegantly solves the nontrivial noise parameter de-embedding problem since the Y parameters have already been de-embedded using a conventional two-step shunt-series technique. Fig. 7 presents measured (from Y parameters) and modeled data for the SiGe HBT emphasizing the impact of the $r_B(I_C)$ model on $F_{\rm MIN}$. The agreement between the Y parameter-derived noise measurements and the conventional noise measurements in Fig. 6 is very good and there is no measurement scatter. Two base resistance models were considered in the simulated characteristics: a) the usual SGP base resistance model for the internal, bias-dependent base resistance term $r_{\rm bi}(I_C)$ (with RBM, RB, and IRB) to which a constant external term RBX is added (Fig. 8), and b) a constant resistance model with RB = RBM. In the case of the constant r_B model, the base resistance was set to more accurately reflect the value at large current bias (peak f_T). In the latter case, the predicted noise figure is optimistic for most of the bias current range. In the case of the bias-dependent SGP base-resistance model, the agreement with the measurements is excellent. The plots indicate that the impact of the base resistance model on the minimum noise figure is only significant at collector currents below the minimum noise current density, where the transistor noise is

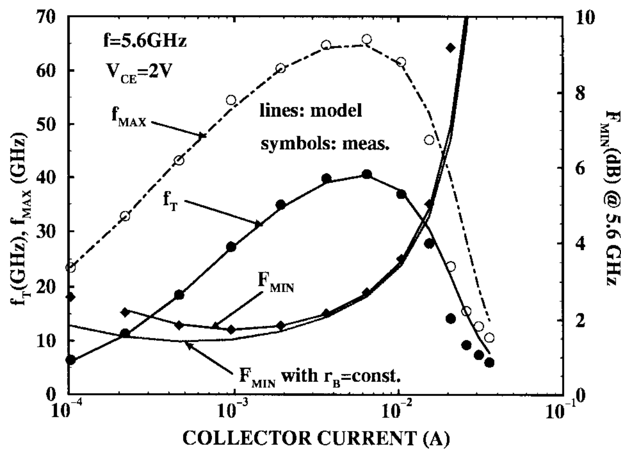

Fig. 7. Measured (from Y parameters) versus SGP-modeled f_T, $f_{\rm MAX}$, and $F_{\rm MIN}$ versus I_C characteristics for 0.5 × 15 μm^2 SiGe HBT, showing impact of the base resistance model on the minimum noise figure.

primarily of thermal origins. Even in that range, the difference is a few tenths of one dB, i.e., within the typical accuracy of on-wafer noise measurements. Based on these experiments and simulations, one expects that, at least for narrow emitter transistors, as is the case of state-of-the-art Si bipolar devices, extracting the base resistance from noise figure measurements alone is of questionable accuracy. An alternative approach is to combine noise and S parameter measurements in the extraction of the small signal parameters [6]. The scatter in the noise measurement can still lead to nonphysical small signal parameters, particularly so if optimization is employed.

In this paper, the SGP base resistance model is obtained as follows: RB is analytically calculated from dc pinched-base resistance measurements and transistor geometry, RBM is set to 0.001 Ω, while IRB and RBX are extracted from the $\mathrm{Re}\{Z_{11} - Z_{12}\}$ and $f_{\rm MAX}(I_C)$ characteristics, as described above. This combined dc and ac-extraction technique, involving highly accurate measurements, appears to provide $r_B(I_C)$ characteristics that, coupled with the appropriate distributed equivalent circuit (Fig. 8), match both the ac (i.e., $\mathrm{Re}\{Z_{11} - Z_{12}\}$, $f_{\rm MAX}$) and the noise behavior of the transistor. The very same RB and RBX values are used in the HICUM model, but the $r_{\rm bi}(I_C)$ dependence follows device physics more closely [2].

IV. Scalable Model Implementation and Verification

The ability to predict the impact of (statistical) emitter width and length variations on the noise parameters depends on the availability of a physically based, scalable compact model. In this paper, *geometry*- and *process-scalable* variants of HICUM [1] and of the SGP models have been used. The scalable HICUM model has been recently described in detail [1]. In the case of the SGP model, the subcircuit presented in Fig. 8 was employed. In addition to the core vertical npn model, it uses external diodes, resistors, and capacitors to reflect the distributed nature of the base resistance and the physical partitioning of the base-emitter and base-collector capacitances [13]. The main features of the scalable SGP model are summarized below.

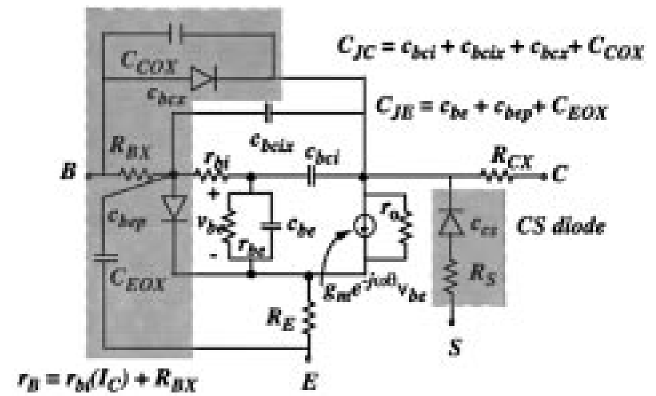

Fig. 8. Small signal equivalent circuit used in the scalable SGP model. Circuit elements added to the core SGP model have been highlighted.

i) An external base-emitter diode is used to account for the different grading coefficients of the voltage dependence of the area and periphery components of the base-emitter capacitance.

ii) The part of the base-collector capacitance corresponding to the selectively implanted collector (SIC) region $c_{\rm bci} + c_{\rm bcix}$ is captured in the internal transistor equivalent circuit whereas the epitaxial part of the collector capacitance $c_{\rm bcx}$ is modeled using the external base-collector diode.

iii) The base resistance is split in a bias-dependent $r_{\rm bi}$ and a bias-independent term $R_{\rm BX}$.

iv) In order to account for the series resistance R_S associated with the collector-substrate region, and to allow for the physical partitioning of the collector resistance and collector-substrate capacitance, an external collector-substrate diode is employed. Even though the value of R_S varies with the number and position of the substrate contacts, its accurate extraction is important as it affects $f_{\rm MAX}$ and, depending on the extraction technique, r_B and even f_T.

v) Bias-independent oxide capacitances associated with the emitter poly overlap of the base $C_{\rm EOX}$ and with the base poly overlap of the field oxide $C_{\rm COX}$ are deployed between the base and the emitter and between the base and the collector, respectively.

vi) The scaling of the low current transit time parameter TF with emitter size is implemented as in HICUM using (8) of [1].

vii) The large current transit time parameter ITF is scaled with emitter area and also accounts for collector current spreading via the same function $f_{\rm cs}$ as HICUM, described by (20) of [1].

viii) Weak avalanche multiplication is implemented using the same equation as in HICUM.

ix) Process scaling is achieved by physically relating area and periphery components of junction capacitances, saturation currents, transit time parameters, internal and external resistances to the pinched base resistance, SIC region resistance, poly sheet resistances, and oxide capacitances.

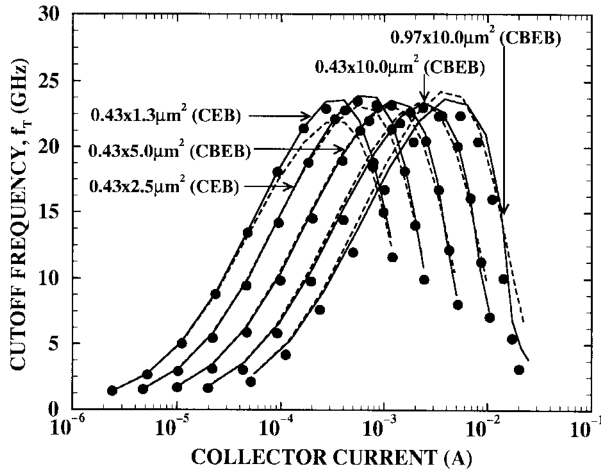

Fig. 9. Measured (symbols) versus HICUM- (solid lines) and SGP- (dashed lines) modeled f_T versus I_C characteristics for "nominal" NT25 Si BJT's biased at $V_{\rm CE} = 1$ V.

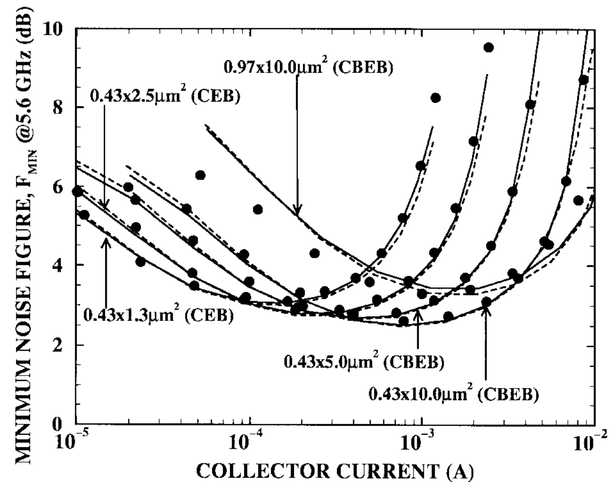

Fig. 10. Measured (symbols) versus HICUM- (solid lines) and SGP- (dashed lines) modeled $F_{\rm MIN}$ versus I_C characteristics for "nominal" NT25 Si BJT's biased at $V_{\rm CE} = 1$ V.

x) All model parameters are derived as functions of emitter geometry and number of emitter, base, and collector contacts, and these functions are implemented as a preprocessor in HSPICE and ELDO decks.

Measured and HICUM- and SGP-modeled f_T and $F_{\rm MIN}$ characteristics are investigated in Figs. 9 and 10, respectively, for different transistor geometries on a "nominal" NT25 wafer at $V_{\rm CE} = 1$ V. The error between measured and SGP and HICUM predicted f_T and $F_{\rm MIN}$ characteristics is less than 7% over all geometries and over the entire bias current range up to more than two times the peak f_T current density. Included in this error are random emitter width variations across the die, typically up to 5%, as well as measurement and de-embedding errors, estimated at 2–3%. This kind of accuracy is also obtained for other $V_{\rm CE}$ bias values ranging from 0.5 V to 3.3 V. The SGP and HICUM model parameters were calculated from the same set of process and geometry data. There was no individual "tweaking" of the model parameters to better fit the characteristics of each transistor. In the low-noise regime, HICUM- and SGP-modeled transistor characteristics are practically indistinguishable. Because of the more sophisticated transit time model, HICUM is slightly more accurate than the SGP model with respect to f_T scaling with transistor geometry at moderate and large currents. In the high-current regime, the dc characteristics are affected by self-heating effects, but the latter do not significantly impact f_T versus I_C characteristics. At present, self-heating effects are only accounted for in the HICUM model. The results in Figs. 9 and 10 establish the accuracy of the scalable HICUM and SGP models and demonstrate their applicability in a new bipolar circuit design philosophy where the transistor geometry becomes part of the design space.

V. Application to LNA Design

Finally, the noise parameter equations and the scalable SGP model are applied to the design of tuned LNA's at 1.9, 2.4, and 5.8 GHz using Si and SiGe double-poly bipolar transistors. Present-day tuned LNA and mixer circuits for wireless systems often trade off noise and input impedance matching [14], [15]. This tradeoff is sometimes caused by the fact that the size of bipolar transistors is not traditionally considered as a design variable which can be continuously varied and optimized in a SPICE deck just like any other circuit element. In other situations, typical for GaAs-based technologies where the importance of optimal noise biasing and matching is well established [16]–[18], the lack of sufficiently accurate physical and scalable transistor models make such an approach unreliable. In the case of Si MOSFET's, where transistor width is a ubiquitous design variable, high-frequency noise performance is at best poorly understood and modeled. To the best of these authors' knowledge, an algorithmic design methodology with an optimal and unique solution to the noise- and input-impedance matching problem has not yet been developed. Instead, a passive network is designed around a given transistor in order to achieve noise matching and/or impedance matching [14], [15]. The passive network itself contributes losses and hence degrades the noise figure. The losses in the passive network increase as the network becomes more complicated and are particularly severe on silicon substrates. For this very reason, in Si RF IC's the matching circuitry is typically left off-chip [15].

Examination of (11) shows that the optimum noise conductance $G_{\rm SOP}$ is different from the input conductance, whereas the optimum noise susceptance $B_{\rm SOP}$ is equal to the complex conjugate of the input susceptance of the device. This is a fundamental characteristic of both bipolar and field-effect transistors and underlies the requirement for separate treatment of matching the real part of the input impedance and the real part of the optimum noise impedance. The goal of the new design philosophy detailed below is to obtain simultaneous noise and input impedance matched circuits. It is applicable to both bipolar and FET circuits.

In order to minimize the losses in the passive network around the transistor, the size of the transistor is first designed so that the transistor becomes noise matched to the characteristic impedance of the system, typically 50 Ω, at the

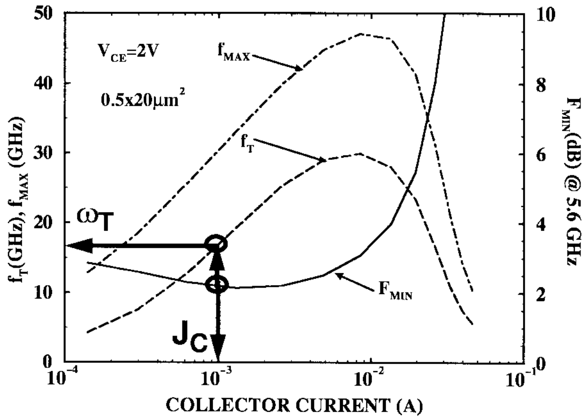

Fig. 11. SGP-modeled $f_T, f_{\rm MAX}$, and $F_{\rm MIN}$ as functions of the collector current for the 0.5-μm emitter, NT25 double-poly Si bipolar process, illustrating the technique for identifying the minimum noise current density J_C and the corresponding cutoff frequency ω_T used in circuit design.

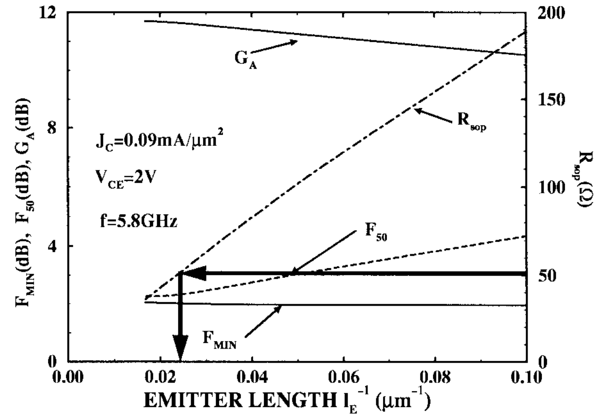

Fig. 12. SGP-modeled noise parameters as functions of the emitter length l_E for the 0.5-μm emitter, NT25 double-poly Si bipolar process. F_{50} is the noise figure in a 50-Ω system. Selection of the emitter length corresponding to an optimum noise source resistance of 50 Ω is also sketched.

desired frequency. Because the transistor is an active device, noise matching is achieved without losses and without noise figure degradation. Since the task of noise matching is removed from the passive network, the latter becomes simpler and less lossy. This can be labeled the *low-noise-matched transistor design stage*. Finally, to complete the circuit, a minimal passive network with two low-loss inductors is designed to provide input impedance matching with the lowest possible degradation of the overall noise figure. This corresponds to *the passive matching network design stage*.

A. Low-Noise-Matched Transistor Design

The transistor design stage first involves finding the optimal noise current density J_C from (9) using the HSPICE deck, as shown in Fig. 11. As mentioned in Section II, the minimum noise figure and the optimum noise current density are practically independent of emitter length. The emitter length is then adjusted so that the optimum source resistance $R_{\rm sop}$ equals Z_0 (50 Ω) at the minimum noise current density and at frequency f, as expressed in (12) and illustrated schematically in Fig. 12. After these two steps, the transistor size and its bias current are determined. The real part of the optimum noise impedance is now matched to 50 Ω without having degraded the minimum noise figure.

B. Passive Matching Network Design

An emitter inductor L_E is added to match the real part of the input impedance to Z_0 [14], [18]

$$L_E \cong \frac{Z_0}{2\pi f_T}. \tag{14}$$

It can be demonstrated using the theory of correlated noise sources in series-series feedback circuits [16] that, if lossless, L_E does not change the value of $R_{\rm SOP}$ but that it does affect the optimum source reactance $X_{\rm SOP}$. For the combined transistor-emitter inductor structure, the latter becomes

$$X_{\rm sop} \cong \frac{\frac{nR_n f_T}{2f}}{\frac{I_C}{2V_T}(r_E + r_B)\left(1+\frac{f_T^2}{\beta_0 f^2}\right) + \frac{n^2}{4}\left(1+\frac{f_T^2}{\beta_0 f^2}\right)} - 2\pi f L_E. \tag{15}$$

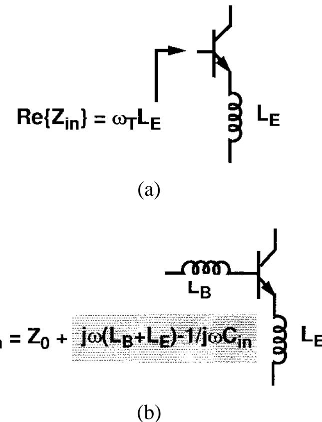

Fig. 13. Illustration of the input impedance matching procedure: (a) adding an emitter inductor to transform the real part of the input impedance to 50 Ω and (b) adding an inductor in the base to simultaneously cancel out the imaginary part of the input impedance and of the optimum noise impedance.

Simultaneous noise and input impedance match is finally obtained by connecting an inductor L_B in the base. It cancels out the reactance due to the input capacitance $C_{\rm in}$ of the device, and, at the same time, it transforms the optimum noise reactance of the amplifier to 0 Ω

$$L_B \cong \frac{1}{\omega^2 C_{\rm in}} - L_E. \tag{16}$$

The matching network design stage is schematically shown in Fig. 13.

This design methodology guarantees optimal noise and input impedance match with the simplest matching network. An LNA design can be completed by adding a suitable matching network in the collector in order to maximize the power gain [18], [19]. Simulation results obtained with LIBRA are shown in Fig. 14. Table I illustrates several design examples at 1.9, 2.4, and 5.8 GHz. Ideal (lossless) inductors were assumed. As expected from the noise parameter equations, the optimal transistor size and bias current decrease with increasing frequency. At 5.8 GHz the SiGe HBT version is

TABLE I
0.5-μm MULTIPLE-FINGER EMITTER, NT25 AND SIGE HBT SINGLE-TRANSISTOR LNA DESIGN DATA AT MINIMUM NOISE BIAS AND $V_{CE} = 2$ V. IDEAL INDUCTORS WERE USED WITH NO OUTPUT MATCHING. CUTOFF AND OSCILLATION FREQUENCY VALUES ARE AT THE LOW-NOISE BIAS CURRENT

	Si npn 1.9 GHz	Si npn 2.4 GHz	Si npn 5.8 GHz	SiGe HBT 5.8 GHz
w_E, l_E	4x0.5x28 μm^2	4x0.5x23 μm^2	2x0.5x20 μm^2	3x0.5x15 μm^2
I_C	3.1 mA	2.5 mA	1.7 mA	1.4 mA
f_T	11 GHz	12 GHz	15 GHz	20 GHz
f_{MAX}	31 GHz	33 GHz	38 GHz	45 GHz
L_E	1.04 nH	1.01 nH	0.54 nH	0.45 nH
L_B	2.30 nH	1.84nH	0.60 nH	1.09 nH
F_{min}	0.87 dB	0.98 dB	2.02 dB	1.43 dB
F_{50}	0.88 dB	0.98 dB	2.02 dB	1.45 dB
G_A	15.2 dB	14.2 dB	11.1 dB	14.0 dB
$\lvert S_{11}\rvert$	-38 dB	-31 dB	-42 dB	-33 dB

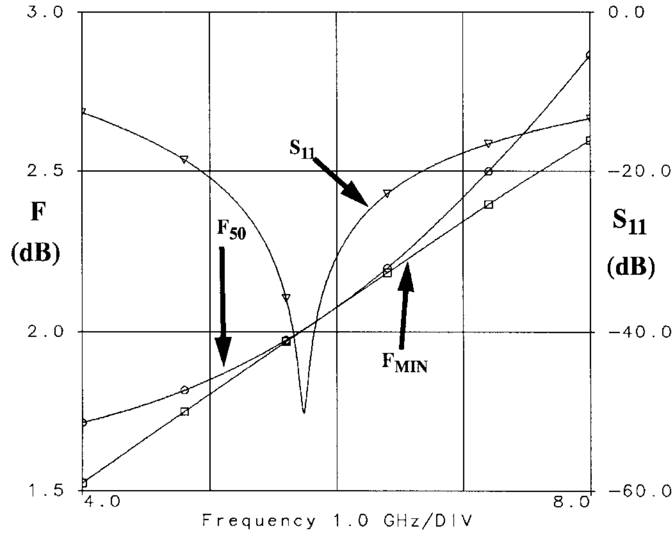

Fig. 14. LIBRA simulated F_{MIN}, F_{50}, and $|S_{11}|$ for a 5.8-GHz LNA employing a $2 \times 0.5 \times 20$ μm^2 Si double-poly transistor at $V_{CE} = 2$ V.

predicted to have lower noise (mostly due to the higher f_T) and higher gain (because of higher f_{MAX}) while dissipating less power than the corresponding Si bipolar circuit.

Single transistor test structures with emitter inductors only, and with both base and emitter inductors, were fabricated in the NT25 Si bipolar process at 1.9, 2.4, and 5.8 GHz. The measured data confirmed the simultaneous noise and input impedance match. The input return loss was better than 19 dB in all cases. Fig. 15 shows the measured input impedance and associated gain for a single transistor structure with on-chip emitter and base inductors as a function of the pinched-base resistance (PBR). The latter was intentionally varied between the process extremes to examine its impact on the manufacturability and yield of tuned LNA's. The measured noise figure varied by 0.2 dB over the estimated process spread of the PBR. Using (13), the small variation in noise figure can be explained by the opposite effects that the PBR has

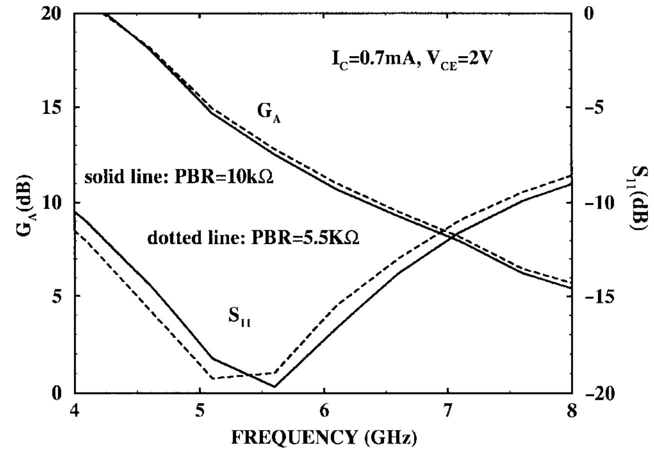

Fig. 15. Measured input impedance and associated gain for a single transistor structure with on-chip emitter and base inductors as a function of pinched-base resistance (PBR) for NT25 bipolar transistors.

on f_T and r_B which tend to cancel out in the same manner as for the maximum oscillation frequency. When compared to the ideal inductor simulation data, the finite Q of the fabricated on-wafer inductors, typically seven to ten, degraded the noise figure by 0.7–1.4 dB. It was found that the base inductor contributed 0.4–0.7 dB to the measured overall noise figure, depending on the inductor value and transistor size. This degradation is proportionally more severe at the lower frequencies (2.4 and 1.9 GHz) where large transistor sizes and large inductor values are required, as indicated in Table I.

The impact of the finite Q of the inductor can be reasonably well accounted for in simulations if an appropriate inductor model is employed [20]. Also, in the previous analytical expressions, the series resistance of the base and emitter inductors can be respectively incorporated into the base and emitter resistances of the transistor. The flow and the validity of the low-noise design methodology remain unaltered. As an example, for a 5.8-GHz tuned cascode LNA fabricated in NT25 and presented in detail elsewhere [19], it was found that the difference between the measured (4.2 dB) and simulated (3.8 dB) noise figures was about 10%. In this case, the common base transistor contributed an extra 1 dB to the overall noise figure of the amplifier. When the base inductor was left off chip, the measured noise figure decreased to 3.8 dB. Clearly, improvement in inductor Q's by using thicker (>3 μm) gold-based metallization and thicker dielectric isolation between the inductor and the Si substrate can have as significant an impact on Si low-noise amplifier performance as moving to the next generation of SiGe-based technology. With similar inductor technology, SiGe still provides 0.5–0.6 dB lower noise figure at 5.8 GHz.

VI. CONCLUSION

The capability of scalable variants of the SGP and HICUM models to accurately predict noise parameters was demonstrated using measurements and simulations on three different high-speed Si and SiGe technologies. A technique for extracting noise parameters from S/Y parameter measurements was described. Finally, a design methodology for low-noise amplifiers was illustrated with the goal of optimizing the

emitter geometry in order to minimize matching circuit losses and overall noise figure. In essence, this design methodology allows for the design of transistors that have the real part of the optimum noise impedance equal to 50 Ω at the desired frequency of operation.

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