An 80-Gb/s $2^{31}-1$ Pseudorandom Binary Sequence Generator in SiGe BiCMOS Technology

Timothy O. Dickson, *Student Member, IEEE*, Ekaterina Laskin, *Student Member, IEEE*, Imran Khalid, Rudy Beerkens, *Member, IEEE*, Jingqiong Xie, *Member, IEEE*, Boris Karajica, and Sorin P. Voinigescu, *Senior Member, IEEE*

***Abstract*—A $2^{31}-1$ pseudorandom binary sequence (PRBS) generator with adjustable output data rates up to 80 Gb/s is reported in a production 130-nm BiCMOS process with 150-GHz f_T SiGe heterojunction bipolar transistor (HBT). The pseudorandom sequence is generated at 20 Gb/s using a linear feedback shift register (FSR), which is then multiplexed up to 80 Gb/s with a 4:1 multiplexer. A BiCMOS logic family combining MOSFETs and SiGe HBTs on high-speed paths is employed throughout the PRBS generator to maximize building block switching speed. Adjustable delay cells are inserted into critical clock paths to improve timing margins throughout the system. The PRBS generator consumes 9.8 W from a 3.3-V supply and can deliver an output voltage swing of up to 430 mV single-ended at 80 Gb/s.**

***Index Terms*—BiCMOS, clock distribution, current-mode logic, PRBS, SiGe HBT.**

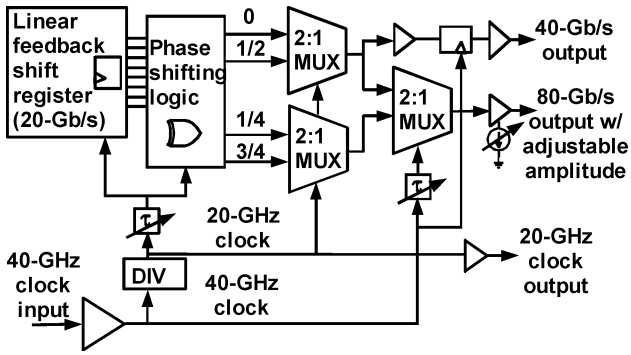

Fig. 1. Simplified system-level block diagram of $2^{31}-1$ 80-Gb/s PRBS generator.

I. Introduction

SILICON GERMANIUM (SiGe) BiCMOS technologies have garnered significant interest for high-speed serial communication circuits for backplane and fiber optic applications. The combination of SiGe heterojunction bipolar transistors (HBTs) and state-of-the-art CMOS makes these technologies attractive for the design of highly integrated broadband circuits, as evidenced by a number of chipsets for 40-Gb/s applications [1]. More recently, high-speed digital building blocks in SiGe bipolar technologies have demonstrated data rates well in excess of 40 Gb/s [2], [3], paving the way for highly integrated transceivers operating at 80 Gb/s or higher. Achieving such a high level of integration at these frequencies still remains a challenge in silicon technologies. Additionally, as data rates in broadband circuits increase, these circuits outperform commercially available test equipment. In particular, pseudorandom binary sequence (PRBS) generators are needed with data rates above 50 Gb/s to provide high-speed digital inputs for testing purposes. To address this issue, recent works have demonstrated 2^7-1 PRBS generators with data rates as high as 100 Gb/s [4]. Typically, longer pattern lengths of $2^{31}-1$ are needed for adequate testing of clock-and-data recovery (CDR) circuits in systems where line coding is not employed. This sequence length is required to ensure that the phase-locked loop in the CDR maintains lock for input data sequences with many consecutive 1s or 0s. While single-chip PRBS generators have been reported with pattern lengths of $2^{31}-1$, their output data rates have been limited to only 15 Gb/s [5].

This work reports the design of a $2^{31}-1$ PRBS generator in a 130-nm BiCMOS technology with 150-GHz f_T SiGe HBT [6]. Output data rates of up to 80 Gb/s are achieved. The design makes extensive use of a true BiCMOS high-speed logic family [7], [8], which combines the best features of the nMOSFET and the SiGe HBT to maximize switching speeds while operating from lower supply voltages than pure HBT implementations. While the BiCMOS implementation of a D-flip-flop (DFF) was reported in [8], the circuits in this work complete the high-speed logic family by introducing other BiCMOS building blocks such as selectors, settable latches, and XOR latches.

II. System Architecture

A simplified system-level block diagram of the $2^{31}-1$ 80-Gb/s PRBS generator is illustrated in Fig. 1. Although fully differential logic is used throughout the design, single-ended signals are depicted in the diagram for simplicity. The pseudorandom sequence is generated at 20 Gb/s using a linear feedback shift register (FSR) and is then multiplexed up to 80 Gb/s using a 4:1 multiplexer (MUX). In order for the output of the 80-Gb/s MUX to exhibit pseudorandom behavior, the four inputs to the 4:1 MUX must be spaced apart by one quarter of the $2^{31}-1$ pattern length [9]. These appropriately shifted outputs are produced using a phase-shifting logic block, which

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T. O. Dickson, E. Laskin, and S. P. Voinigescu are with the Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON M5S 3G4, Canada (e-mail: tod@eecg.toronto.edu).

I. Khalid, R. Beerkens, J. Xie, and B. Karajica are with STMicroelectronics, Ottawa, ON K2H 8R6, Canada.

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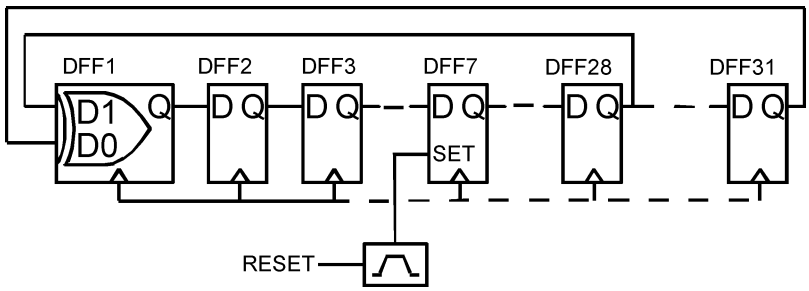

Fig. 2. Block diagram of linear FSR consisting of 31 DFFs.

will be discussed shortly. The only input to the system is a 40-GHz clock signal, which is divided internally to produce a 20-GHz clock. Full-rate (80 Gb/s) and half-rate (40 Gb/s) outputs are available. A revision of the design presented in [10] includes an 80-Gb/s output driver with adjustable output swing control, retiming on the 40-Gb/s output, and a 20-GHz clock output for synchronization. MATLAB and Verilog system level simulations were initially performed to verify the functional integrity of the PRBS system. Once circuit-level design and layout were completed, at-speed transistor-level SPECTRE simulations of the entire system with extracted layout parasitics were run for timing verification.

A. Linear FSR

The $2^{31}-1$ bit sequence is generated at data rates up to 20 Gb/s using an FSR as shown in Fig. 2. It consists of 31 DFFs clocked at 20 GHz. Outputs of the 28th and 31st flip-flops are added together and fed back into the first flip-flop in the chain, thus producing a maximal-length linear sequence with polynomial $x^{31} + x^{28} + 1$. To reduce latency in the feedback loop, the XOR function required to add these outputs is incorporated into the first latch of a master–slave flip-flop. Implementation of this and other latches will be discussed in Section III. Upon reset, a pulse is generated to insert a logic "1" into the seventh flip-flop of the shift register, thus avoiding the all-zero state.

B. Phase-Shifting Logic

The phase-shifting logic block produces four delayed versions of the 20-Gb/s pseudorandom sequence that can be multiplexed to produce an 80-Gb/s pseudorandom output. By making use of the cycle-and-add property of PRBS, a delayed version of a maximal-length sequence can be generated through modulo-2 addition of existing sequences from an FSR [11]. The phase-shifting logic block takes multiple inputs from the 20-Gb/s FSR and produces the four appropriately shifted outputs through a network of adders. Matching path lengths throughout the phase-shifting logic block is critical, as the addition of improperly delayed sequences will produce non-pseudorandom outputs after multiplexing. To avoid this, synchronous modulo-2 addition is performed by employing the same XOR DFF as the first flip-flop of the FSR.

III. Circuit Implementation

A SiGe BiCMOS logic topology is employed throughout the $2^{31}-1$ PRBS generator. In this family, lower-level switching pairs are implemented with nMOSFETs to take advantage of their low input time constant while upper-level switching pairs are realized with SiGe HBTs to take advantage of their high intrinsic slew rate [8].

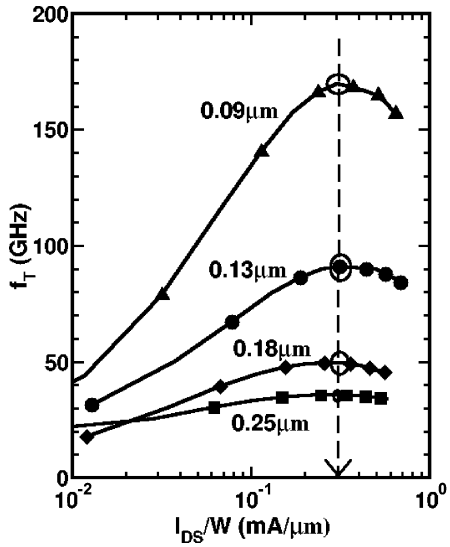

Fig. 3. Measured f_T of nMOSFETs in 250-, 180-, 130-, and 90-nm technologies as a function of drain current density.

Transistor biasing and sizing for optimal switching speed is an important aspect of current-mode logic (CML) circuit-level design at very high data rates. In bipolar designs, techniques for sizing the emitter length based on the peak f_T current density of the device have become fairly common [12]. For our designs, the emitter length $l_{\rm E}$ is sized such that HBT exceeds its peak f_T current density $(J_{\rm pfT})$ when all of the tail current I_T flows through the device, i.e.,

$$l_{\rm E} = \frac{I_T}{1.5 J_{\rm pfT} w_{\rm E}}. \tag{1}$$

Here, the emitter width $w_{\rm E}$ is fixed at the minimum allowed by the technology. A similar approach can be employed for sizing the gate width of nMOSFETs in MOS CML. Fig. 3 presents measured f_T data collected over various MOS technology generations and shows that the cutoff frequency peaks at a drain current density of approximately 0.3 mA/μm irrespective of technology generation. Thus, in MOS CML designs, the gate width of each transistor in a differential pair is sized such that

the MOSFET reaches its peak f_T when all of the tail current I_T in the pair is switched through that device, i.e.,

$$W_{\rm G} = \frac{I_T}{0.3\ {\rm mA}/\mu{\rm m}}. \tag{2}$$

Equivalently, it can be said that each transistor is biased at one half of its peak f_T current density. This technique maximizes switching speed without requiring excessive voltage swing at the gates of the transistors [8]. Furthermore, since the peak f_T current density remains constant as technology scales, current-density-centric biasing schemes allow for designs to be ported to new technology generations without requiring a redesign.

An additional advantage of the BiCMOS logic topology is its potential for low-voltage and low-power operation beyond the 130-nm technology node. When biased at one half of the peak f_T current density, the $V_{\rm GS}$ of a standard threshold 130-nm nMOS is around 650 mV [13]. Replacing SiGe HBTs, whose corresponding $V_{\rm BE}$ is around 950 mV, with nMOSFETs allows for a reduction in supply voltage. Other low-voltage high-speed logic topologies have lowered supply voltages by reducing transistor stacking [14]. However, that technique relies on placing transistors in parallel and doubles the required tail current. As the supply voltage is not reduced by half, the overall power consumption increases. In previous work, we have demonstrated that BiCMOS logic is capable of supporting clock rates of 45 GHz from a supply voltage as low as 2.5 V [8]. However, this PRBS generator operates from a 3.3-V supply voltage due to the use of three-level logic in certain latch structures (to be discussed shortly). Clearly, reducing the supply voltage to 2.5 V can lead to nearly a 25% savings in power consumption. While dual supply voltages could be employed to accommodate three-level logic, this would further add to the overall chip complexity. To avoid additional power supply routing as well as level shifters, a single 3.3-V supply is used throughout the chip.

A. 80-Gb/s BiCMOS MUX

A block diagram of the 80-Gb/s 2:1 MUX used in the final stage of multiplexing is shown in Fig. 4. The 2:1 MUX consists of five inductively peaked D-type latches and an 80-Gb/s 2:1 selector. The implementation of this selector is presented in the schematic of Fig. 5. The fastest signal in the selector, the 40-GHz clock, is applied to the gates of nMOSFETs despite their lower f_T as compared with SiGe HBTs. While this approach may seem counterintuitive, the low input time constant of the nMOSFET is more important for fast switching of the 40-GHz clock signal than the cutoff frequency of the device. The output of the selector is taken from the collector of SiGe HBTs, as their low output capacitance results in fast rise and fall times. Shunt series inductive peaking is used at the output to further enhance switching speed. Shunt peaking inductors $L_{\rm P}1$ and $L_{\rm P}2$ are implemented as three-dimensional (3-D) inductors to minimize area while improving the quality factor and self-resonant frequency [15]. Double emitter followers are employed along the clock path to maximize its bandwidth. Unlike the conventional bipolar $\rm E^2CL$ that typically requires 5-V supplies or higher [2], the use of the BiCMOS topology

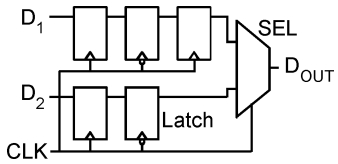

Fig. 4. 80-Gb/s 2:1 MUX consisting of five latches and a BiCMOS selector.

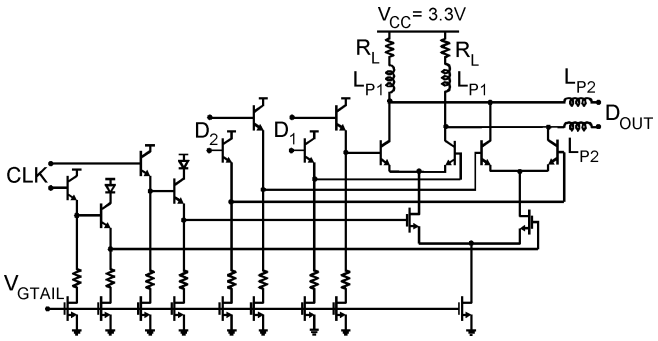

Fig. 5. BiCMOS implementation of 80-Gb/s 2:1 selector employed in the MUX of Fig. 4.

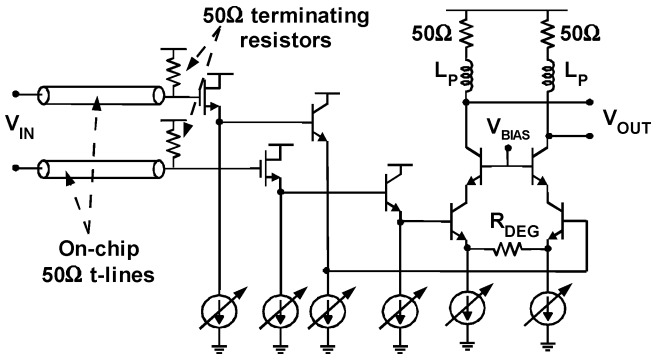

Fig. 6. 80-Gb/s output driver with adjustable output swing control.

allows for reliable operation from a 3.3-V supply without compromising speed. The corresponding power savings is a critical aspect for achieving the high level of integration required in a $2^{31}-1$ PRBS.

B. 80-Gb/s Output Driver With Adjustable Output Swing

A broadband output driver was designed to drive external 50-Ω loads for testing purposes. The driver, whose schematic is shown in Fig. 6, follows the 80-Gb/s selector in the final stage of multiplexing. In layout, the selector and the driver are separated by a 1.5-mm on-chip 50-Ω transmission line. To avoid reflections along this line, 50-Ω terminating resistors must be placed at the input to the driver. A bipolar cascode amplifier is chosen as the gain stage in the output driver. The differential cascode amplifier is loaded with on-chip 50-Ω resistors for impedance matching purposes. When the external 50-Ω load is also considered, a 16-mA tail current in the output driver is required to generate a 400-mV swing per side. Adjustable output swing is achieved by varying this tail current. Emitter degeneration in the output stage not only increases bandwidth but also lessens the impact of varying tail current on the input impedance of the driver. Output voltage swings adjustable between 150 and 450 mV are achieved through this technique.

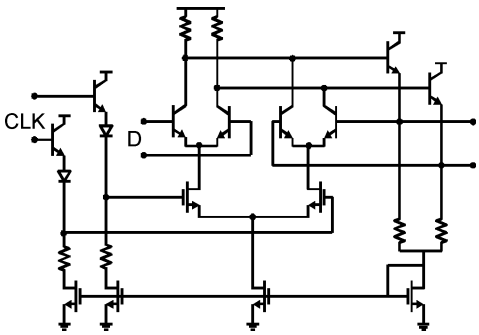

Fig. 7. BiCMOS latch.

For DC level-shifting purposes, source and emitter followers are placed at the input of the driver. Due to the use of a bipolar differential amplifier, double emitter followers cannot be employed at the input of the driver if the circuit is to operate from a 3.3-V voltage supply. Instead, a MOSFET source follower allows for sufficient voltage headroom. Despite the fact that 130-nm MOSFETs are employed on the 80-Gb/s high-speed path, this output driver achieves higher data rates than even the fastest 90-nm CMOS digital circuit reported to date [16].

C. BiCMOS Latches and Flip-Flops

DFFs clocked at 20 and 40 GHz are used throughout the FSR, phase-shifting logic, and the 4:1 MUX. These flip-flops consist of two of the BiCMOS latches placed in a master–slave configuration. As seen from the schematic of Fig. 7, the latch employs a feedback self-biasing scheme. This technique is applied to all latches throughout the PRBS generator to simplify bias distribution on chip. As with the BiCMOS selector, the clock signal is applied to lower-level MOS differential pairs while SiGe HBTs are used to switch high-speed data. Unlike the BiCMOS flip-flop presented in [8], emitter followers are employed in the feedback path instead of source followers. As a 3.3-V supply voltage has been chosen, the voltage headroom is sufficient to allow emitter followers. Inductive peaking is added in the 40-GHz flip-flops to improve the bandwidth without increasing power consumption. However, the 20-GHz flip-flops in the FSR and phase-shifting logic are not inductively peaked in order to save area.

In addition to the standard latch of Fig. 7, two other latch structures are employed in the PRBS design. The XOR function is incorporated into the first latch (Fig. 8) of a master-slave flip-flop to produce the XOR DFF. The XOR latch is also employed in the phase-shifting logic to ensure that synchronous additions are performed. Both data inputs to the XOR latch are applied to SiGe HBTs. It is possible to further reduce the supply voltage in this three-level logic latch if HBTs Q1/Q2 in the second logic level are replaced with nMOSFETs. Furthermore, the seventh flip-flop in the FSR makes use of a settable latch for reset purposes. This latch is realized by modifying the one in Fig. 8 as follows. The inputs of differential pair Q3/Q4 are tied to a logic "1," while a "SET" signal and the input data are applied to Q1/Q2 and Q5/Q6, respectively. When the CLK signal is high (hence M1 is on), the state of the "SET" signal either forces the latch output to a logic "1" or allows the input data to pass through to the output. When the CLK signal is low (hence M2 is on), the output is latched by Q7/Q8.

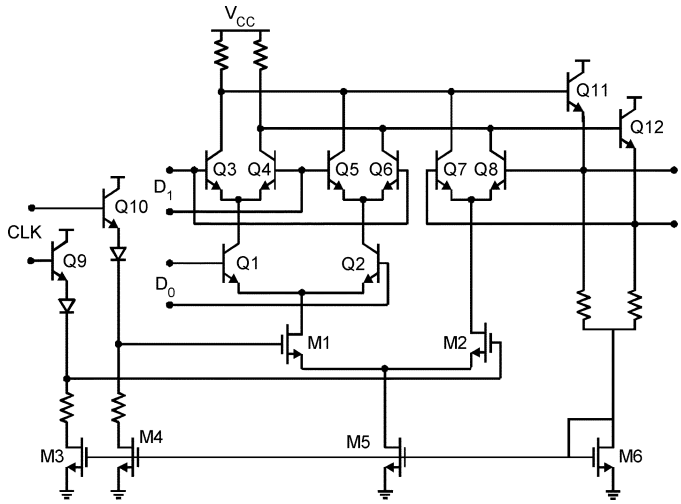

Fig. 8. BiCMOS latch with built-in XOR function.

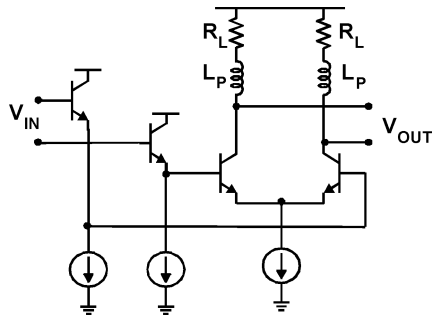

Fig. 9. Bipolar clock buffer.

D. Clock Distribution

Clock distribution is the most critical aspect of the overall system-level design of any high-speed PRBS generator. Careful attention must be paid in the layout routing to match path lengths and to minimize systematic clock skew. Even if the FSR is clocked at a quarter rate, as is the case in this work, delivering a 20-GHz clock signal synchronously to all 31 flip-flops represents a considerable challenge in addition to that of distributing the 40-GHz clock required for multiplexing.

Both the 20- and 40-GHz clock distribution networks consist of cascades of single SiGe HBT inverters (INV), as shown in Fig. 9. Inductive peaking is used in the 40-GHz INV but is omitted in 20-GHz clock buffers to reduce the overall number of on-chip inductors. Each INV has a fan-out of at most three throughout the clock tree to minimize loading. The output voltage swing of each clock buffer is dictated by the required input voltage swing of the loading stage. If the loading stage is another INV, a voltage swing of 300 mV per side and a tail current of 4 mA are sufficient to ensure full switching of the differential pair over all process and temperature corners. Larger voltage swings should be avoided in this loading case, as they require either higher tail current (and hence higher power

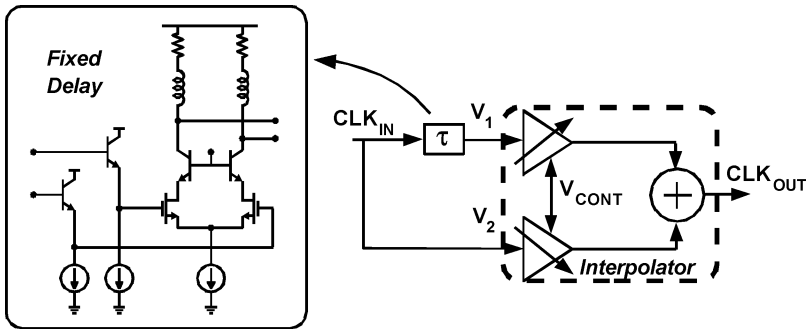

Fig. 10. Concept of adjustable delay cell. (Inset) Implementation of the fixed delay element as a BiCMOS cascode amplifier with emitter follower inputs.

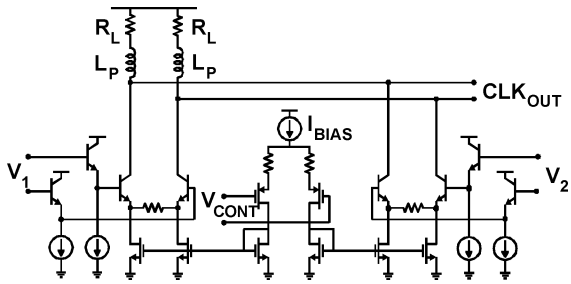

Fig. 11. Implementation of adjustable phase interpolator used in the adjustable delay cell.

consumption) or larger load resistances (and hence lower bandwidth). However, larger voltage swings are needed at the ends of the clock tree when the INV clock buffer drives the MOS switching pair in a BiCMOS logic stage. In a 130-nm technology, the minimum voltage needed for complete switching of a MOS differential pair is approximately 450 mV per side if the sizing guidelines of (2) are followed. However, for complete switching over all process corners and temperatures, the single-ended voltage swing is typically chosen to be 600 mV in this case.

To improve timing margins in critical clock paths, an adjustable delay cell with 50-GHz bandwidth is employed. Its concept is illustrated in Fig. 10. An incoming 40-GHz clock signal is split into a fast and a slow path, which are then interpolated to determine the phase of the output 40-GHz clock. The schematic of the variable phase interpolator is shown in Fig. 11. The two 40-GHz clocks from the fast and slow paths are applied to two SiGe HBT differential pairs. A control voltage, applied to a pMOS differential pair, steers I_{BIAS} between the two SiGe HBT differential pairs to determine the strength with which the signals along the fast and slow paths appear at the output of the interpolator. While this concept of phase interpolation has previously been applied to adjustable delay elements [17], the high bandwidth of the BiCMOS cascode amplifier [8] as the fixed delay element enables operation beyond 40 GHz. The schematic of this fixed delay element is presented in the inset of Fig. 10. Simulations show this amplifier configuration to have more than 70-GHz bandwidth. To avoid output amplitude distortion over the tuning range of the variable delay cell, two design precautions are exercised. First, the two SiGe HBT differential pairs in the interpolator are degenerated to desensitize both their input capacitance and their transconductance to variations in bias current. Moreover, the small-signal gain of the fixed delay element is set to unity to equalize the clock signal amplitudes at the input of the interpolator.

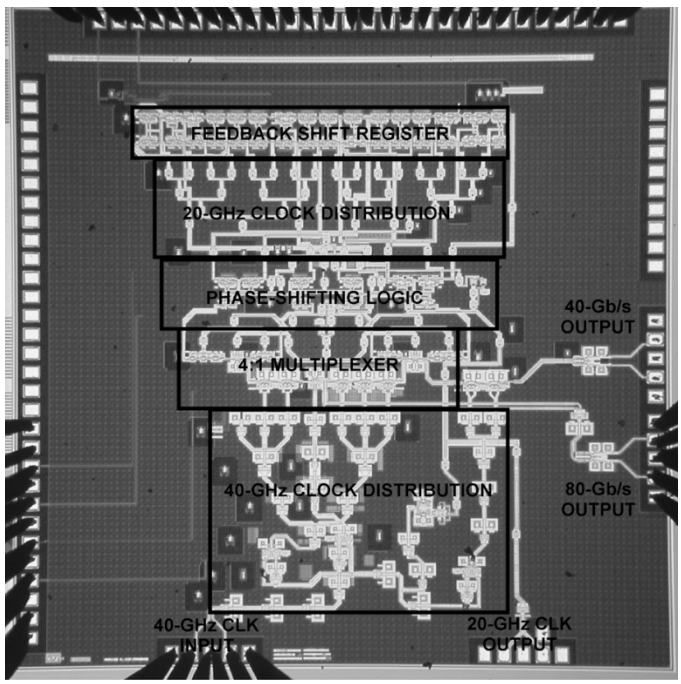

Fig. 12. Die photo of 80-Gb/s $2^{31}-1$ PRBS generator.

IV. Fabrication and Layout

The 80-Gb/s $2^{31}-1$ PRBS generator and other associated test structures were fabricated in a production 130-nm SiGe BiCMOS technology with 150-GHz f_T SiGe HBTs [6]. The chip microphotograph for the PRBS generator is shown in Fig. 12 and occupies an area of 3.5 mm $\times$ 3.5 mm. More than half of the active circuit area is devoted to the distribution of the 20- and 40-GHz clock signals, underscoring the critical role clock distribution plays in the overall system level design. The circuit employs a total of 100 integrated millimeter-wave spiral inductors, primarily along the 40-GHz clock distribution network. Minimizing inductor footprint over substrate is paramount in obtaining adequate self-resonant frequency for millimeter-wave operation [15]. As each multiturn spiral coil is at most 30 μm $\times$ 30 μm, it becomes possible to integrate a large number of inductors on a single chip without occupying excessive area. Reduction of switching noise is also a concern in such a highly integrated high-speed digital circuit. Decoupling

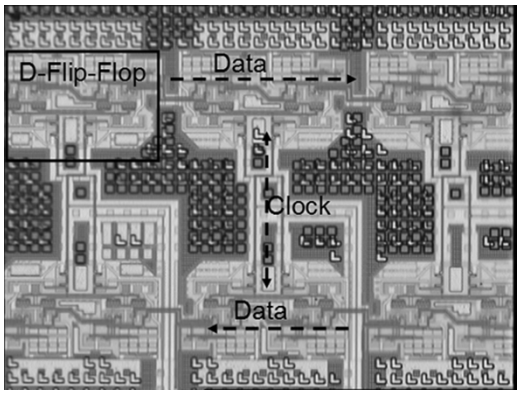

Fig. 13. High-resolution die photo showing details of 20-GHz flip-flops with data and clock routing in the FSR.

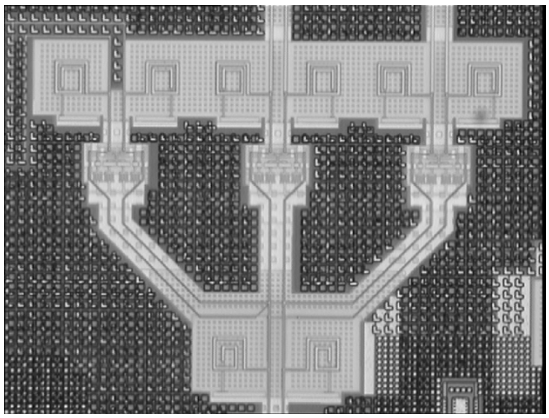

Fig. 14. High-resolution die photo showing details of the 40-GHz clock tree layout.

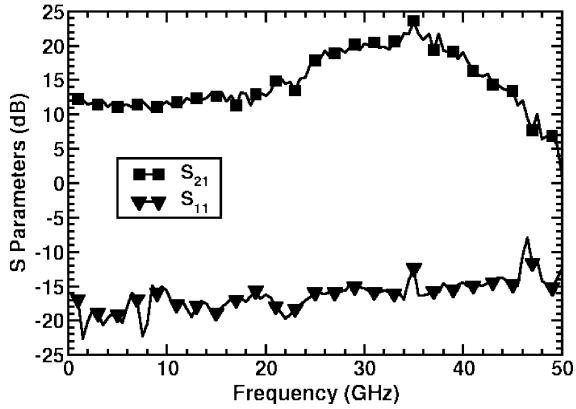

Fig. 15. On-wafer single-ended S_{11} and S_{21} measurements of the clock path.

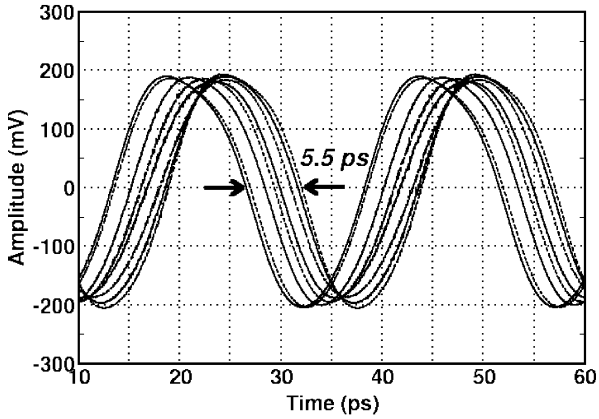

Fig. 16. Time-domain measurements of adjustable delay cell with 40-GHz input clock signal.

capacitors between the supply voltage lines and ground are placed locally throughout the chip layout. Furthermore, n-wells connected to the power supply are inserted beneath resistors in all CML digital building blocks. This helps to reduce noise injection into the silicon substrate and thus improves isolation between blocks.

A high-resolution die photo showing details of the 20-GHz FSR flip-flops is presented in Fig. 13. The flip-flops are placed along two rows to minimize the feedback path length, resulting in at most 550 μm of feedback interconnect. The corresponding delay is approximately 3 ps, which is within the timing margin of the shift register when clocked at 20 GHz. Data input/output lines run horizontally between the flip-flops. The 20-GHz clock signal is distributed in a tree-like manner to each group of four latches (two flip-flops), perpendicular to the data flow.

A test structure with the 80-Gb/s 2:1 MUX block of Fig. 4 was also fabricated. It includes the entire 40-GHz clock tree but does not include the 80-Gb/s output driver found in the PRBS generator. A detail of the 40-GHz clock tree layout is reproduced in Fig. 14. The peaking inductors, smaller than 30 μm per side, are clearly visible. The relatively long microstrip inductors leading to the following stages are essential to extend the distance between clock tree INVs. They contribute series peaking, further improving the bandwidth of the clock tree. Finally, a separate test structure of a single 40-GHz clock path including the adjustable delay cell was also fabricated.

V. Experimental Results

A. Building Blocks

The test structure of the clock path with adjustable delay cell was characterized on wafer. The single-ended S_{11} and S_{21} of the clock path are reproduced in Fig. 15, showing adequate gain and input matching from DC up to 50 GHz. It features intentional gain peaking in the 30- to 50-GHz range to ensure sufficient gain over process variation and temperature even when the clock signal is applied in single-ended mode. Fig. 16 shows large-signal time-domain measurements. As the control voltage is varied, the delay can be adjusted by approximately 5.5 ps, which corresponds to a 79° phase shift at 40 GHz. Constant signal amplitude is maintained over the entire tuning range. The 2:1 MUX was measured separately and its operation was verified up to 80 Gb/s, as seen in Fig. 17.

B. PRBS Generator

First, the clock path and the divider chain were verified to be operational for single-ended clock signals in the 3–57-GHz range by measuring the divide-by-two clock output available at the bottom of the die. Note that, due to the physical limitation of having more than four probes mounted at the same time, the divide-by-two clock output and the data outputs cannot be probed at the same time on wafer. This prevents the clock output

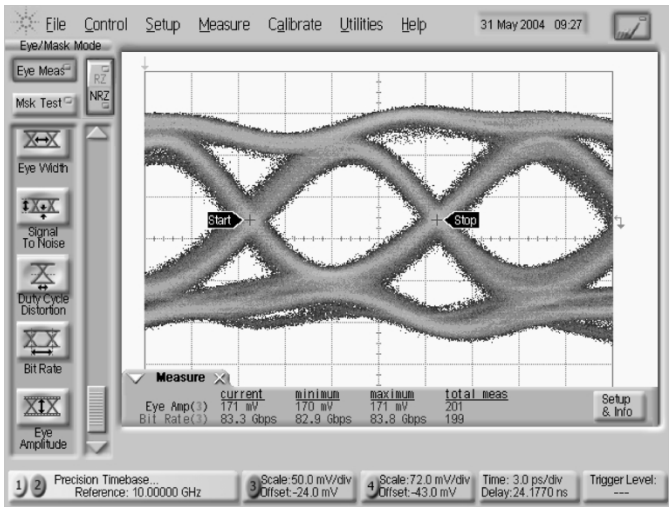

Fig. 17. Measured 80-Gb/s output eye diagrams of the 2:1 MUX test structure.

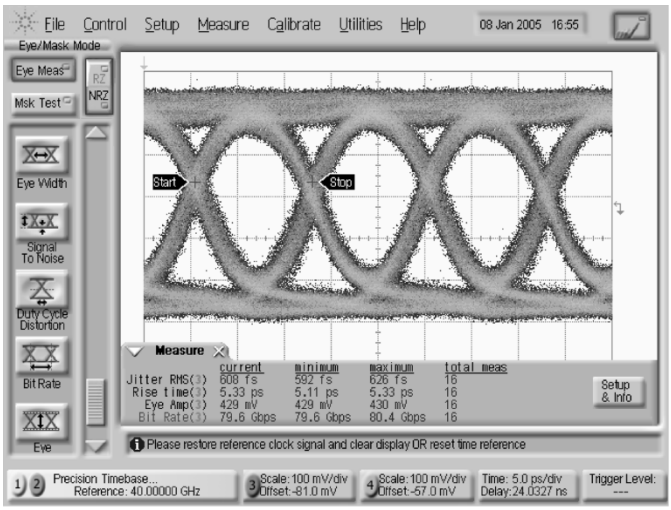

Fig. 18. 80-Gb/s eye diagrams measured with 110-GHz probes. Errors are produced due to drifting of the two signal sources used to synchronize the PRBS generator and the precision timebase of the Agilent DCA.

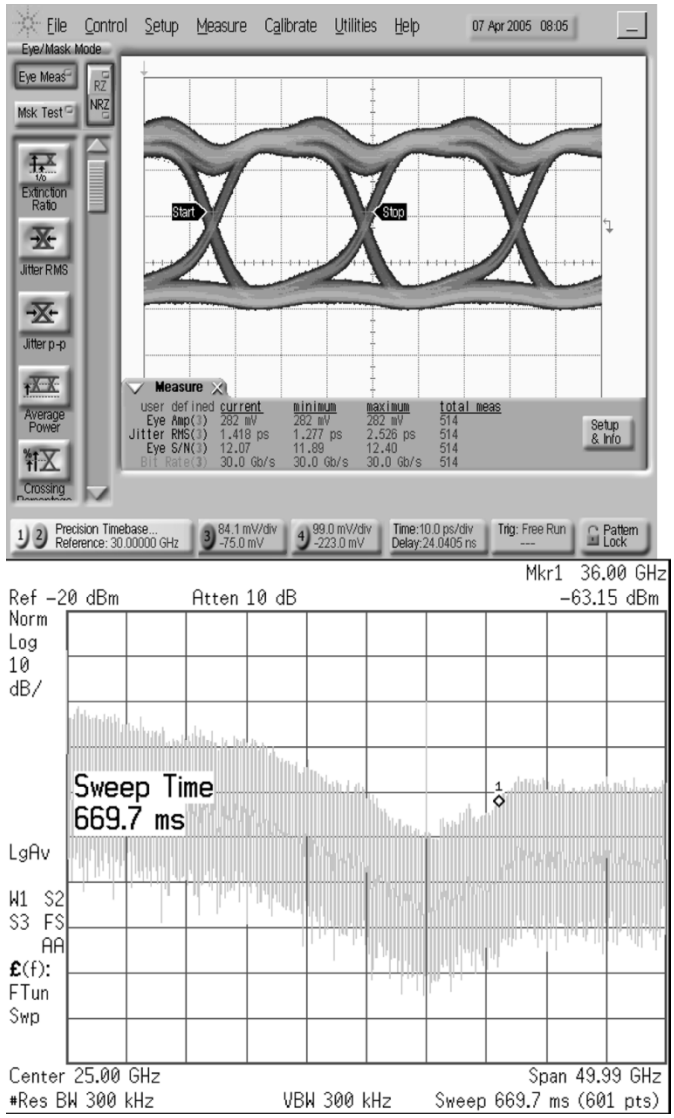

Fig. 19. Measured large-signal eye diagrams and corresponding spectral content of a 30-Gb/s $2^{31}-1$ PRBS pattern from the half-rate output.

of the PRBS chip from being used for synchronization during on-wafer measurements.

Eye diagrams at full rate and half rate outputs of the PRBS generator were measured using an Agilent 86100C DCA with the 86118 A 70-GHz dual remote sampling heads and external precision timebase. A 67-GHz signal source (Agilent E8257D), along with a power splitter, was employed to synchronize both the PRBS generator and the precision timebase of the DCA. At 80 Gb/s, as little as 1-ps delay mismatch along the clock path can impact the alignment of the 40-GHz clock and data signals at the input of the final 2:1 MUX. Therefore, the adjustable delay cells in the 40-GHz clock path are manually tuned to maximize the eye opening and minimize duty-cycle distortion. Once set, the control voltage of the delay cell was found to be consistent over different dice and data rates. Using this setup and 110-GHz GGB probes, eye diagrams were measured at data rates up to 80 Gb/s, as seen in Fig. 18. The 5.3-ps 20%–80% rise time is comparable to that obtained in a recently reported 132-Gb/s digital building block implemented in a 210-GHz f_T SiGe bipolar technology [3]. The output jitter of the 80-Gb/s eye is 600 fs rms, with an output swing of $2\times 430\ \mathrm{mV_{pp}}$. Note that the addition of the 80-Gb/s output driver compensates for losses in the 1.5-mm on-chip transmission lines and reduces clock feedthrough in the measured output eye diagram as compared with the 80-Gb/s eye diagram from the MUX test structure shown in Fig. 17.

Next, the spectral content up to 50 GHz of the pseudorandom output was obtained with an Agilent E4448 spectrum analyzer using GGB 67-GHz differential probes. Large-signal eye diagrams were measured on the DCA simultaneously by examining the other differential output. Figs. 19 and 20 demonstrate 30- and 60-Gb/s output eye diagrams along with the corresponding spectral content of the half rate and full rate outputs, respectively, when a single-ended 30-GHz signal is applied to the clock input of the PRBS generator. As compared with previously reported data from an earlier design [10], the addition of retiming on the half-rate output eliminates the appearance of

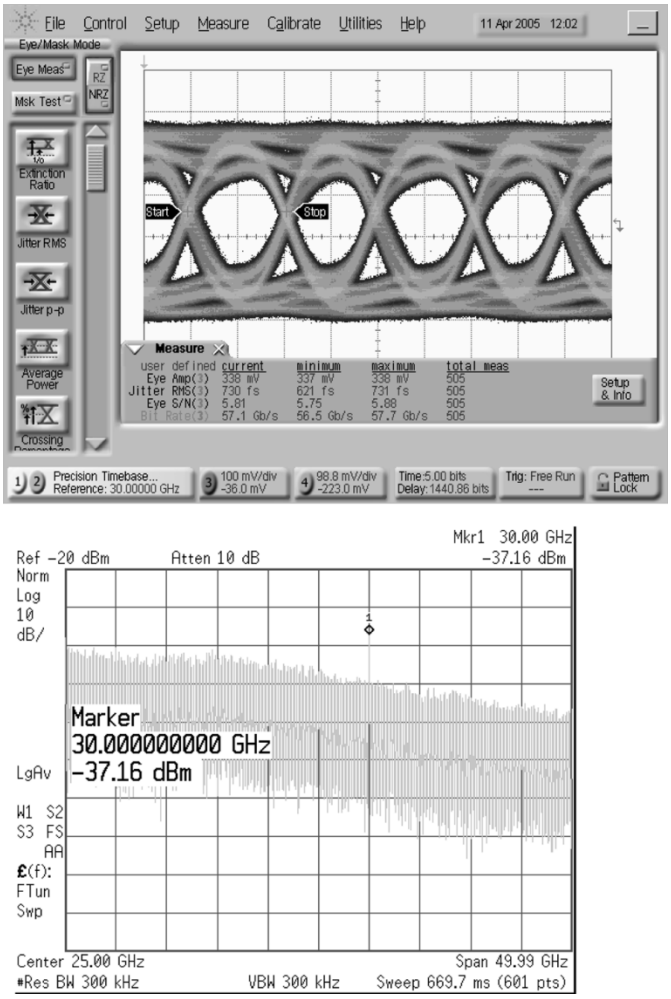

Fig. 20. Measured large-signal eye diagrams and corresponding spectral content of a 60-Gb/s $2^{31}-1$ PRBS pattern from the full-rate output.

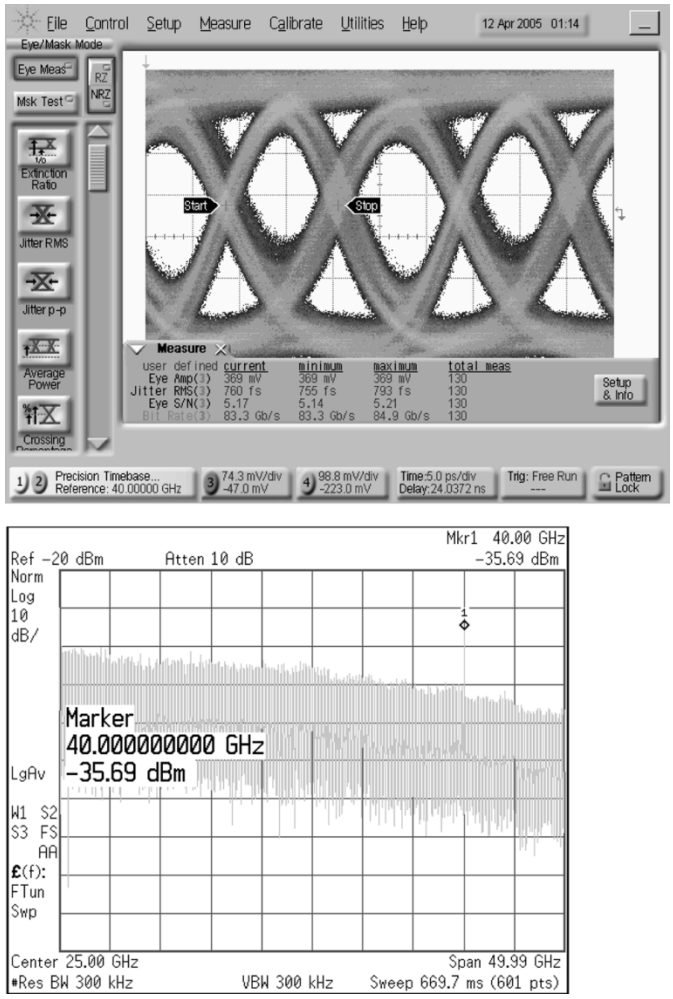

Fig. 21. Measured large-signal eye diagrams and corresponding spectral content of a 80-Gb/s $2^{31}-1$ PRBS pattern from the full-rate output.

a divide-by-two clock signal in the output spectrum. Since retiming is not performed on the full-rate output, a 30-GHz clock tone is observed in the 60-Gb/s output spectrum in Fig. 20. As the Agilent DCA takes approximately three measurements per second, the 500 measurements of the 60-Gb/s eye correspond to a persistence of 167 s and a total of more than 10^{13} measured bits. Similarly, eye diagrams and spectral content for the PRBS generator operating at 80 Gb/s are presented in Fig. 21. The number of eye readings indicates that more than 3×10^{12} bits have been measured. Note that the rise and fall times are worse than those presented in Fig. 21 due to the use of lower bandwidth 67-GHz probes.

The most challenging aspect in the testing of a $2^{31}-1$ PRBS is the verification of the pattern length in the absence of a commercially available error detector. At shorter pattern lengths such as 2^7-1, certain oscilloscopes can lock onto the pattern. This allows for individual bits to be displayed, and thus a 127-bit sequence can be easily identified by inspection. This technique has been widely used in a number of previously reported single-chip PRBS generators with pattern lengths of 2^7-1 [4], [18], [19]. Even the current state-of-the-art Agilent DCA 86100C with pattern-locking capabilities only has sufficient memory to lock to a PRBS pattern length of $2^{23}-1$. Therefore, this technique cannot currently be applied to a $2^{31}-1$ pattern.

The most compelling evidence of the pattern length lies in the spectral content of the PRBS signal. Theory predicts that the spectrum of a 2^n-1 pseudorandom sequence is comprised of discrete tones spaced apart by

$$\Delta f = \frac{f_{\mathrm{BR}}}{2^n - 1}. \tag{3}$$

Here, f_{BR} is the bit rate frequency (i.e., 80 GHz for an 80-Gb/s sequence). For a pattern length of 2^7-1, these discrete tones can readily be resolved [20]. As the pattern length increases, the tone spacing becomes smaller and the entire spectrum resembles a continuous $\sin(x)/x$ function as expected from random non-return-to-zero (NRZ) data [21]. Fig. 22 presents measured eye diagrams along with DC-to-50-GHz spectral content of a 17-Gb/s $2^{31}-1$ sequence from the PRBS generator. By reducing the resolution bandwidth of the Agilent E4448 spectrum analyzer to 1 Hz and examining the spectral content over a 30-Hz span cen-

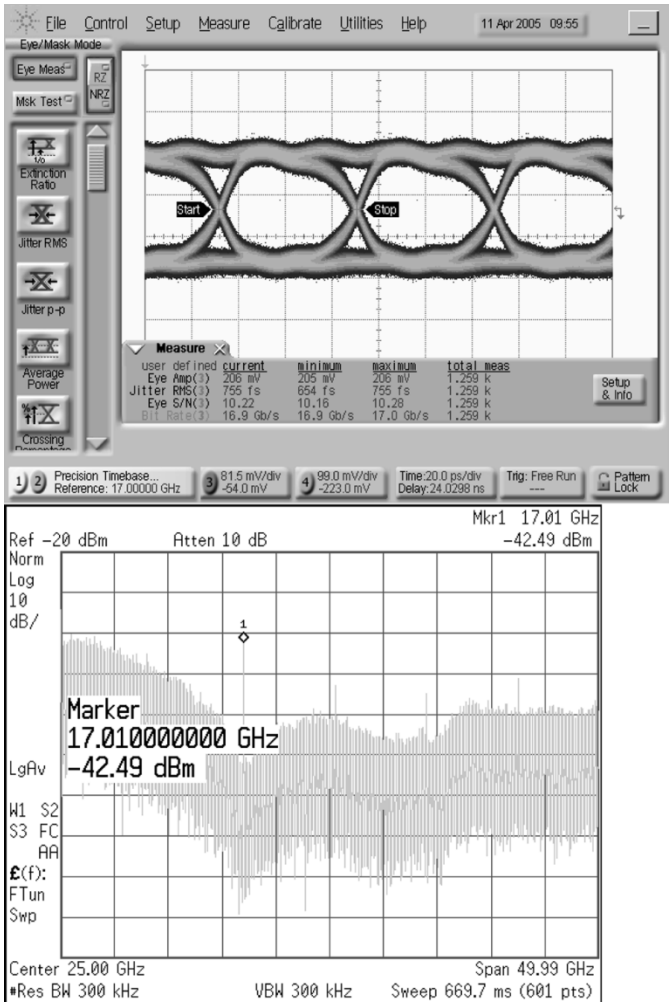

Fig. 22. Measured large-signal eye diagrams and corresponding spectral content of a 17-Gb/s $2^{31}-1$ PRBS pattern.

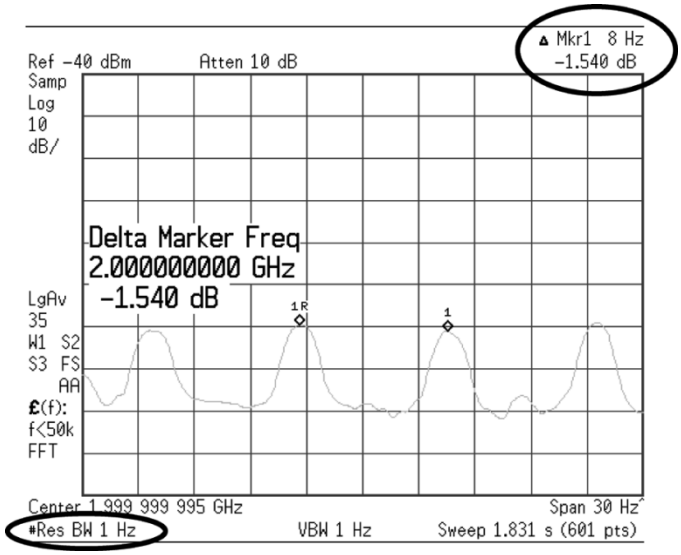

Fig. 23. Spectral content of a 17-Gb/s PRBS pattern measured using a spectrum analyzer with 1-Hz resolution bandwidth. Discrete tones spaced apart by 7.9 Hz can be distinguished, corresponding to a sequence length of $2^{31}-1$.

TABLE I
PERFORMANCE SUMMARY OF 80-Gb/s PRBS GENERATOR

Technology	SiGe BiCMOS (130-nm CMOS, 150-GHz SiGe HBT)
Supply Voltage	3.3 V
Power Consumption	9.8 W
Output Data Rate	5 – 80 Gb/s (adjustable)
Pattern Length	2^{31}-1
Output Swing	180 - 430mV x 2 @ 80-Gb/s (adjustable)
Output Jitter	600fs (RMS)
Rise Time (20-80%)	5.3 ps
Components	1118 MOSFETs
	1519 SiGe HBTs
	100 integrated spiral inductors
Chip Size	3.5 x 3.5 mm^2

tered near 2 GHz, it is possible to resolve the discrete tones of this $2^{31}-1$ sequence as seen in Fig. 23. The 8-Hz spacing identified by the spectrum analyzer is close to the 7.91 Hz predicted by (3) and indicates that the FSR and phase-shifting logic generates the correct $2^{31}-1$ pattern length at lower speeds. Note that the power associated with each individual tone in this 17-Gb/s sequence is very small—approximately -100 dBm near 2 GHz. As the NRZ power spectrum decreases with frequency, it is not possible to resolve these tones for the 17-Gb/s pattern at higher frequencies. Additionally, the NRZ power spectrum is proportional to the bit interval [21]. Therefore, as the data rate is increased beyond 17 Gb/s, the power becomes distributed over a wider frequency range and observation of these tones becomes limited by the sensitivity of the spectrum analyzer. While sequence length can be verified at lower data rates, it is not possible to the authors' best knowledge that the $2^{31}-1$ sequence length can be identified at 80 Gb/s at this time.

The performance of the PRBS generator is summarized in Table I. The circuit consumes 9.8 W from a 3.3-V supply. The 20- and 40-GHz clock distribution network accounts for 45% of the total power consumption.

VI. CONCLUSION

For the first time, a single-chip PRBS generator with a pattern length of $2^{31}-1$ has been demonstrated at a data rate above 15 Gb/s. The design, implemented in a production 130-nm SiGe BiCMOS technology with 150-GHz f_T SiGe HBTs, makes extensive use of a SiGe BiCMOS logic family that takes full advantage of the best features of both nMOSFETs and SiGe HBTs to achieve 80-Gb/s operation. With over 2600 transistors and 100 integrated spiral inductors, this work represents the highest level of single-chip integration reported to date at data rates above 40 Gb/s and demonstrates the potential for designing highly integrated 80-Gb/s broadband transceivers using this true BiCMOS high-speed logic family.

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Timothy O. Dickson (S'01) received the B.S. (Hons) and M.E. degrees in electrical engineering from the University of Florida, Gainesville, in 1999 and 2002, respectively, and is currently working toward the Ph.D. degree at the University of Toronto, Toronto, ON, Canada.

From 2000 to 2002, he was a Graduate Research Assistant at the University of Florida, where he investigated isolation issues in RF and mixed-signal silicon-based technologies. He has held internships in the areas of analog and RF circuit design at Dallas Semiconductor and Global Communication Devices. His research interests lie in the area of high-frequency integrated circuits for wireless and wireline communications.

Mr. Dickson was named an undergraduate University Scholar by the University of Florida in 1999. In 2004, he received the Best Student Paper Award at the VLSI Circuits Symposium in Honolulu, HI. He holds a University of Toronto Doctoral Fellowship and is an Edward S. Rogers, Sr. Scholar.

Ekaterina Laskin (S'04) received the B.ASc. (Hons) degree in computer engineering from the University of Toronto, Toronto, ON, Canada, in 2004, and is currently working toward the M.S. degree at the Department of Electrical and Computer Engineering, University of Toronto.

Her research interests include the design of millimeter-wave and high-speed integrated circuits.

Ms. Laskin was a University of Toronto Scholar from 2000 to 2004. She received the National Science and Engineering Research Counsel of Canada (NSERC) undergraduate student research award in industry and university in 2002 and 2003. She currently holds the NSERC Postgraduate Scholarship.

Imran Khalid received the B.Eng. degree in electrical engineering from Carleton University, Ottawa, ON, Canada, in 1999.

He joined Nortel Networks in 2000, where he worked on design methodology for SiGe bipolar technologies. In the later part of 2000, he joined STMicroelectronics, Ottawa, ON, Canada, where he currently designs high-speed communication blocks for serial transceivers using high-performance SiGe-BiCMOS technologies. His scientific interests include high-speed broadband communication blocks for Ethernet and backplane applications.

Mr. Khalid was awarded the Merit of Technical Excellence by STMicroelectronics in 2005.

Rudy Beerkens (M'91) received the B.Sc. degree in electrical engineering from the University of Waterloo, Waterloo, ON, Canada, in 1986.

From 1986 to 2000, he was with Nortel Networks, Ottawa, ON, Canada, during which time he was involved in the areas of semiconductor manufacturing, BiCMOS process development, yield enhancement, device characterization, and reliability. In 2000, he joined STMicroelectronics, Ottawa, where he currently heads an integrated circuits design team. His scientific interests include high-speed broadband and millimeter-wave integrated circuits.

Jingqiong Xie (M'98) received the B.Eng. and M.Eng. degrees from Zhejiang University, Hangzhou, China, in 1983 and 1986, respectively, and the Ph.D. degree from the University of Newcastle, Newcastle, Australia, in 1997.

From 1986 to 1993, he was with Southeast University, Nanjing, China, where he worked on real-time electronic control systems. From 1997 to 2000, he was with Calian Technology, Ottawa, ON, Canada, where he worked on sonar signal processing. In 2000, he joined STMicroelectronics, Ottawa, where he works on high-speed clock and data recovery, frequency dividers, VCOs, I/O buffers, ASIC physical design, and signal integrity. His research interests include transistor-level circuits design methodology, digital and analog signal processing, and system-level design and integration.

Boris Karajica was born in Banjaluka, Yugoslavia, in 1977. He received the B.E.E. degree from Carleton University, Ottawa, ON, Canada, in 2000.

He joined STMicroelectronics, Ottawa, as a Test and Product Engineer for optoelectronics applications. In 2001, he joined the Central Research and Development group of STMicroelectronics for high-speed and millimeter-wave applications. He has been working on high-speed modules for OC-768 application in SiGe BiCMOS technology. His scientific interests include high-speed laser drivers, laser modulator drivers, high-speed data buffers, and implementation of test strategies for high-speed applications.

Sorin P. Voinigescu (S'92–M'91–SM'02) received the M.Sc. degree in electronics from the Polytechnic Institute of Bucharest, Bucharest, Romania, in 1984, and the Ph.D. degree in electrical and computer engineering from the University of Toronto, Toronto, ON, Canada, in 1994.

From 1984 to 1991, he was involved with research and development and with academia in Bucharest, where he designed and lectured on microwave semiconductor devices and integrated circuits. From 1994 to 2002, he was with Nortel Networks and Quake Technologies in Ottawa, ON, Canada, where he was responsible for projects in high-frequency characterization and statistical scalable compact model development for Si, SiGe, and III–V devices. He also led the design and product development of wireless and optical fiber building blocks and transceivers in these technologies. In September 2002, he joined the Department of Electrical and Computer Engineering, University of Toronto, as an Associate Professor. He has authored or co-authored over 60 refereed and invited technical papers spanning the simulation, modeling, design, and fabrication of GaAs-, InP-, and Si-based heterostructure devices and circuits. His research and teaching interests focus on nanoscale semiconductor devices and their application in integrated circuits at frequencies beyond 100 GHz.

Dr. Voinigescu is a Member of the Technical Program Committee of the IEEE Compound Semiconductor Integrated Circuits Symposium. He was a co-recipient of the Best Paper Award at the 2001 IEEE Custom Integrated Circuits Conference.