High-Speed SiGe BiCMOS Technologies: 120-nm Status and End-of-Roadmap Challenges

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***Abstract* — This paper presents the status of high-speed SiGe BiCMOS technologies at STMicroelectronics. Process and electrical characteristics of two 120-nm platforms, qualified or under development, are presented together with results demonstrated on optical and millimeter-wave circuits. Advanced developments addressing end-of-roadmap BiCMOS are also presented and discussed.**

***Index Terms* — BiCMOS, Heterojunction Bipolar Transistors (HBT), millimeter-wave circuits, optical communications, Silicon Germanium (SiGe).**

I. Introduction

SiGe BiCMOS technologies extend the application range of Si technologies towards higher frequencies. Just as the frequency limit of CMOS technologies is increased with gate length reduction, encroaching on markets and products which were covered by BiCMOS in the past, SiGe BiCMOS is now able to address applications above 50 GHz, previously the domain of III-V technologies. Although these very same high-speed applications are also targeted by advanced CMOS technologies, SiGe BiCMOS continues to have the performance edge [1]. This paper presents the status of ST's most advanced high-speed SiGe BiCMOS technologies going from a production 120-nm BiCMOS platform to current developments on high-speed HBTs for end-of-roadmap CMOS nodes. Approaches to increase device performance, which take into account integration constraints of advanced CMOS, are summarized and results are presented. We finally discuss the perspectives of high-speed BiCMOS technologies.

II. Current Status: 120-nm BiCMOS Platforms

A. A platform available for production: BiCMOS9

The most advanced high-speed SiGe BiCMOS technology in production at STMicroelectronics is the so-called BiCMOS9 [2]. This technology, whose main characteristics are summarized in Table 1, offers a quasi self-aligned (QSA) 160-GHz f_T / f_{max} Si/SiGeC HBT (f_T and f_{max} being respectively the transit and the maximum oscillation frequencies), dual V_T (high performance / low leakage) and dual gate oxide (1.2 V / 2.5 V) 120-nm CMOS devices, passives and a 6-level copper back-end. A high-voltage HBT (BV_{CEO} = 3 V) is also available.

Table 1 ST 120-nm high-speed SiGe BiCMOS technologies.

Technology Targets	**BiCMOS9**		**BiCMOS9MW**	
CMOS	T_{OX}=20nm (GO1) / T_{OX}=50nm (GO2) –			
(NMOS & PMOS)	High & Low V_T (mV)			
N: 120nm/1.2V (GO1)	450	340	450	340
P: 120nm/1.2V (GO1)	395	300	395	300
N: 280nm/2.5V (GO2)	430	140	430	140
P: 280nm/2.5V (GO2)	485	180	485	180
Si/SiGe:C HBT	QSA structure		FSA structure	
	W_E = 170 nm		W_E = 120 nm	
f_T (GHz)	160		230	
f_{max} (GHz)	160		280	
BV_{CEO} (V)	1.8		1.6	
BEOL (Cu)	6ML + Al		6ML + Al	
thin / thick Cu layers	5 / 1		3 / 3	
α *@ 80GHz* (dB/mm)	1.2		0.5	

Manufacturability of this technology is assessed by the histograms shown in Fig. 1 for the current gain (at medium injection) and the pinched base resistance of bipolar transistors. These statistics have been collected on 45 lots produced in the last 9 months (January 1st to beginning of October 2006). Standard deviation is about 10% for the current gain and below 5% for the pinched base resistance.

BiCMOS9 has been designed to address optical networking and wireless applications up to 40 Gb/s – 40 GHz. Numerous circuits have been fabricated in this technology, demonstrating its suitability for the targeted applications. A low-power flip-flop (2.5 V / 20 mW) has been validated at 40+ Gb/s [3]. Fig. 2 and Fig. 3 show the layout and 45-Gb/s eye diagram of this circuit. Circuits

operating at 80 Gb/s have also been demonstrated using the MOS-HBT ECL and CML logic families [4]-[5]. Millimeter-wave building blocks such as a 40-GHz LNA [6], a 70-GHz frequency divider [7] and a 95-GHz VCO [8] further illustrate the technology capabilities.

The largest circuit in production today has a surface area close to 200 mm². Yield up to 35%, a record for such a large ASIC, is reached thanks to a D_0 as low as 110 defects / m².

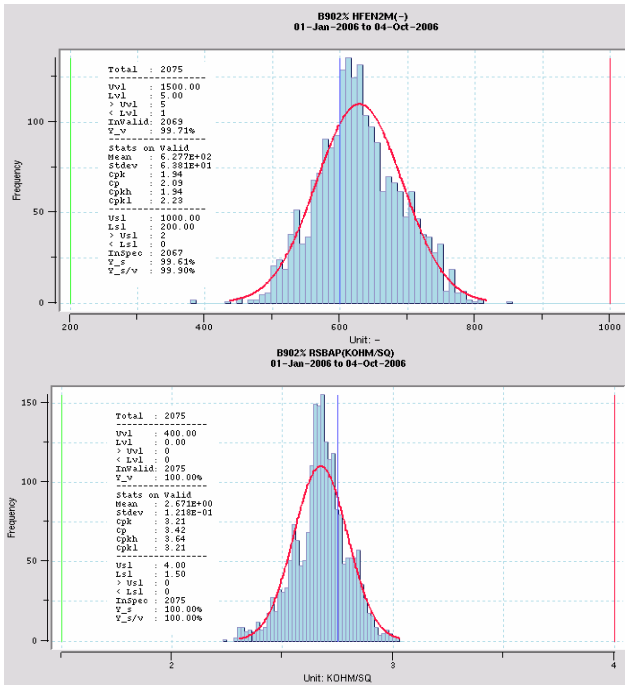

Fig. 1. Current gain at V_{BE} = 0.75V of 0.17×5.6µm² HBTs (Top) and Pinched Base Resistance (Bottom) histograms built with measurements done on 45 BiCMOS9 lots produced over about 9 months.

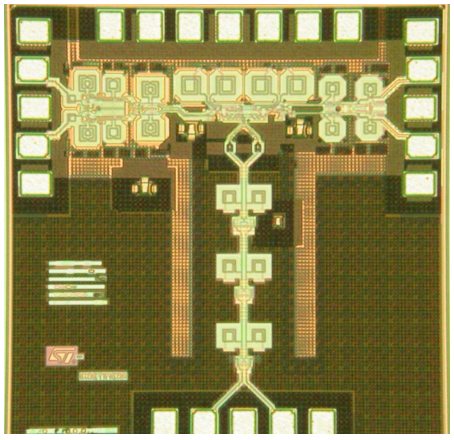

Fig. 2. ST 120-nm BiCMOS9 retimer die photo [3].

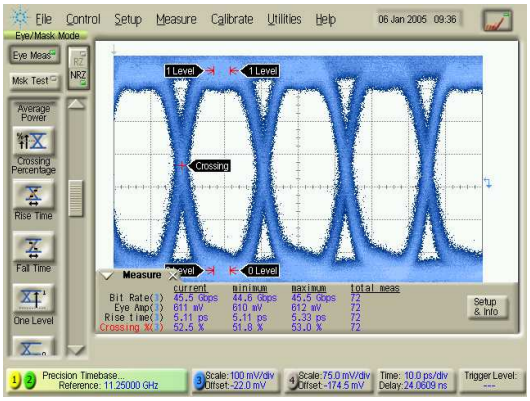

Fig. 3. ST 120-nm BiCMOS9 45 Gb/s output eye diagram [3].

B. A new platform dedicated to millimeter-wave applications: BiCMOS9MW

Applications such as 60-GHz WLAN, 77-GHz automotive radars and 80-Gb/s optical communications can not be addressed with BiCMOS9 technology. Since a first limitation is the HBT performance, many studies have been conducted to increase f_T and f_{max} above 200 GHz [9]-[10]. 230-GHz f_T and 280-GHz f_{max} (cf. Fig. 4) have been achieved with a fully self-aligned (FSA) architecture using selective epitaxial growth of the base. The device features record low minimum noise figures NF_{min} of 1.2 dB at 40 GHz and 1.6 dB at 60 GHz (cf. Fig. 4).

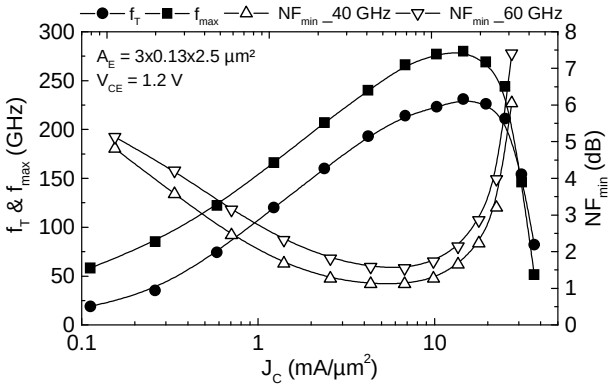

Fig. 4. f_T, f_{max} and NF_{min} @ 40 GHz and 60 GHz vs. current density of a 3 × 0.13 × 2.5 µm² FSA Si/SiGeC HBT.

This FSA architecture has reached a good maturity level. Fig. 5 exhibits indeed the full mapping (35 dice) of Gummel characteristics measured on yield monitors (arrays of more than 3000 devices). None of the measurable device is failing. Furthermore, collector current is ideal down to a V_{BE} = 0V and base current remains below 0.2 nA at low injection, i.e. below the pA/µm² for all the arrays. The shape of the base

current observed at low V_{BE} on yield monitors is the signature of a band-to-band tunneling current [11]. Besides, Fig. 6 shows that HF characteristics are very uniform with standard deviations below 2% within a wafer (76 dice) for both f_T and f_{max}.

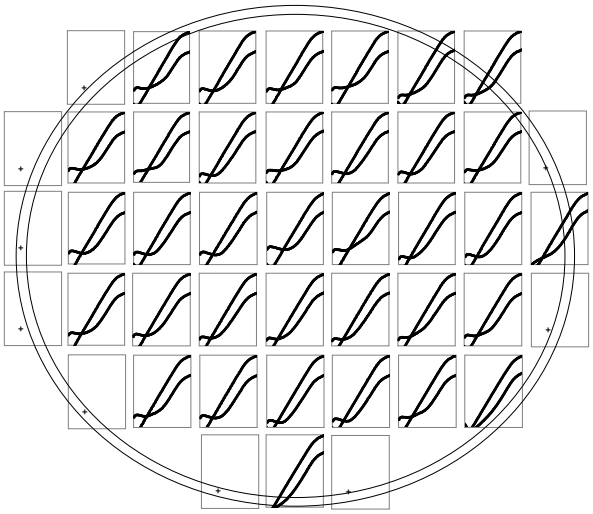

Fig. 5. Mapping of Gummel characteristics at V_{BC} = 0 V of 240 / 270 GHz f_T / f_{max} FSA Si/SiGeC HBT arrays (3024×0.13×0.5 µm²). V_{BE} scale (lin) is from 0 to 0.9V, I_C and I_B scale (log) is from 1pA to 100mA. '+' indicates structure position in the die and notch is at bottom.

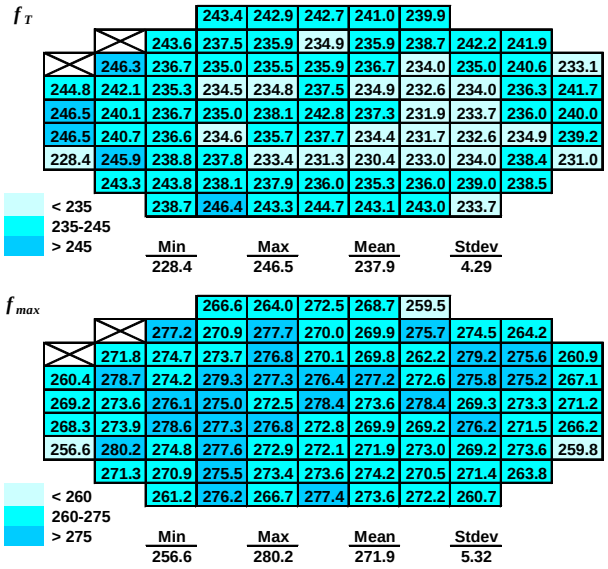

Fig. 6. f_T and f_{max} mappings [GHz] of a 240/270 GHz f_T / f_{max} 0.13 × 3.6 µm² FSA HBT at V_{CB} = 0.5 V and V_{BE} = 0.92 V.

We have verified, using a bipolar-only technology integrating the main BiCMOS integration constraints, that circuits' specifications could indeed be met with these improved HBT performances. A frequency divider having a self-oscillation frequency of 77 GHz (highest reported to date in any SiGe HBT/BiCMOS technology) and dividing correctly up to at least 100 GHz has been demonstrated with a power consumption of only 122 mW [7]. The divider was tested over temperature and found to divide up to 97 GHz at 50°C and up to 91 GHz at 100°C (Fig. 7). A 105-GHz VCO with a phase noise of -101.3 dBc/Hz at 1 MHz offset has been fabricated too [8]. It delivers +2.7 dBm of differential output power at 25ºC, with operation up to 125ºC. The measured spectrum of this record performance VCO is given in Fig. 8.

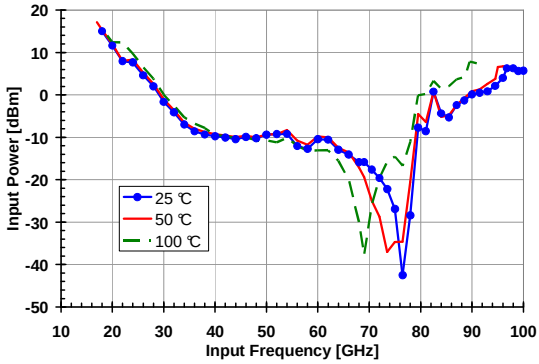

Fig. 7. Sensitivity curves across temperature for a 100 GHz divider fabricated in FSA Si/SiGeC HBT technology [7].

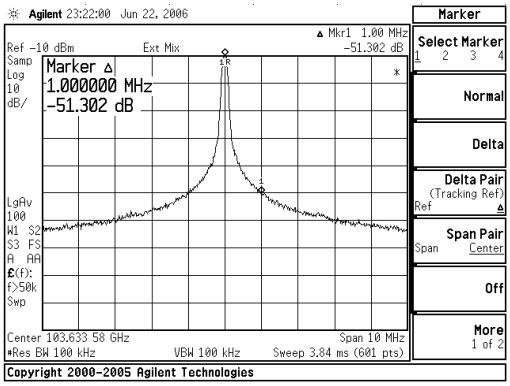

Fig. 8. Averaged spectral plot of phase noise (phase noise is -101.3 dBc/Hz at 1 MHz offset) of 105-GHz VCO in FSA Si/SiGeC HBT technology [8].

The second limitation of BiCMOS9 is the back-end of line (BEOL). Indeed, all the previous results were obtained with a 6-copper metal layers digital CMOS BEOL, featuring 50-Ω microstrip (MS) transmission lines (TL) with a poor attenuation constant α of 1.2 dB/mm at 80 GHz. BiCMOS9MW, whose development is under way, removes these two limitations since it embeds a 230-GHz f_T / 280-GHz f_{max} HBT together with a BEOL dedicated to millimeter-wave applications, featuring α = 0.5 dB/mm at 80 GHz (cf. Fig. 9 and Table I).

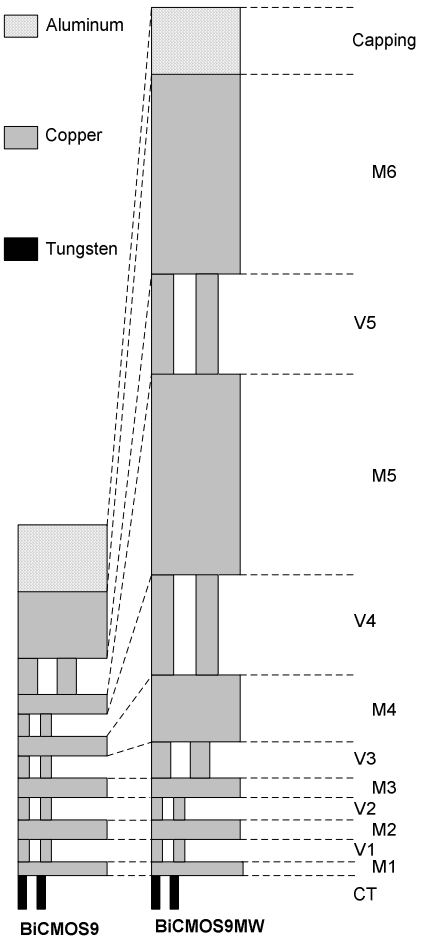

Fig. 9. Schematic comparison of the BEOL cross-sections of BiCMOS9 and BiCMOS9MW technologies (both feature 6 copper metal layers but with twofold height difference).

III. End-of-Roadmap Challenges

A. The BiCMOS roadmap

BiCMOS roadmap does not follow Moore's law, whose driver is the shrink of digital functions. The move from one CMOS node to the next can be motivated by the increase of gate density. Then, HBT performance may remain unchanged if operation frequency of the targeted application does not change (e.g. cellular phone transceivers). This roadmap is likely to end with the dramatic increase of HF performances of advanced CMOS technologies.

On the contrary, high-speed BiCMOS roadmap is driven by, on one hand the increase of the optical communications data rate, and on the other hand the emergence of applications towards higher frequencies. The result of this is a step-by-step roadmap aiming at the best combination between CMOS density and HBT performance. This roadmap will go on as long as Si/SiGeC HBT performances can be pushed forward (with significant advantages over CMOS) and applications to ever increasing frequencies carry on.

Advanced developments are in progress to further improve device characteristics, always having the BiCMOS integration as a target. Since HBT performance is not directly linked to a CMOS node, the improvement can be made inside a node (cf. BiCMOS9 / BiCMOS9MW) or from one node to another. Nevertheless, FEOL (front-end of line) and BEOL processing, overall thermal budget, and available design rules have an impact on the HBT performance through the vertical profile and/or the lateral dimensions. f_T is indeed mainly determined by the vertical profile while lateral dimensions have considerable impact on f_{max}, NF_{min} and power consumption.

B. From 120 nm to 65 nm…and 45 nm to the end of the roadmap

From the current 120-nm node to the next 90-nm and 65-nm nodes, the main limitations are first, the final anneal performed for CMOS junctions activation (~1100°C: only ~30°C reduction in 65 nm compared to 120 nm and 90 nm) and second, the BEOL design rules that are not in favor of the high current densities needed by the HBT. It is indeed important to notice that raising the collector doping to delay the onset of the Kirk effect, which is an efficient way to improve f_T, leads to an increase of the collector current density at peak f_T (cf. Fig. 10). The limits of our present bipolar architecture, with the integration scheme in use (HBT between polygate deposition and final anneal), is probably close to 300-GHz f_T for a CMOS spike anneal of ~1100°C: 280-GHz f_T and 300-GHz f_{max} has indeed been achieved while the extracted intrinsic cut-off frequencies of this device are 380-GHz f_T and 350-GHz f_{max} (cf. Fig. 11). Cryogenic measurements have shown that this architecture can potentially reach higher performances (at room temperature, with a different integration scheme) since ~ 400-GHz f_T and 440-GHz f_{max} have been measured at 50 K (cf. Fig. 12). This is the highest f_{max} ever reported for a SiGe:C HBT since the device reported in [12] features a relatively low f_{max} that does not increase significantly at low temperature. Circuit results have indeed shown that f_{max} must not be sacrificed for f_T [7]. Architecture changes are currently being investigated to approach cryogenic performances at room temperature, without changing the integration scheme and keeping the 1100°C spike anneal.

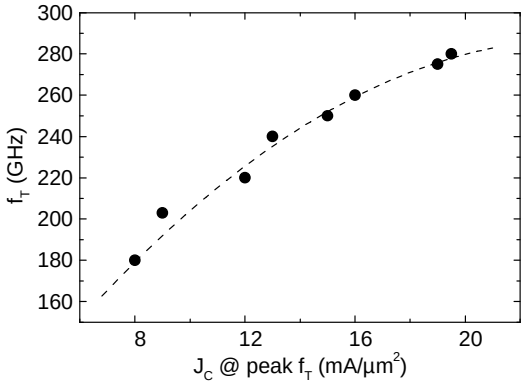

Fig. 10. Evolution trend of the current gain cut-off frequency f_T with the collector current density J_C.

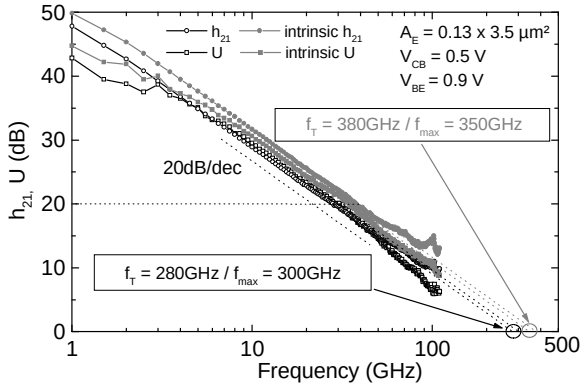

Fig. 11. HF gains vs. frequency characteristics of a 280-GHz f_T – 300-GHz f_{max} HBT. Intrinsic device, extracted by removing extrinsic components, features 380-GHz f_T and 350-GHz f_{max}.

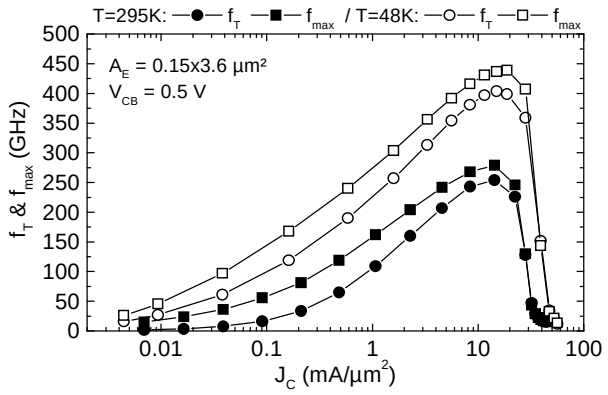

Fig. 12. f_T & f_{max} vs. J_C curves of a Si/SiGeC HBT at 295 K and 48 K. Peak f_T and f_{max} increase from 250 GHz / 280 GHz at 295 K to 400 GHz / 440 GHz at 48 K.

From the 45-nm CMOS node to the end of the roadmap, the situation is reversed for the thermal budget since spike annealing is replaced by laser annealing, which allows dopant activation with nearly no diffusion. This is favorable for realizing narrow neutral base widths but calls for the development of new materials for the extrinsic base and for the emitter: For example, arsenic has to be replaced by phosphorus for the in-situ doping of the polyemitter. A TEM cross-section of a first device using a boron in-situ doped polybase, a phosphorus-doped emitter and nickel silicide is shown in Fig. 13. Beyond 45 nm, the use of very thin SOI substrates that could belong to the mainstream CMOS will exacerbate the BiCMOS integration challenge [13].

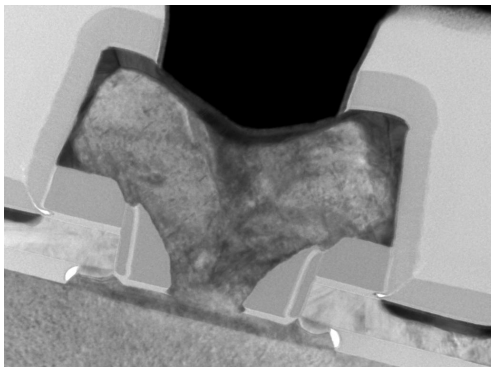

Fig. 13. TEM cross-section of a FSA Si/SiGeC HBT (W_E ~ 100nm) with boron in-situ doped polybase, phosphorus doped emitter and nickel silicide.

C. Levering up the HBT limits

Raising the transistor speed requests the increase of both the doping level of the neutral regions of the HBT and the abruptness of the junctions, which are conflicting targets. Tunneling currents may appear [11] due to this scaling and, more classically, BV_{CEO} decreases for increasing f_T. Therefore, the main hurdle to maintaining a significant advantage over CMOS is to break up the classical trade-off between BV_{CEO} and f_T. A significant improvement has been achieved in the past years with the introduction of carbon in the base to reduce boron diffusion.

Solutions currently investigated to increase BV_{CEO} without affecting f_T focus on the increase on the base current [14]-[15]-[16]. Results of recent investigations, summarized in Fig. 14, have shown an encouraging progress of more than 50 GHz.V of the $f_T \times BV_{CEO}$ product by increasing the base current through base [15] or through emitter [16] engineering. This last solution, relying on a 'metallic' emitter transistor, can be obtained in a robust way by using an original process of poly replacement through contact holes (Fig. 15).

Nevertheless, high-power / high-frequency circuits should still require III-V technologies, in which breakdown voltages benefit from larger bandgap materials.

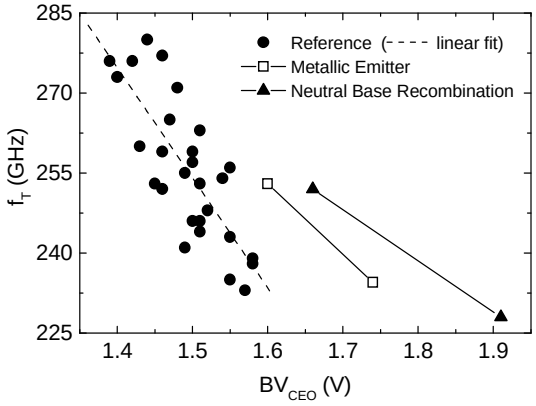

Fig. 14. f_T – BV_{CEO} chart of different high-speed Si/SiGeC HBTs: 'metallic emitter' and 'neutral base recombination' HBTs are compared to more standard devices (reference).

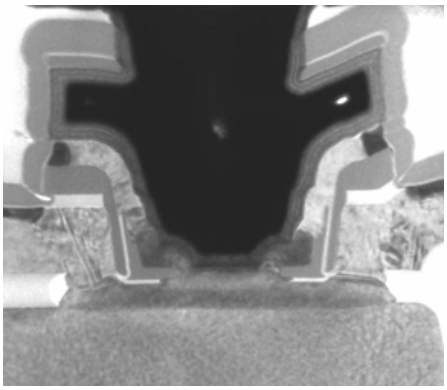

Fig. 15. TEM cross-section of a FSA Si/SiGeC HBT (W_E ~ 150nm) featuring a 'metallic emitter' obtained with a 'Poly REplacement Through Contact Holes' process.

IV. Conclusion

First 120-nm SiGe BiCMOS platform from STMicroelectronics is released for production. This technology addresses applications up to 40 Gb/s – 40 GHz. Next BiCMOS platform will be able to cover applications up to 100 GHz. Efforts are underway to further increase SiGe HBT performances in spite of the constraints placed by the BiCMOS integration: no brick wall has been identified for the integration of high-speed HBTs in advanced CMOS nodes already defined. Nevertheless, the high-speed BiCMOS roadmap is not yet frozen since it depends on applications for which products are only in an advanced R&D phase.

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References

[1] P. Chevalier et al., "Advanced SiGe BiCMOS and CMOS platforms for Optical and Millimeter-Wave Integrated Circuits", in CSICS Tech. Dig., 2006, in press.
[2] M. Laurens et al., "A 150GHz fT / fmax 0.13µm SiGe:C BiCMOS technology", in Proc. BCTM, 2003, pp 199-202.
[3] T.O. Dickson et al., "The Invariance of Characteristic Current Densities in Nanoscale MOSFETs and its Impact on Algorithmic Design Methodologies and Design Porting of Si(Ge) (Bi)CMOS High-Speed Building Blocks", IEEE J. Solid-State Circuits, vol. 41, no. 8, August 2006, pp. 1830-1845.
[4] T.O. Dickson et al., "An 80-Gb/s 2^31 -1 Pseudo-Random Binary Sequence Generator in SiGe BiCMOS Technology", IEEE J. Solid-State Circuits, vol. 40, no.12, Dec. 2005, pp. 2735-2745.
[5] T.O. Dickson and S.P. Voinigescu, "Low-Power Circuits for a 2.5-V, 10.7-to-86 Gb/s Serial Transmitter in 130nm SiGe BiCMOS", in CSICS Tech. Dig., 2006, in press.
[6] S. Pruvost et al., "A Compact Low Noise Amplifier in SiGe:C BiCMOS Technology for 40GHz Wireless Communications", in RFIC Symp. Dig., 2005, pp. 565-568.
[7] E. Laskin et al., "Low-Power, Low-Phase Noise SiGe HBT Static Frequency Divider Topologies up to 100 GHz", in Proc. BCTM, 2006, pp.xxxx.
[8] S.T. Nicolson et al., "Design and Scaling of SiGe BiCMOS VCOs Operating Near 100GHz", in Proc. BCTM, 2006, pp.xxxx.
[9] P. Chevalier et al., "230 GHz Self-Aligned SiGeC HBT for Optical and Millimeter-Wave Applications", IEEE J. Solid-State Circuits, vol. 40, no. 10, Oct. 2005, pp. 2025-2034.
[10] P. Chevalier et al., "300 GHz fmax self-aligned SiGeC HBT optimized towards CMOS compatibility", in Proc. BCTM, 2005, pp. 120-123.
[11] D. Lagarde et al., "Band-to-band Tunneling in Vertically Scaled SiGe:C HBTs", IEEE Electron Dev. Lett., vol. 27, no. 4, April 2006, pp. 275-277.
[12] R. Krithivasan et al., "Half-Terahertz Operation of SiGe HBTs", IEEE Electron Device Letters, vol. 27, no. 7, July 2006, pp. 567-569.
[13] P. Chevalier et al., "Low-Cost Self-Aligned SiGeC HBT Module for High-Performance Bulk and SOI RFCMOS Platforms", in IEDM Tech. Dig., 2005, pp. 983-986.
[14] B. Martinet et al., "An investigation of the static and dynamic characteristics of high speed SiGe:C HBTs using a poly-SiGe emitter", in Proc. BCTM, 2002, pp. 147-150.
[15] B. Barbalat et al., "Carbon effect on neutral base recombination in high-speed SiGeC HBTs", in Proc. ISTDM, 2006, pp. 238-239.
[16] B. Barbalat et al., "Experimental Study of Metallic Emitter SiGeC HBTs", in Proc. BCTM, 2006, pp.xxxx.