A Comparison of Si CMOS, SiGe BiCMOS, and InP HBT Technologies for High-Speed and Millimeter-Wave ICs

S. P. Voinigescu[1], T. O. Dickson[1], R. Beerkens[2], I. Khalid[2], and P. Westergaard[1]

1) Edward S. Rogers Dept. of Electrical & Computer Engineering, University of Toronto, 10 King's College Rd. Toronto, ON, M5S 3G4, Canada

2) STMicroelectronics, Ottawa, ON, Canada.

***Abstract* — This paper presents an overview of Si MOSFET, SiGe HBT, and InP HBT device and circuit performance for broadband and tuned millimeter-wave applications. Implementations of CMOS-only, SiGe-HBT-only, SiGe BiCMOS, and InP-HBT 30-80 Gb/s high-speed circuit in production 130-nm SiGe BiCMOS and InP HBT technologies are compared.**

***Index Terms* — Heterojunction bipolar transistor, silicon-germanium, indium-phosphide, CMOS, BiCMOS, CM, low-noise amplifiers.**

I. Introduction

As illustrated in Fig.1, production 90-nm CMOS, 130-nm SiGe BiCMOS, and 1-μm InP HBT technologies from multiple foundries have demonstrated simultaneous f_T and f_{MAX} values exceeding 150 GHz. At the same time, advanced SiGe and InP HBTs with cutoff frequencies of 350 GHz and 450 GHz, respectively, are being developed by several groups. Not surprisingly, the last year has brought about a significant increase in the number of publications addressing millimeter-wave (mm-wave) and high-speed digital ICs with data rates exceeding 40 Gb/s [1]-[6]. Interest in mm-wave circuits has been kindled by the potentially large automotive radar market (60 million cars were produced world-wide in 2002) and by the newly licensed 70-GHz band for wireless gigabit Ethernet. In each case, volumes are predicted to reach $1.5B in 5 years [7]. This paper presents an overview of Si MOSFET, SiGe HBT, and InP HBT devices. Their performance in broadband and tuned mm-wave circuits implemented in production 130-nm SiGe BICMOS [8] and InP HBT [9] technologies is compared.

II. Transistor Performance Comparison

A. f_T, f_{MAX}

The I_{DS}-V_{GS} characteristics of very deep submicron MOSFETs biased in saturation exhibit two distinct regions. At low effective gate voltages ($V_{eff} = V_{GS} - V_T$) the well-known, long-channel square law applies. At larger gate voltage, the characteristics become linear. The boundary between the two regions corresponds roughly to the V_{eff} at which f_T and f_{MAX} reach their peak values. For example, in 130-nm n-MOSFETs [10], for V_{eff} lower than 0.2 V, the experimental behaviour is accurately captured by simple expressions that describe the linear increase in g_m, f_T, and f_{MAX} with V_{GS}, as well as their dependence on device geometry (N_f, W_f) and on the series resistances R_s, R_g, R_d and the channel resistance R_i. Beyond V_{eff} = 0.4 V, g_m, f_T and f_{MAX} become almost independent of gate voltage, underscoring the linearity of MOSFETs when biased at or beyond peak f_T.

$$2\pi f_T \approx \frac{N_f C_{OX} \mu_n \frac{W_f}{l_G}(V_{GS}-V_T)}{\frac{2}{3}C_{ox}N_f W_f l_G + (C_{GDO}+C_{GSO})N_f W_f + C_{GBO} N_f l_G} \quad (1)$$

$$f_{MAX} \approx \frac{f_T}{2\sqrt{\frac{R_{gsq} W_f^2}{12(3) l_G}(g'_{ds}+2\pi f_T C'_{gd}) + g'_{ds}(R'_i + R'_s)}} \quad (2)$$

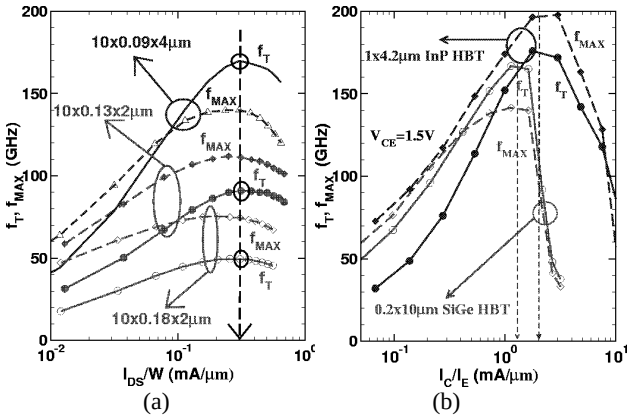

Fig.1 Measured f_T and f_{MAX} as a function of drain/collector current for a) 180-nm, 130-nm, and 90-nm n-MOSFETs, and b) for SiGe and InP HBTs [12].

C'_{gd}, g'_{ds}, R'_i, R'_s indicate unit gate width parameters. As the minimum feature size of MOSFETs reaches 100 nm, the gate-source and gate-drain overlap and fringing capacitances (C_{GSO}, C_{GDO}, C_{GBO}) become comparable to the

internal gate capacitance and contribute significantly to performance degradation in digital and RF circuits. Shrinking the unit gate finger width W_f below 1 μm and/or contacting the gate on both sides does little to improve f_{MAX} and noise figure while severely reducing f_T [10].

As a result of the constant-field scaling rules being applied to every new CMOS generation since the 0.5-μm technology node, V_{eff} at peak f_T scales with the technology node and is therefore more difficult to predict and use in analytical circuit design. However, the drain current per total device width at which the peak f_T and f_{MAX} of Si n-MOSFETs occurs is 0.25 to 0.3 mA/μm, independent of technology node, as shown in Fig.1a. In p-MOSFETs, the corresponding value is 0.125 to 0.15 mA/μm. This fundamental property of MOSFETs can be applied to simplify CMOS CML-logic and mm-wave circuit design using current-centric rather than V_{eff} bias techniques. This approach is similar to the one used in bipolar circuits which rely on peak f_T bias. For comparison, in SiGe and InP HBTs the peak f_T/f_{MAX} current density per emitter length is 1.2 mA/μm and 2mA/μm, respectively, Fig. 1b. Given the comparable f_T and f_{MAX} of production CMOS, SiGe BiCMOS, and 1-μm InP HBT technologies, the differences in their circuit behaviour can be explained by transconductance, gate/base resistance, and slew rate.

B. Noise and narrow-band noise matching sensitivity

As in the case of f_{MAX}, due to the increase of the gate resistance with W_f, the MOSFET minimum noise factor F_{MIN} is a strong function of gate geometry. Layout, therefore, becomes an important differentiator between the performance of LNAs implemented in the same CMOS technology node by different designers, even when similar circuit topologies are employed.

$$F_{MIN(MOS)} \approx 1 + 2k_1\frac{f}{f_T}\sqrt{g_m' R_s' + \frac{g_m' R_{gsq} W_f^2}{12(3) l_G} + k_2(1+\omega^2 R_i^2 C_{gs}^2)} \quad (3)$$

In contrast, the F_{MIN} of HBTs is only weakly dependent on emitter length, making LNA design far more predictable across foundries and designers. In both SiGe and InP HBTs, the optimal F_{MIN} bias current is frequency-dependent and considerably lower than the maximum-gain bias, leading to a trade-off between noise and gain, Fig. 2.

$$F_{MIN(HBT)} \approx 1 + \frac{1}{\beta} + \frac{f}{f_T}\sqrt{\frac{I_C}{2V_T}(R_E + R_b)\left(1 + \frac{f_T^2}{\beta f^2}\right) + \frac{f_T^2}{4\beta f^2}} \quad (4)$$

At low current densities the bias dependence of $F_{MIN(HBT)}$ is determined by the base resistance variation with bias current. In this respect, InP and SiGe HBTs exhibit quite different behaviour. InP HBTs, with very high doping levels in the base, exceeding 10^{20} cm^{-3}, have practically constant base resistance which leads to a continuous decrease in F_{MIN} as the bias current is reduced. In SiGe HBTs, due to the lower base doping, the internal base resistance decreases with increasing bias current, leading to $F_{MIN}(I_C)$ characteristics that exhibit a minimum when the base resistance thermal noise equals the collector shot noise. In contrast, in n-MOSFETs, the optimum F_{MIN} bias, approximately 0.13 mA/μm, is close to the maximum gain bias and occurs at the same current density, irrespective of frequency and of the technology node. This is a consequence of the fact that, when MOSFETs are biased in the saturation region, f_T, f_{MAX}, and F_{MIN} are strongly dependent on the $g_m(V_{GS})$ and $g_m(V_{DS})$ characteristics. F_{MIN} reaches a minimum when $g_m(V_{GS})$ peaks.

$$F_{MIN(MOS)} \approx 1 + \text{Const}\frac{f}{\sqrt{g_m}} \approx 1 + \text{Const}\frac{f}{\sqrt{V_{GS} - V_T}} \quad (5)$$

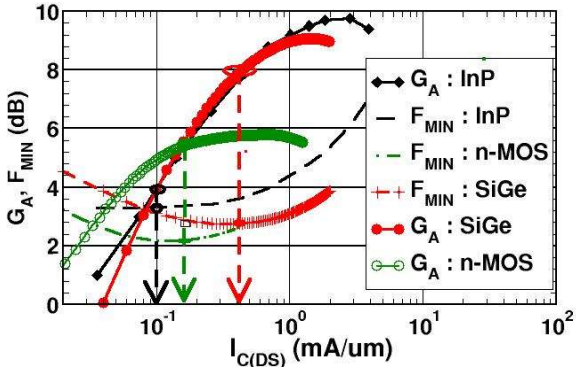

Fig. 2 F_{MIN} and associated gain as a function of bias current at 36 GHz for 130-nm n-MOSFETs, SiGe and InP HBTs.

Si MOSFETs benefit from the lower transconductance and capacitance per unit gate width and from the layout dependence of gate resitance to achieve lower noise figures than those of SiGe and InP HBTs of comparable or higher f_T and f_{MAX}. However, these benefits are seldom achieved in practical implementations of tuned circuits at microwave and mm-wave frequencies. The very high noise resistance R_n, low optimum noise admittance Y_{sopt}, and high quality factor of the MOSFET input and noise impedances, in concert with the strong layout dependence, make CMOS circuits considerably more sensitive than HBT ones to process variations, impedance mismatch, and model inaccuracy.

$$R_{n(MOS)} \approx \frac{P}{g_m} + (R_s + R_g); \quad R_{n(HBT)} \approx \frac{1}{2g_m} + (R_E + R_b) \quad (6)$$

$$Y_{sopt(MOS)} \approx \frac{f}{f_T R_n}\left[\sqrt{P g_m (R_s + R_g)} - jP\right] \text{ where } P > \frac{2}{3} \quad (7)$$

$$Y_{sopt(HBT)} \approx \frac{f}{f_T R_n}\left[\sqrt{\frac{g_m}{2}(R_E+R_b)} - j\frac{1}{2}\right] \quad (8)$$

C. High-speed digital performance metrics

The open-circuit time constant (OCTC) of a chain of differential MOS-CML inverters and of a HBT-CML inverter chain with a stage-to-stage loading factor of k can provide a useful metric of the ultimate digital speed of these technologies.

$$\tau_{MOS} \approx \Delta V \frac{C_{gd}+C_{db}}{I_T} + \left(k+\frac{R_g}{R_L}\right)\Delta V \frac{C_{gs}+(1-A_V)C_{gd}}{I_T} \quad (9)$$

$$\tau_{HBT} \approx \Delta V \frac{C_{\mu}+C_{cs}}{I_T} + \left(k+\frac{R_b}{R_L}\right)\Delta V \frac{C_{\pi}+(1-A_V)C_{\mu}}{I_T} \quad (10)$$

A_V is the small signal voltage gain of the input transistor, typically -2 for MOS, and -1 for cascode HBT inverters, respectively, I_T is the tail current, R_L is the load resistance, and ΔV is the logic swing. The first term in the OCTC equations represents the voltage swing divided by the intrinsic slew rate of the device. The latter is larger in HBTs than in MOSFETs. For highest digital speed, the tail current of the MOS-CML inverter corresponds to the peak f_T bias (i.e. each transistor in the differential pair is biased at 0.15 mA/μm). This allows full switching with a voltage swing of 450 mVp-p and 300 mVp-p in 130-nm and 90-nm CMOS, respectively. The HBT CML inverters have 250 mVp-p swing and are biased at a tail current 1.5 times the peak f_T current density.

It has been recognized recently that the base resistance term is the major roadblock limiting the switching speed of SiGe HBT logic in the 120-GHz and 200-GHz SiGe HBT generations [13]. In MOS-CML, the gate resistance term can be rendered negligible through layout techniques by reducing the unit finger width. Based on the previous analysis, a novel BiCMOS-CML logic family has recently been proposed that employs a cascode stage consisting of a MOSFET common-source device followed by a common-base HBT [11]. Such a structure takes advantage of the large intrinsic slew rate of the HBT and of the small gate resistance of the MOSFET, resulting in faster switching speed than either MOS or HBT CML families. At the same time, as a result of the low MOSFET threshold voltage and superior f_T at low V_{DS} (Fig. 3) it operates with lower (less than 2.5 V) supply voltages than SiGe HBT ECL and CML logic.

$$\tau_{BiCMOS} \approx \Delta V \frac{C_{\mu}+C_{cs}}{I_T} + \left(k+\frac{R_g}{R_L}\right)\Delta V \frac{C_{gs}+C_{gd}}{I_T} \quad (11)$$

III. Circuit Performance Comparison

By taking advantage of the fine-line, multi-level copper back-end of Si CMOS and SiGe BiCMOS technologies [8,12], designers can compensate for the higher silicon substrate loss to achieve similar transmission line [12] and inductor performance to that obtained on InP semi-insulating substrates [14]. Fig.4 compares measured data for 150-pH inductors fabricated on Si and InP substrates. Q factors reaching 15 at 50 GHz, and self-resonant-frequencies beyond 100 GHz are predicted in both cases. The stripe width is 2 μm and 5 μm, for the Si and InP inductors respectively, resulting in a 75% smaller footprint for the silicon implementation.

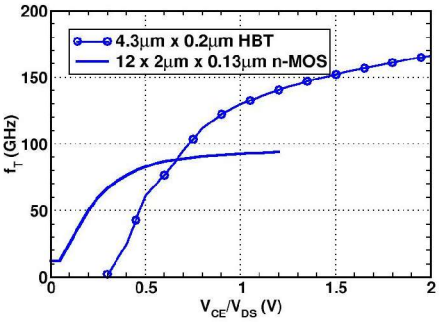

Fig. 3 Drain/collector voltage dependence of f_T in 130-nm n-MOSFETs and SiGe HBTs.

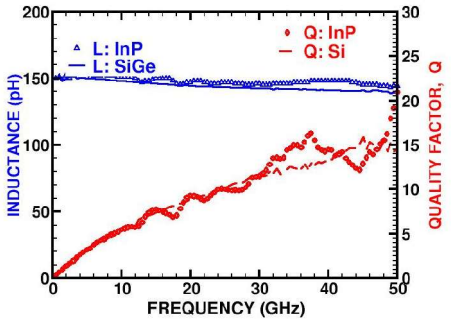

Fig. 4 Measured L and Q of Si and InP inductors.

InP HBT [9] and SiGe HBT broadband transimpedance amplifiers were designed using an algorithmic methodology to ensure that the minimum noise figure is achieved over the 3dB-bandwidth of the amplifier. Their 50-Ω noise figures, shown in Fig.5a, were measured on-wafer up to 20 GHz and compared to that of a broadband CMOS amplifier [15] fabricated in the same 130-nm SiGe BiCMOS technology [8]. The noise of the InP and SiGe amplifiers is comparable in the 15-GHz to 20-GHz range. Below 15 GHz, the SiGe HBT amplifier has a single-ended noise figure of 9.5 dB, 1.5 dB lower than that of the InP amplifier, and 7 dB better than that of the CMOS

amplifier with resistively-matched inverter input stage. Large signal eye diagrams for all three circuits are shown in Figs. 5b, 5c, and 5d. The 130-nm CMOS amplifier operates from a 1.5-V supply with 300-mVp-p output swing per side. Its sensitivity is 10 mVp-p per side at 20 Gb/s and 100 mVp-p per side at 30 Gb/s. The InP amplifier operates from a 3.3-V supply and has a sensitivity of 8 mVp-p at 43 Gb/s [9] while the SiGe amplifier demonstrated an eye *Q* of 7 with a 2^{31}-1 PRBS at 43 Gb/s for a single-ended 20 mVp-p input. The SiGe HBT circuit was operational with a supply voltage down to 1.9 V. The eye diagrams of an 80-Gb/s 2:1 MUX, implemented in a 150-GHz SiGe BiCMOS process [8] using the proposed BiCMOS logic, are shown in Fig. 6.

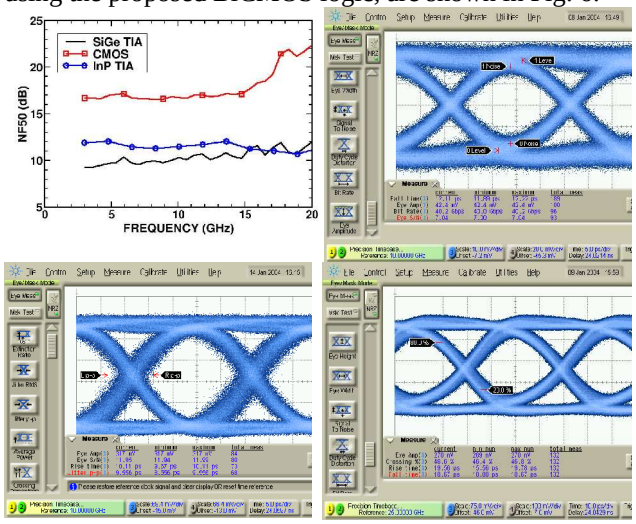

Fig. 5: a) (top left) Noise figure and eye diagrams of b)(top right) SiGe HBT comparator at 40Gb/s, c) InP comparator at 40 Gb/s (bottom left), and d) CMOS at 30 Gb/s (bottom right).

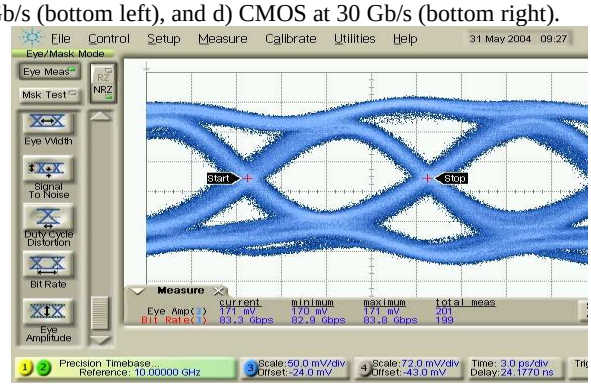

Fig.6: 80-Gb/s output eye of SiGe BiCMOS 2:1 MUX.

VI. Conclusion

Experimental device and circuit data, and simple analytical expressions of the main high-frequency FOMs of SiGe and InP HBTs have proved that, at comparable f_T and f_{MAX}, there is very little difference in their performance in narrow-band mm-wave and in broadband and high-speed digital circuits. For the first time, starting with the 130-nm SiGe BiCMOS technology node, designers can take advantage of the comparable n-MOSFET and SiGe HBT speed to combine the two devices on the high-frequency signal path in truly BiCMOS topologies and thus realize low-voltage and low-power mm-wave ICs in the 30-GHz to 80-GHz range.

Acknowledgement

We thank A. Mangan and M. LaCroix, D. Gloria, S. Boret, and B. Prokes of STMicroelectronics for their contributions and are indebted to H. Tran and M. Tazlauanu of Quake Technologies for InP TIA data. This work was supported by Micronet, NSERC, CFI, STMicroelectronics, and Gennum Corporation.

References

[1] M. Meghelli, "A 108Gb/s 4:1 Multiplexer in 0.13 µm SiGe-Bipolar Technology," *ISSCC Digest*, pp.236-237, 2004.

[2] Y. Suzuki et al., "110 Gb/s Multiplexing and Demultiplexing ICs," *ISSCC Digest*, pp.232-233, 2004.

[3] D. Yamazaki et al., "A 25GHz Clock Buffer and a 50Gb/s 2:1 Selector in 90nm CMOS," *ISSCC Digest*, pp.240, 2004.

[4] S. Reynolds et al., "60GHz Transceiver Circuits in SiGe Bipolar Technology," I*SSCC Digest*, pp.442-443, 2004.

[5] H. Li et al., "Design of W-Band VCOs with High Output Power for Potential Applications in 77 GHz Automotive Radar Systems," *IEEE GaAs IC Symp.*, pp.263, Nov. 2003.

[6] Y. Baeyens and Y.K. Chen, "A monolithic integrated 150 GHz SiGe HBT push-push VCO with simultaneous differential V-band output," *Proc.IEEE MTT-S* pp.877, 2003

[7] Emerging 60 and 70-90 GHz "GigaBit Wireless" Communications,"http://www.iwpc.org/Workshop_Folders/GigaBitWireless/GigaBitWirelessAgenda.htm

[8] M. Laurens et al., "A 150 GHz f_T/f_{MAX} 0.13 µm SiGe:C BiCMOS technology," *Proc. IEEE BCTM*, Sept. 2003.

[9] H. Tran et al., "6-kΩ, 43-Gb/s Differential Transimpedance-Limiting Amplifier with Auto-Zero Feedback and High Dynamic Range," *IEEE GaAs IC Symp.*, pp.241, Nov. 2003.

[10] S.P. Voinigescu et al., "Direct Extraction Methodology for Geometry-Scalable RF-CMOS Models", *Proc.IEEE ICMTS*, pp.235-240, March 2004.

[11] T.O. Dickson et al., "A 2.5-V, 40-Gb/s Decision Circuit Using SiGe BiCMOS Logic," *VLSI Symposium*, June 2004.

[12] S.P. Voinigescu, et al., "A Comparison of Silicon and III-V Technology Performance and Building Block Implementations for 10 and 40 Gb/s Optical Networking ICs," *IJHSES*, Vol.13, No.1, paper 2, March, 2003

[13] G. Freeman et al. "Transistor Design and Application Considerations for >200 GHz SiGe HBTs," *IEEE Trans ED*, Vol.50, No.3, pp.645-655, 2003.

[14] T.O. Dickson et al., "Si-based Inductors and Transformers for 30-100 GHz Applications", *IMS*, June 2004.

[15] P.Westergaard et al., "A 1.5V, 20/30 Gb/s CMOS Backplane Driver with Digital Pre-emphasis," *CICC*, 2004.