A 49-Gb/s, 7-Tap Transversal Filter in 0.18 µm SiGe BiCMOS for Backplane Equalization

Altan Hazneci and Sorin P. Voinigescu
Edward S. Rogers, Sr. Department of Electrical & Computer Engineering, University of Toronto
10 King's College Rd., Toronto, Ontario, M5S 3G4, Canada
e-mail: hazneci@eecg.toronto.edu, sorinv@eecg.toronto.edu

***Abstract*—This paper describes the first integrated transversal filter for feed-forward equalizers (FFE) operating above 40 Gb/s. Equalization of a 2^{31}–1 PRBS over a 9-ft and 6.5-ft cable with SMA connectors is demonstrated on-wafer at 40 Gb/s and 49 Gb/s respectively. The circuit is implemented in a commercial 0.18 µm SiGe BiCMOS process and is based on a differential distributed 7-tap fractionally spaced transversal filter topology. Microstrip transmission lines are employed as delay elements. With input and output return loss better than –10 dB up to 55 GHz, and a 1 x 2 mm^2 die area, the circuit draws 150 mA from a single 5-V supply.**

Keywords-Equalizer, 40 Gb/s, SiGe BiCMOS, Gilbert cell, microstrip

I. INTRODUCTION

The frequency dependent losses in the backplane and dispersion in optical fiber channels pose a major problem in broadband communication systems exceeding 10 Gb/s data rates. This non ideal frequency response causes intersymbol interference (ISI) and significantly shortens the distance over which data can be reliably transmitted. To send data over longer distances, various techniques exist to compensate for these losses in order to flatten the overall frequency response of the channel. One such approach is to use a transversal filter to equalize the received signal [1]. Recently, integrated 10-Gb/s equalizers for multimode fiber links [2-3] and backplanes [4-5] have been demonstrated using this approach. In addition, an InP-HBT 40-Gb/s equalizer for optical fiber links was demonstrated in [6] based on a 3-tap transversal architecture.

Printed circuit boards (PCBs) for backplane applications present demanding design challenges for frequencies approaching 20 GHz (40 Gb/s) and above. At these frequencies the skin effect and dielectric losses dominate. These two effects combine to significantly attenuate the signal content at higher frequencies giving rise to severe ISI. Another area of concern, which receives perhaps less attention, is communication between backplanes. Inter-cabinet cabling is not immune to these effects either and presents similar challenges. Fig. 1.a shows the measured attenuation for a 20-cm long, 50-Ohm controlled impedance trace on FR4 substrate and a 9-ft cable with SMA connectors. At 20 GHz the trace loss is approximately 30 dB whereas the cable loss is approximately 15 dB. Moving to even higher frequencies, at 50 GHz, the FR4 trace loss is greater than 50 dB and presents a formidable if not impossible task of equalizing the signal.

The preceding discussion highlights the fact that microwave PCBs require substrate materials which exhibit very low loss. As the measured data in Fig. 1.b indicate, with the new generation of organic substrates, it is possible to achieve attenuation levels lower than 0.75 dB/cm at 20 GHz and less than 1.7 dB/cm at 50 GHz. Such results point to the feasibility of chip-to-chip communication over 30-cm of backplane at 40 Gb/s and over 12-cm long controlled-impedance lines at 100 Gb/s in conjunction with adaptive equalization. In this paper, we demonstrate the first integrated feed-forward equalizer operating above 40 Gb/s.

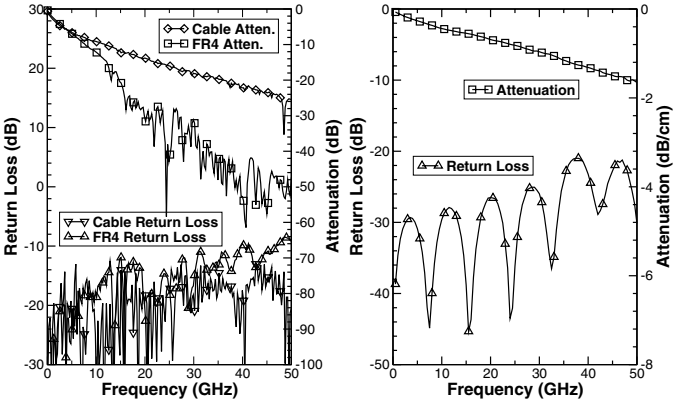

Figure 1. a) Measured attenuation and return loss of a 20-cm long 50-Ohm controlled impedance trace on FR4substrate and 9-ft section of SMA cable. b) Measured attenuation and return loss of a 1-cm long 50-Ohm microstrip line on MICROLAM substrate. (Courtesy of Stefan Szilagyi of Quake Technologies)

II. CIRCUIT DESIGN

The block diagram of the FFE is shown in Fig. 2. It consists of seven gain stages in a 7-tap transversal filter topology. The delay elements are realized using microstrip transmission lines consisting of top-metal lines over metal-2 ground planes. Each transmission line section is 500-µm long and 12-µm wide, corresponding to a 50-Ohm characteristic impedance. The input and output transmission line sections are 250-µm long. The nominal delay per section is 6.75 ps, adding up to a total adjustable delay of 48 ps. The DC level at the input and output pads can be controlled externally, allowing for versatility in testing the circuit both as an equalizer and as a distributed amplifier.

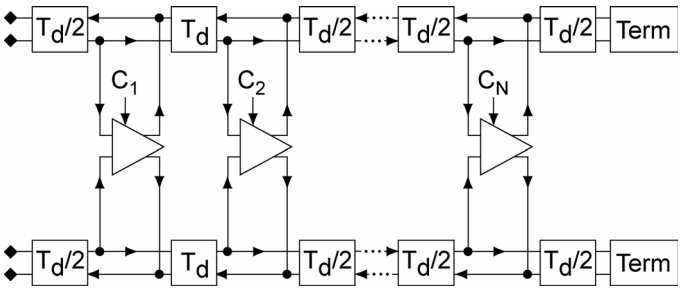

Figure 2. Block diagram of the equalizer.

The core of each gain stage is a Gilbert cell, as shown in Fig. 3, where the tail current of the differential pair controls the tap weight (GAIN pad) while the SP/N pad controls the tap sign. In order to improve the bandwidth and to reduce the loading presented to the input transmission line, the cascode differential pair is buffered by two emitter-follower stages whose tail currents are partially controlled by the GAIN pad. The latter feature ensures that the quality of the large signal eye diagrams is maintained while the tail current of the differential pair is varied in a 4:1 ratio. Resistive padding and local bias decoupling were carefully designed in order to avoid any negative resistance in the emitter-follower stages and in the cascode stage. The nominal bias current of each gain cell is 21 mA.

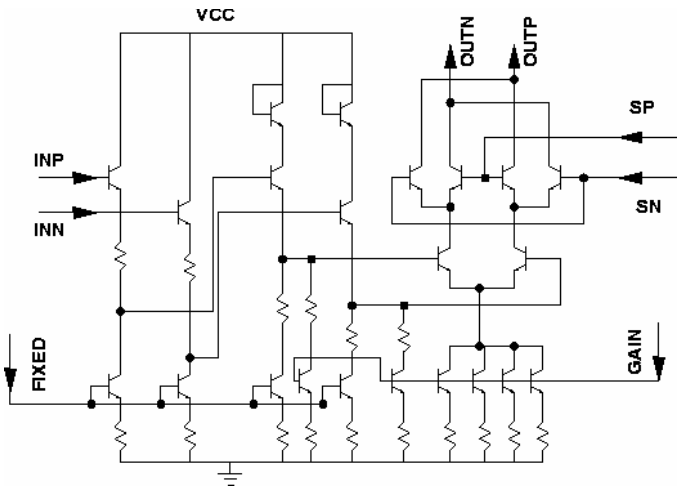

Figure 3. Gain stage schematic.

III. Fabrication And Layout

The circuit, whose layout is shown in Fig. 4, occupies an area of 1 mm x 2 mm and was fabricated in Jazz Semiconductor's SBC18, 0.18 µm SiGe BiCMOS technology featuring SiGe HBTs with f_T and f_{MAX} values of 160 GHz [7]. The differential input and output transmission lines are clearly visible in the die micrograph. The two inner and two outer transmission lines form the differential output and input paths, respectively.

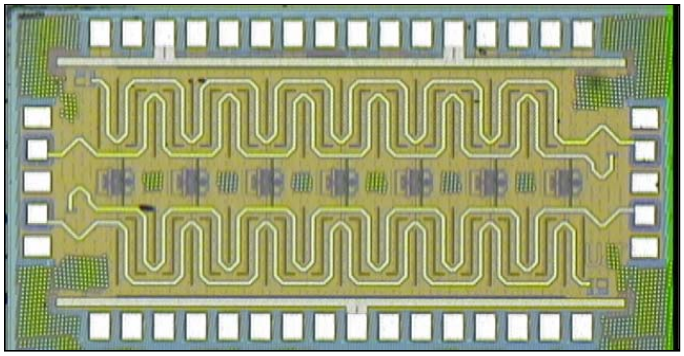

Figure 4. Equalizer layout.

The bias and control signal pads are located along the top and bottom. All the bias and control signals were routed in metal-1, and are isolated from the transmission lines via the metal-2 ground plane. The gain stages are situated along the length of the chip, between the output transmission lines. The use of multi-metal ground planes between adjacent transmission lines improves isolation and ensures that simultaneous single-ended and differential matching is maintained. Finally, to minimize the area, serpentine transmission lines were employed.

IV. Testing

The circuit was biased from a single 5-V power supply and drew 150 mA at the nominal tap settings suitable for operation as a distributed amplifier. A custom board was fabricated to provide all the various bias and control signals to set the tap signs and weights. The board was controlled via a laptop running a MATLAB GUI. S parameter measurements were carried out on the bare die up to 65 GHz using an Anritsu Network Analyzer and 65-GHz GGB probes. The measured input and output return losses, lower than −10 dB up to 55 GHz, are shown in Fig. 5.

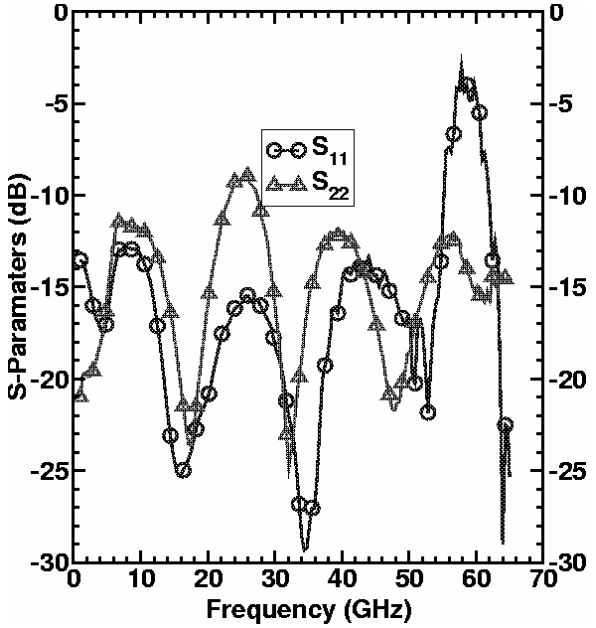

Figure 5. Measured single-ended input and output return loss.

Fig. 6 reproduces the phase response of each tap to a 10 GHz sinusoidal signal. The taps were turned on individually and the resulting waveforms were post-processed to combine the outputs from each tap. From the figure, the relative delay between each tap is approximately 6.75 ps. The total delay after the 7th tap is 48 ps.

The eye diagrams were measured on die, using an Anritsu MP1801A 43.5-Gb/s BERT and an Agilent 786100A DCA with the 86118A 70-GHz dual remote sampling head and external timebase. Operation up to 49 Gb/s (beyond the factory-specified range of the BERT) was verified by applying a 2^{31}-1 PRBS signal to the input of the equalizer through a 16-dB power attenuator and a section of SMA cable. The circuit was operated single-endedly and the unused ports were terminated off chip. Equalization was obtained by manually adjusting the gain and sign of the 7 taps through the MATLAB GUI. Figs. 7 through 10 show the measured single-ended input (after attenuator and 9-ft cable) and equalized output eye diagrams at 40, 43, 48 and 49 Gb/s, respectively. In each case, the signal level at the FFE input was approximately 200 mV_{pp} and the input eye diagram was completely closed. The output eye amplitude at 40 and 49 Gb/s was 98 mV_{pp} and 78 mV_{pp} respectively, per side. For reference the input return loss and attenuation of the 9-ft cable is given in Fig. 1a. As the data rate is ramped up from 40 to 49 Gb/s the output eye begins to close. The incremental losses become too large for the equalizer to adequately compensate. The measurement was repeated at 49 Gb/s using a 6.5-ft SMA cable (Fig. 11). The performance demonstrated over the shorter cable at 49 Gb/s is comparable to results achieved over the longer cable at 40 Gb/s. This illustrates the tradeoff between cable length and data rate in terms of the equalizer performance.

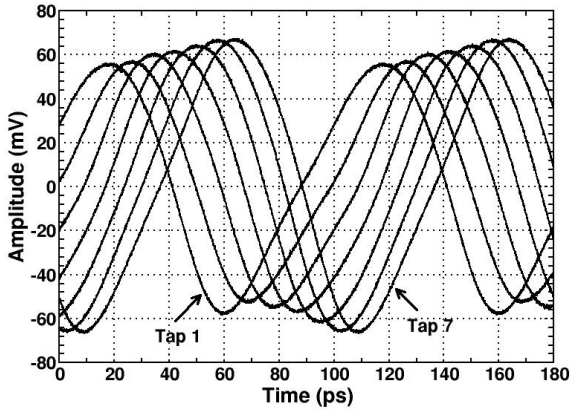

Figure 6. Measured tap delay for a 10 GHz sinusoidal input.

V. Conclusion

The design and experimental characterization of a 7-tap feed forward equalizer operating above 40 Gb/s were described. The circuit architecture is based on a transversal filter topology with on-chip microstrip transmission lines. The transmission lines were used to delay the input signal and to combine the weighted outputs of each tap. The performance was verified up to 49 Gb/s (upper data rate limit of the BERT) using a 2^{31}-1 PRBS signal over a 6.5-ft SMA cable. The FFE significantly reduces ISI and produces an open eye at the output despite having a totally closed input eye at 40 and 49 Gb/s. To the authors' best knowledge, this is the first SiGe BiCMOS FFE operating above 40 Gb/s. Together with the SiGe BiCMOS flip-flop reported in [8], it indicates that a full-fledged 40 Gb/s FFE-DFE equalizer, similar to the ones now being introduced at 10 Gb/s, is realizable in silicon.

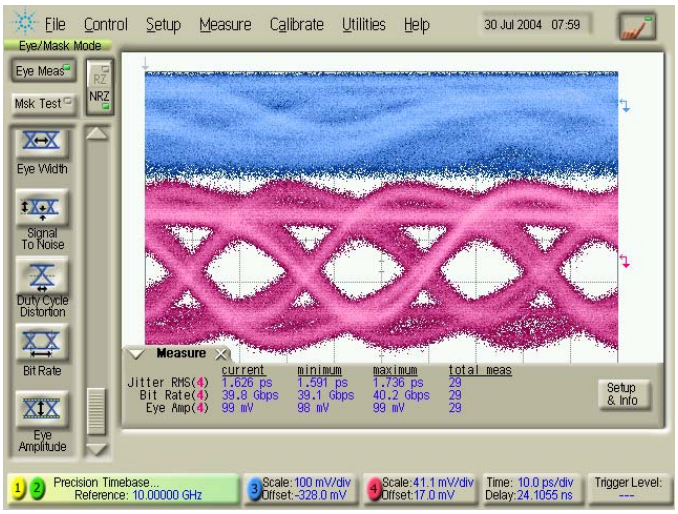

Figure 7. Measured 40 Gb/s (top) input after 9-ft SMA-cable and (bottom) equalized output eye diagram.

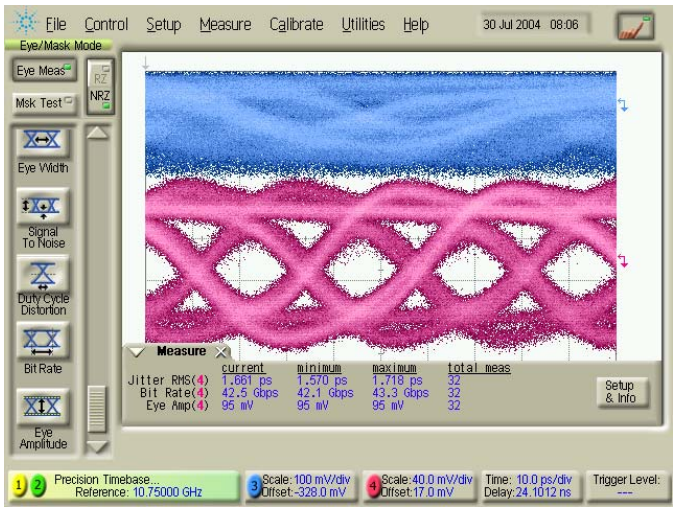

Figure 8. Measured 43 Gb/s (top) input after 9-ft SMA-cable and (bottom) equalized output eye diagram.

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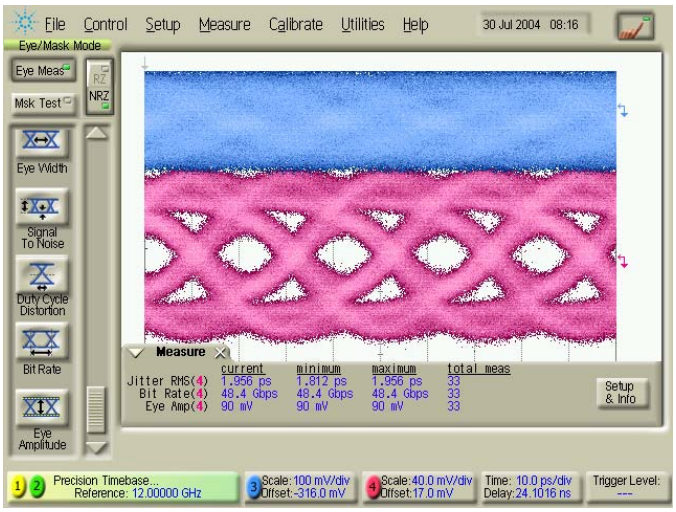

Figure 9. Measured 48 Gb/s (top) input after 9-ft SMA-cable and (bottom) equalized output eye diagram.

Figure 10. Measured 49 Gb/s (top) input after 9-ft SMA-cable and (bottom) equalized output eye diagram.

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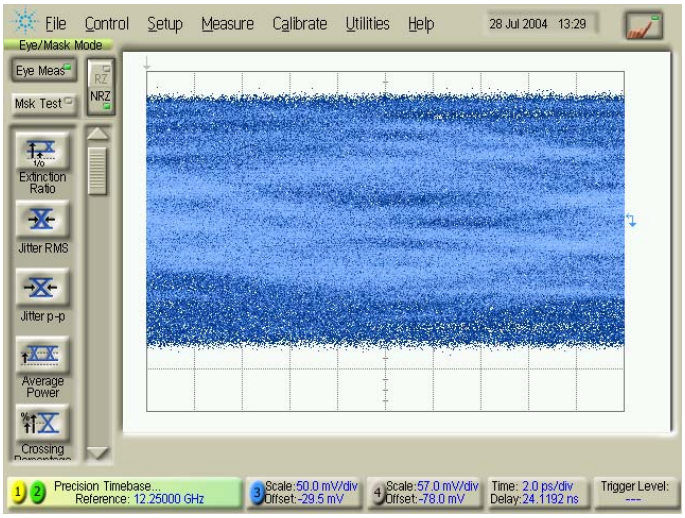
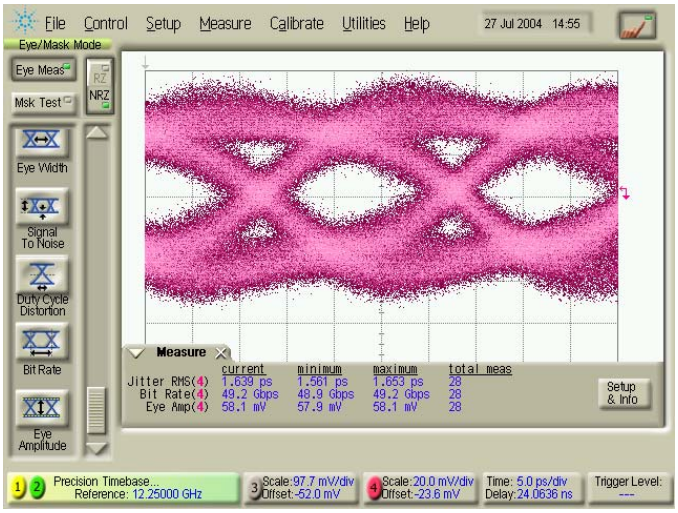


(a)



(b)

Figure 11. Measured 49 Gb/s (a) input after 6.5-ft SMA-cable and (b) equalized output eye diagram.