Low-Power, Low-Phase Noise SiGe HBT Static Frequency Divider Topologies up to 100 GHz

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***Abstract* — Static 2:1 frequency dividers with different latch configurations were designed and fabricated in two SiGe HBT technologies. The self-oscillation and maximum operation frequency are found to be correlated with the f_{MAX} but not with the f_T of the technology. A self-oscillation frequency of 77 GHz, the highest among static dividers in SiGe HBT technology, is achieved with the lowest power consumption of 122 mW from 3.3 V supply. Phase noise measurements of the 100-GHz input and 50-GHz output signals indicate ideal behavior with no measurable noise contribution from the divider. All fabricated dividers feature an integrated single-ended-to-differential transformer for ease of testing, yet broadband 20 GHz-100 GHz operation is maintained.**

***Index Terms* — Static frequency dividers, SiGe HBT.**

I. Circuit Design

A study of static divider performance in two SiGe technologies was performed. For a fair comparison, the same divider topology, shown in Fig. 1, was maintained and the same supply voltage was used. The single-ended input is converted to a differential signal through an on-chip transformer. A 50-Ω, 250-mVpp swing buffer is used at the output. Two different latch configurations are implemented in the core of the divider for comparison.

A. Integrated Transformer

A 1:1 transformer similar to that in [1] was scaled to 100 GHz and realized with vertically-stacked, symmetrical square coils in the top 2 metal layers of the technology. The transformer diameter is 30 µm, with 2-µm stripe width and 1-µm spacing. The coupling coefficient between the two coils is 0.855. The role of the transformer is solely to facilitate divider measurements and to avoid the use of expensive and bulky test setups. A matching network consisting of an inductor and a capacitor was added to match the divider input to 50 Ω. Simulation results of the transformer with matching network are reproduced in Fig. 2. S_{21} peaks at 100 GHz, with a maximum value of -3.5 dB, while S_{11} remains below -10 dB from 30 GHz to 110 GHz. This is the first demonstration of an integrated transformer in a circuit operating at 100 GHz.

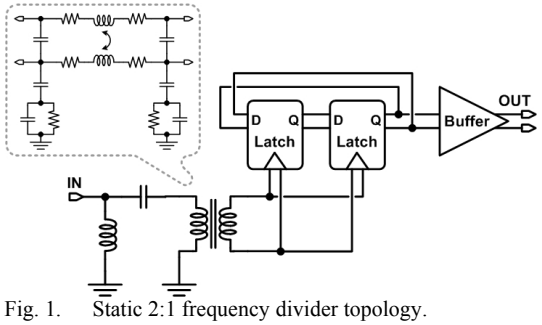

Fig. 1. Static 2:1 frequency divider topology.

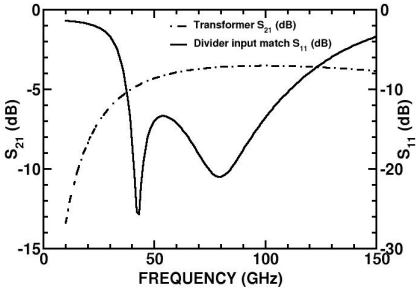

Fig. 2. Simulated on-chip transformer performance.

B. Latch Design

Two different ECL latches, with and without emitter followers (EF) on the clock input path, shown in Fig. 3a and 3b, respectively, were designed. Notice that, apart from peaking inductors operating at 100 GHz, no bandwidth improvement techniques, such as split-resistor load [1] or double emitter-followers in the feedback [2], are employed. The use of inductors is critical to reduce power dissipation while still achieving high frequency operation. The first version, with double EF on the clock input path, operates from 3.3 V and consumes 19.5 mA. The second latch consumes only 11.5 mA from 3.3 V.

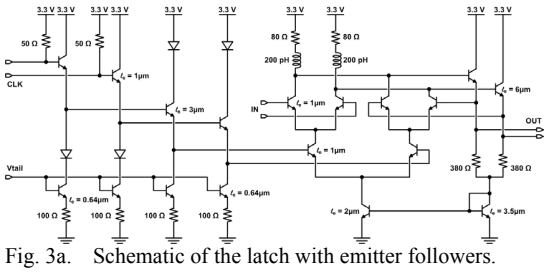

Fig. 3a. Schematic of the latch with emitter followers.

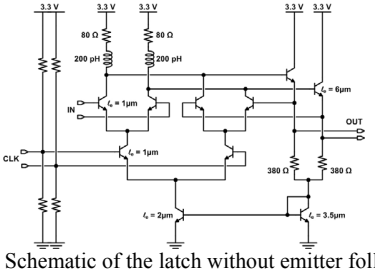

Fig. 3b. Schematic of the latch without emitter followers.

II. Fabrication

Die photos of the two dividers are shown in Fig 4. Both dividers were fabricated in two SiGe HBT technologies with exactly the same circuit layout and without redesign between the two technologies. The first technology is a 0.13 µm SiGe BiCMOS process (referred to as BiCMOS9 [3]). Only the BiCMOS9 HBTs, with an f_T of 170 GHz and f_{MAX} of 200 GHz, were utilized. The second technology (referred to as BipX [4]) features HBTs with an f_T of 230 GHz and f_{MAX} of 300 GHz. Measured f_T and f_{MAX} curves for the two technologies are plotted versus collector current density in Fig. 5. Dividers were also fabricated and tested in two other BipX process splits with f_T/f_{MAX} in the 220 GHz to 270 GHz range.

III. Test Setup

The test setup used for divider characterization is shown in Fig 6. All measurements were performed directly on wafer with 110-GHz GGB probes. An HP 83752A 0.01-20-GHz signal source and Millitech AMC 15 00000 ×4 and AMC 10 00000 ×6 frequency multipliers were employed to generate the input signal in the 50-75 GHz and 75-100 GHz frequency bands, respectively. Below 50 GHz, measurements were carried out with the Agilent E8257D PSG analog 250 kHz-67 GHz signal generator as the signal source. A 50-GHz Agilent E4448A PSA with an Agilent 11970W 75-110 GHz waveguide mixer was used to observe the spectrum and phase noise of the input and output signals.

IV. Measurement Results

All fabricated dividers operate from 3.3 V and consume 122 mW without clock EF, and 145 mW with clock EF. Their sensitivity curves are plotted in Fig. 7. In both technologies, the elimination of the EF stages from the clock input path results in a 20% increase in the self-oscillation frequency (SOF). This is in agreement with simulations and with the reduced voltage gain of the EF at high frequency [5]. Fig. 7 also shows that the SOF is correlated with the speed of the technology. By moving to a faster technology, the transistor f_{MAX} is increased 1.5 times from 200 GHz to 300 GHz, and the SOF of the dividers increases from 54 GHz to 77 GHz. The results on different BipX splits, with f_T of 230 GHz and 265 GHz, reveal lower divider SOF for the 265-GHz f_T circuits, in agreement with the HBT power gain at 65 GHz, rather than its f_T. Measurements also indicate that the maximum divider frequency tracks its SOF. Therefore, we recommend that the self-oscillation frequency be used to more fairly compare the performance of static dividers because it depends solely on the circuit parameters. On the other hand, the maximum operating frequency of the divider depends to a large extent on the test setup and on the power available from the signal source.

The fastest divider has a SOF of 77 GHz, the highest reported to date in any SiGe HBT/BiCMOS technology. It divides correctly up to at least 100 GHz. The spectrum of the 50-GHz divided-by-two output signal is shown in Fig. 8.

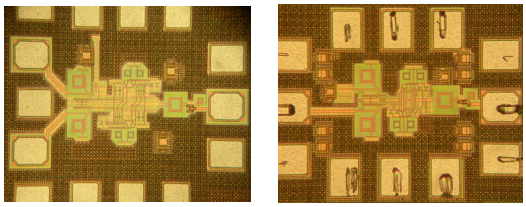

Fig. 4. Die photos of the divider a) with (left - 515µm × 473µm) and b) without EF (right - 502µm × 360µm).

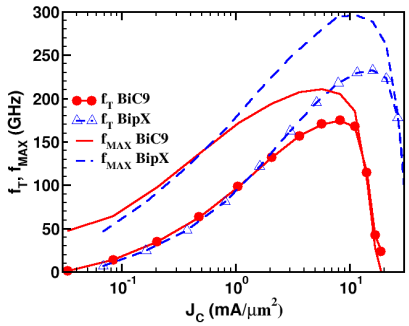

Fig. 5. Measured f_T and f_{MAX} at V_{CE}=1V on transistors with 3 emitter stripes, 6 base, and 4 collector contacts in the two technologies (BiCMOS9 and BipX).

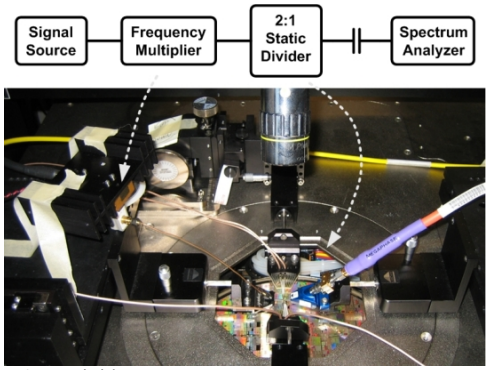

Fig. 6. Divider test setup.

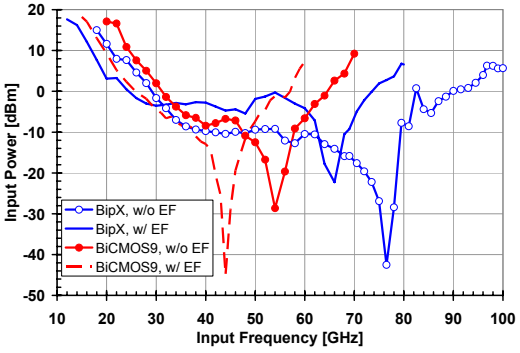

Fig. 7. Measured sensitivity curves of the 2 static dividers in the BiCMOS9 and BipX technologies.

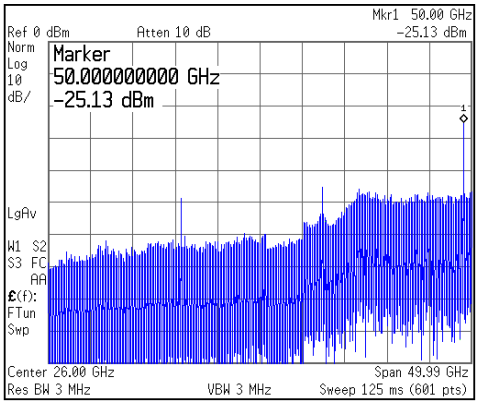

Fig. 8. Spectrum of the divide-by-two 100-GHz signal obtained from the BipX divider without EF.

In order to assess the noise added by the divider, the phase noise of the 100 GHz multiplier output signal was measured as a function of the multiplier input power at 16.667 GHz (Fig. 9). The measurement accuracy is limited by the mixer noise floor for low-power inputs, and by the mixer non-linearity for high-power inputs. Fig. 10 shows a phase noise of -96.4 dBc/Hz at 100 kHz offset from the 50-GHz divider output. For comparison, the measured phase noise at a 100 kHz offset from the 100-GHz divider input signal is -90.4 dBc/Hz (with 0.3 dBc/Hz measurement error). This proves that the divider noise contribution is negligible since the phase noise is improved by an ideal 6 dB after the divide-by-two operation. This is an important result for PLL applications, where the phase noise of the VCO must not be degraded by the divider. Lack of a signal source with sufficient output power prevented divider testing above 100 GHz. The same divider was tested over temperature and found to divide up to 97 GHz at 50°C and up to 91 GHz at 100°C, Fig. 11. To explore the effect of process variations on the performance of the divider without EF, a wafer map of its SOF in the BipX process is presented in Fig. 12. Sensitivity curves collected from 12 dice on 4 wafers are shown in Fig. 13 for the BiCMOS9 version.

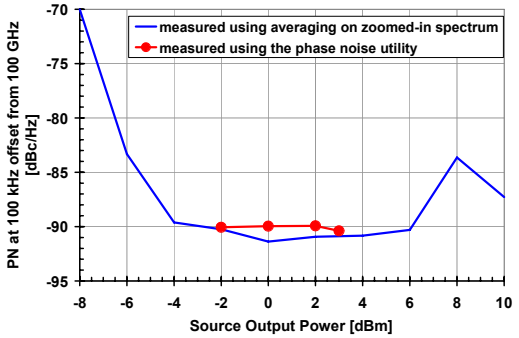

Fig. 9. Phase noise of a 100-GHz signal measured using two methods. This 100-GHz signal was used as the divider input.

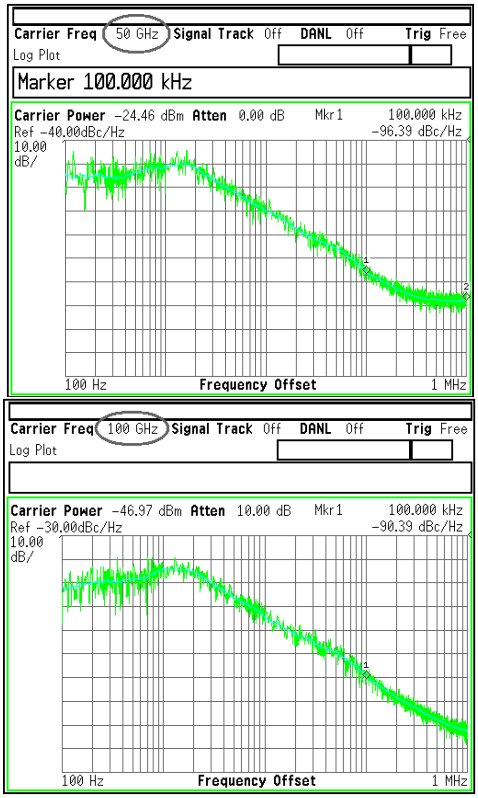

Fig. 10. Phase noise of the divider without emitter followers fabricated in BipX (top) with 100-GHz input signal. Phase noise of the 100-GHz input signal (bottom).

V. Comparison with Previous Dividers

The two dividers fabricated with 170-GHz HBTs, are compared in Fig. 14 with a previously published divider fabricated in the same technology and which is based on a MOS-HBT (BiCMOS) cascode topology [1]. In the BiCMOS cascode latch, the clock HBT pair is replaced by an NMOS pair [1]. Since the BiCMOS latch is 15% faster, it is expected that the self-oscillation frequency of the 230-GHz HBT divider can further be improved by employing a BiCMOS cascode when 90-nm MOSFETs are available.

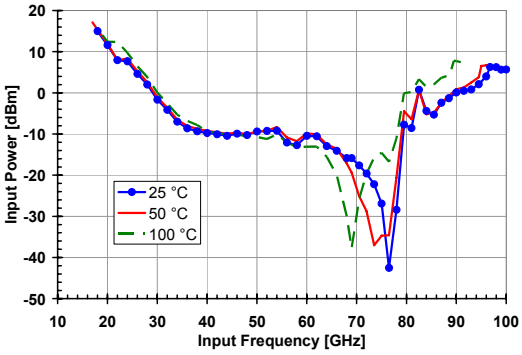

Fig. 11. Sensitivity curves across temperature for the divider without EF fabricated in the BipX technology.

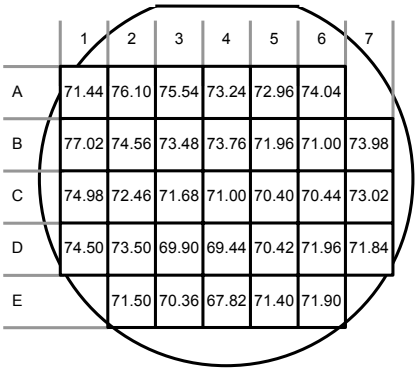

Fig. 12. Wafer map of the self-oscillation frequency (in GHz) for the BipX dividers without EF.

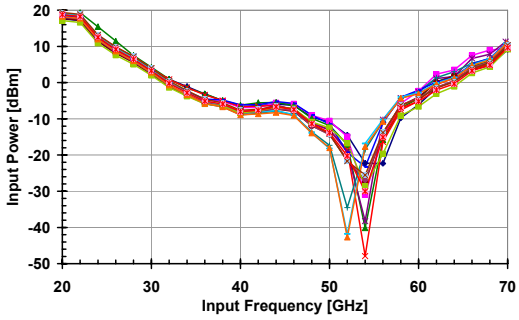

Fig. 13. Effect of process variations on the divider without EF fabricated in the BiCMOS9 process.

Finally, dividers presented in this work are compared to other state-of-the-art dividers in Table 1. With a SOF of 77 GHz and a power dissipation of 122 mW, this design has the lowest power and the highest self-oscillation frequency among all SiGe HBT dividers.

VI. Conclusion

Static frequency dividers with two different topologies were designed and fabricated in 170-GHz and 230-GHz SiGe HBT technologies. It was observed from measurements and simulations that dividers operate faster when EF are removed from the clock path. The maximum operation frequency and the SOF were found to be correlated with the transistor f_{MAX} but less so with f_T. A 1:1 transformer was employed to provide single-ended-to-differential conversion of the input signal, yet the circuit operates from 20 GHz to 100 GHz. A record low power of 122 mW and operation up to at least 100 GHz (limited by the measurement setup) was demonstrated with no measurable phase noise contribution from the divider.

References

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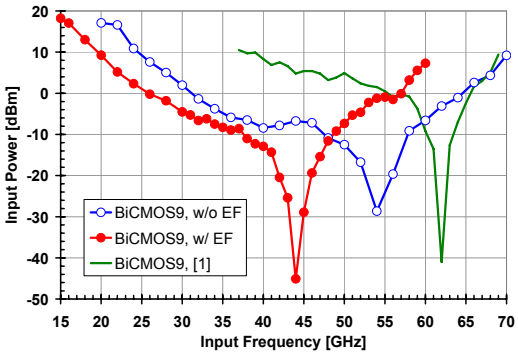

Fig. 14. Comparison of the two HBT-only dividers to a MOS-HBT static divider from [1]. All dividers were fabricated in the same BiCMOS9 process and were biased from a 3.3V supply.

Table. 1. Comparison to Previously Published Static Frequency Dividers.

Reference	Self-Oscillation Freq.	Max. Divider Freq.	Power Consumption	Technology
[6]	86 GHz	150 GHz	?	450-GHz f_T InP
[5]	33 GHz	100 GHz	750 mW	135-GHz f_T InP
[7]	48 GHz	66 GHz	80 mW (1.8V)	90nm CMOS
[8]	65 GHz	110 GHz	1.35 W (-5.2V)	225-GHz f_T SiGe:C HBT
[9]	95 GHz	143.6 GHz	90 mW	400-GHz f_T InP
[2]	71 GHz	96 GHz	770 mW (-5.0V)	210-GHz f_T SiGe HBT
This Work	77 GHz	>100 GHz	122 mW (3.3-3.6V)	230-GHz f_T SiGe HBT
This Work	54 GHz	70 GHz	145 mW (3.3-3.6V)	170-GHz f_T SiGe HBT