SiGe BiCMOS for Analog, High-Speed Digital and Millimetre-Wave Applications Beyond 50 GHz

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***Abstract* — This paper explores the application of SiGe BiCMOS technology to mm-wave transceivers with analog and digital signal processing. A review of 10-80Gb/s SERDES performance across 3 SiGe BiCMOS and CMOS technology nodes reveals remarkable similarities with digital CMOS IC scaling and points to the benefits of a SiGe BiCMOS roadmap. Examples of 40-Gb/s equalizers, track-and-hold amplifiers and ADCs with mm-wave sampling clocks are provided, along with GHz-range opamp filters and 65-GHz wireless transceivers. Automotive radar and imaging applications in the 80-100 GHz range are also briefly discussed.**

I. Introduction

Historically, due to larger-scale economies, wireless and (briefly) fibre-optic applications have driven SiGe BiCMOS process development [1]-[3]. While SiGe HBT performance has steadily improved over the last few years [4]-[8], the frequency of most applications has remained in the 2-10 GHz range. This has allowed CMOS technology to catch up in some of the larger volume markets, such as WLAN and 10-Gb/s datacom, where SiGe BiCMOS technology had carved a niche. The shift away from continual speed enhancement and towards higher digital signal processing content will place greater demand in the future for ultra-fast ADC techniques in applications such as 40-Gb/s fibre-optic, backplane and chip-to-chip communication, instrumentation, and digital cinema. In these applications, SiGe HBTs must be paired with nanoscale MOSFETs to deliver the required performance at acceptable power dissipation levels. Ultra high f_T and f_{MAX} values, simultaneously exceeding 250 GHz, as well as low phase noise are, however, required for the potentially lucrative 77/94GHz automotive, mm-wave imaging, and 100-Gb/s Ethernet applications. This paper addresses transistor performance scaling and building blocks for 40-80Gb/s transceivers with analog and digital signal processing and for mm-wave radio and radar.

II. SiGe HBT and SERDES Performance Scaling

Benefiting from the clear guidelines set forth by the International Roadmap for Semiconductors (ITRS), CMOS technology scaling has continued unabated to nanometre dimensions. Cut-off and maximum oscillation frequencies in general purpose (GP) 65-nm CMOS technologies with physical gate lengths below 45 nm now exceed 200 GHz at 1V supply [9]. Power dissipation, noise figure, and phase noise performance in CMOS RF and fibre-optic ICs improve with scaling. At the same time, as the data compiled in Fig. 1 illustrate, SiGe BiCMOS technology evolution has been rather irregular, with missed nodes and at least 3 foundries jockeying up for the leading position at one time or another. Interestingly, a clear scaling law exists, as indicated by the dashed trend line, which allows SiGe BiCMOS to retain a 2-generation advantage over CMOS in terms of f_T and f_{MAX}.

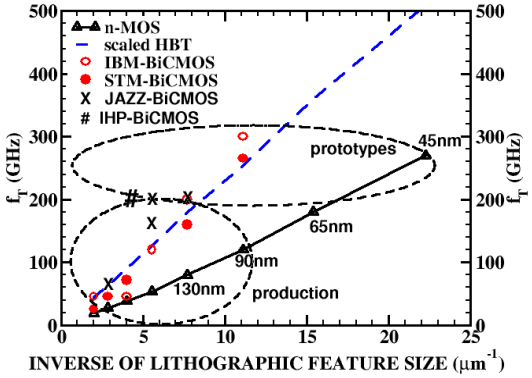

Fig. 1 f_T scaling in CMOS and SiGe BiCMOS technology nodes

Fig. 2 shows the measured f_T of production and of prototype SiGe HBTs as a function of collector current density, along with the f_T of a scaled device simulated using Silvaco's T-CAD platform. The scaled transistor has 100-nm emitter width, a 5-nm thick base doped 8×10^{19} cm^{-3}, a 25-nm thick collector, and features a trapezoidal Ge profile varying from 20% to 40%. Its NF_{MIN} is 1.1 dB at 65 GHz while f_T and f_{MAX} simultaneously exceed 500 GHz at a current density of 30 mA/μm^2 with a peak of 560 GHz at 60 mA/μm^2. The simulator was calibrated on experimental 160-GHz SiGe HBT characteristics from production SiGe BiCMOS processes [4], [6]. For comparison, an InP HBT with 12.5-nm base width and 710/340 GHz f_T/f_{MAX} at 20 mA/μm^2 was

recently fabricated [10]. These results indicate that a SiGe HBT structure, much like the ones prototyping today, is capable of maintaining the 2× advantage over 45-nm MOSFETs. However, the significant increase in current density with scaling, and slightly higher NF_{MIN} than MOSFETs at comparable f_T, remain weak points of SiGe HBTs. Indeed, experimental device [11] and 60-GHz circuit data [12] indicate comparable or lower NF_{MIN} for 90/65-nm MOSFETs than for the best SiGe HBTs.

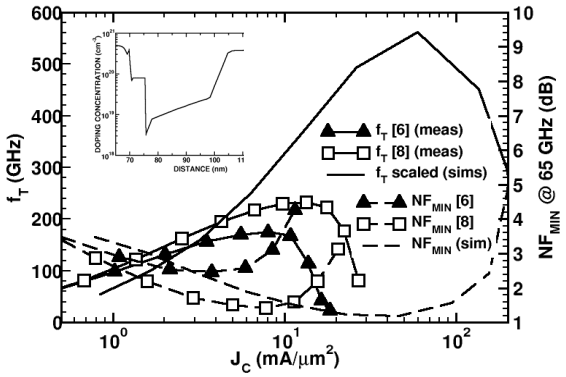

Fig. 2 f_T and NF_{MIN} at 65 GHz vs J_c in production [6], prototype [8], and in simulated scaled SiGe HBTs. The simulated structure is shown in the inset.

A fully integrated 5-GHz wireless transceiver and a 10-Gb/s SONET receiver were first reported at MRS in 1998 [13]. These circuits were implemented in an early version of a 0.5µm SiGe BiCMOS process with 45/60-GHz f_T/f_{MAX} [1]. The SONET receiver employed E^2CL logic and operated from a -5.2V supply. The first single-chip 10-Gb/s SONET SERDES [14] and a 10-Gb/s Ethernet (10GE) SERDES (Fig. 3) fabricated in 0.35µm [2] and 0.25µm [3] SiGe BiCMOS processes were introduced in December 2000 and the summer of 2001, respectively. Both these ICs rely on simpler ECL families to reduce the supply voltage of the 10-Gb/s circuitry to 3.3V.

The 0.35µm SiGe HBT has an f_T of 45 GHz and allows for a 10-GHz latch to be realized with 2-mA tail current and no inductive peaking. The total power dissipation of the SONET SERDES is 2.2 W and includes a VCSEL driver with output swing and pre-emphasis control, laser bias and monitoring circuitry. The output swing and VCSEL modulating current are adjustable over a 3:1 range up to $2\times750mV_{pp}$ and 15mA, respectively [14]. The 10GE SERDES dissipates 3.2 W from 3.3-V, 2.5-V and 1.8-V supplies. It incorporates over 200,000 digital CMOS gates embedded between the analog 10.3-Gb/s and 3.125-Gb/s interfaces (Fig.3). Taking advantage of both SiGe HBT and CMOS scaling across technology nodes, and reducing the number of vertically-stacked transistors, two new generations of this chip have since been ported, first to 180-nm SiGe BiCMOS [4] dissipating about 2 W from 3.3-V and 1.8-V supplies, and next to 130-nm CMOS, dissipating approximately 1 W from a 1.2-V supply.

The most interesting aspect of this SERDES family is that it demonstrates the benefits of scaling for mixed-signal SiGe BiCMOS products. Scaling leads to an almost linear improvement in jitter, rise/fall times, die area, supply voltage and power dissipation [15]. It also confirms the prediction made in [14] that only at the 130-nm node would CMOS be able to compete with SiGe BiCMOS technology for 10-Gb/s SERDES applications. Indeed, several 10-Gb/s SERDES chips in 130-nm CMOS, including a VCSEL driver [16], have been reported during the last 2 years while 180-nm CMOS solutions could not compete [17].

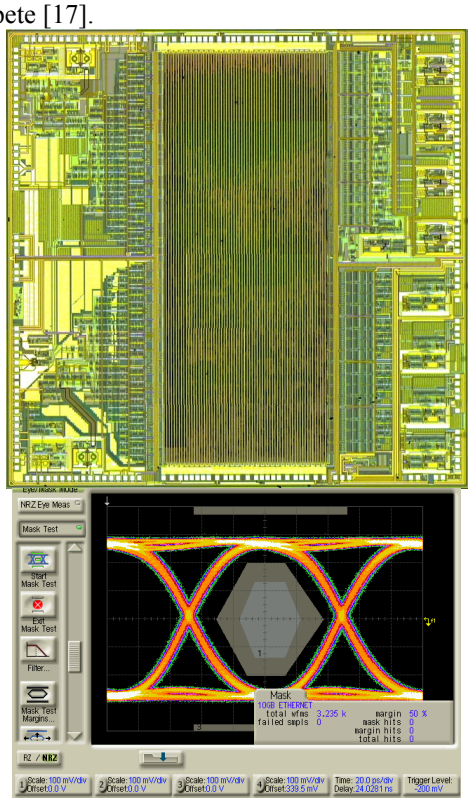

Fig. 3 Single-chip 10GE transceiver in 0.25µm SiGe BiCMOS: a) die photograph and b) 10.3-Gb/s output eye diagram (Quake Technologies 2001)

Although a 40-GHz flip-flop [18] and a 60-Gb/s 2:1 MUX [19] have recently been realized in 90-nm CMOS, a 45-GHz flip-flop, as needed for a full-rate 40-Gb/s SONET SERDES with FEC, has only been demonstrated in InP [20] and SiGe BiCMOS technologies [21]-[23]. Scaled 40/80-Gb/s SERDES can now be fabricated in 130-nm SiGe BiCMOS technology [6], operating from 2.5-V supply with similar power dissipation and performance margin (Fig.4) as the first-generation 10GE chip (Fig. 3). This (4-8)× speed increase [23] at comparable power dissipation and cost has been made possible by the 4× improvement in transistor f_T/f_{MAX} and by relying on a MOS-SiGe HBT cascode topology and inductive

peaking [23]. The combination of MOSFETs and HBTs on the high-speed path capitalizes on the low V_T of nanoscale MOSFETs, the cancellation of Miller capacitance, and on the low gate resistance to improve switching speed over HBT-only logic while reducing the power supply voltage to 2.5 V and 1.8 V [11, 24].

Fig. 5 illustrates the scaling of MOS-HBT cascode inverter delay between production 180-nm and 130-nm SiGe BiCMOS nodes with comparable SiGe HBT performance. The benefits of future scaling to 90-nm BiCMOS are also clearly apparent where the delay reduction from 5.1 ps to 3.3 ps is solely due to replacing 130-nm with 90-nm MOSFETs. The inset shows how emitter-followers (EF) can be employed for level shifting and further increase speed. Note that the optimal delay is achieved when the tail current corresponds to 0.3mA/μm of gate width for the MOSFETs that make up the differential pair [27].

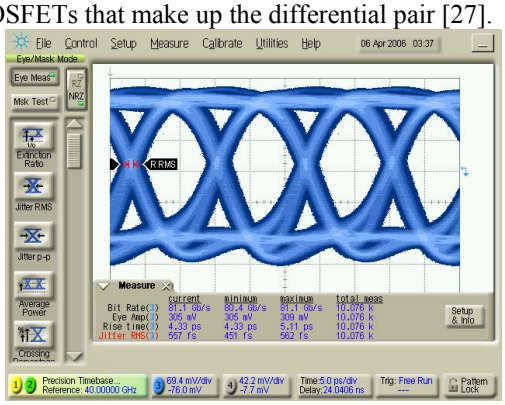

Fig. 4 2×300mV$_{pp}$, 80-Gb/s output eye diagram (running for 1 hour) of a 2.5-V, 1.4W transmitter [23] implemented in a 130-nm SiGe BiCMOS process [6].

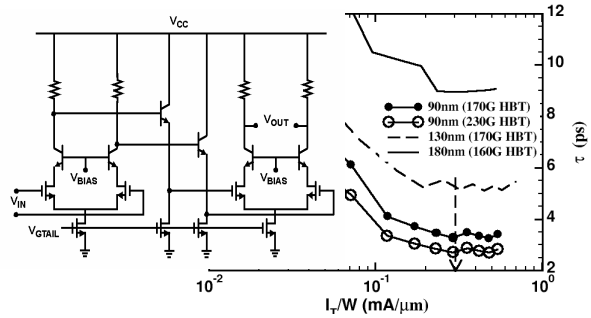

Fig. 5 Scaling of BiCMOS cascode inverter delay across nodes obtained from measured DC and high-frequency characteristics. All inverters have a gain of 1.5 and a fanout of 1. The impact of the EF stage is not included.

III. Analog Circuits

Operational amplifiers (opamps) can be used in GHz-range filters and delta-sigma modulators if their unity gain bandwidth exceeds 10 GHz [25], [26]. The schematic of a fully differential opamp employing a MOS-HBT cascode with cascode p-MOSFET load [25] is shown in Fig. 6. The circuit has an EF output for level-shifting purposes and to reduce the output impedance. It was implemented in 130-nm and 180-nm generations of SiGe BiCMOS technologies with similar HBT f_T/f_{MAX} [25],[26]. The MOS-HBT cascode has speed, linearity and noise advantages over the HBT-HBT cascode. This is the result of the lower input time constant $R_G\times(C_{gs}+C_{gd})$, better phase margin and concomitant low-noise and high-linearity bias in MOSFETs, as opposed to HBTs. To maximize the unity gain bandwidth, all MOSFETs and HBTs are biased at the peak f_{MAX} current density which, for n-MOSFETs and p-MOSFETs, is approximately 0.2 mA/μm and 0.08 mA/μm, respectively, across technology nodes and foundries [27]. A record unity gain bandwidth of 37 GHz was measured in the 130-nm half-circuit with 10-mA current [25]. Opamp biquad filters (Fig. 7) were fabricated and their performance was compared with that of 2-stage g_m-LC bandpass filters based on the same MOS-HBT cascode topology (Fig. 8). The measured transfer characteristics, *NF* and linearity of both filters are shown in Figs. 9-11. With comparable linearity and power dissipation, the opamp filter occupies 10 times smaller area than the g_m-LC filter.

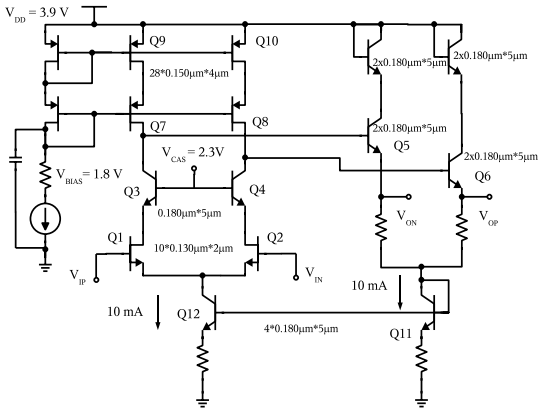

Fig. 6 130-nm SiGe BiCMOS opamp schematics.

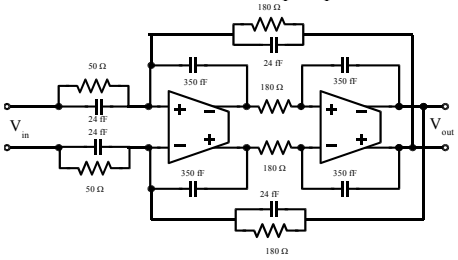

Fig. 7 130-nm SiGe BiCMOS biquad filter diagram.

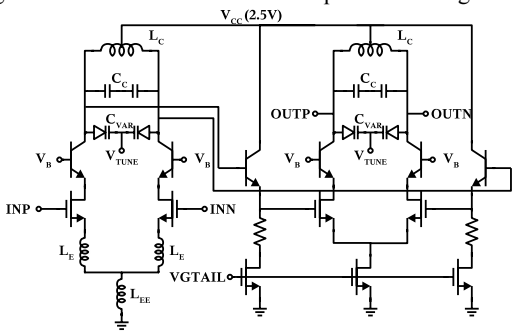

Fig. 8 Block diagram of 130-nm SiGe BiCMOS g_m-LC filter based on a BiCMOS cascode.

IV. 40-Gb/s Equalizers

Production SiGe BiCMOS technology is well-poised to address 45-Gb/s transceivers with equalization. A typical block diagram of an equalizer with analog DSP is shown in Fig. 12. While the FFE block could be realized in 90-nm CMOS, the DFE requires a full-rate 45-GHz flip-flop which is unlikely to be implemented in CMOS with adequate margin before the 65-nm node.

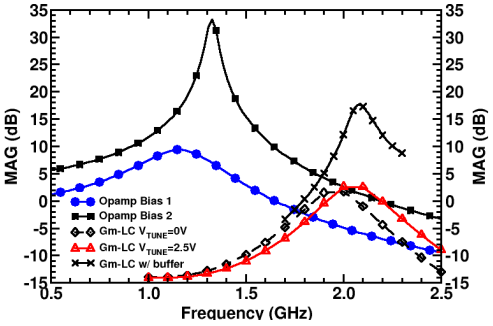

Fig. 9 Measured biquad and gm-LC filter characteristics for different bias conditions. Measurements of the g_m-LC filters with and without an output buffer are provided.

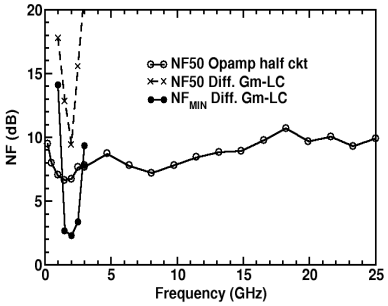

Fig. 10 Measured 50-Ω *NF* of opamp half-circuit and of differential gm-LC filter.

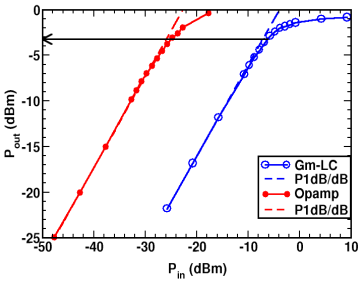

Fig. 11 Comparison of the measured linearity of two-stage opamp and g_m-LC filters operating at 1.2 GHz and 1.9 GHz, respectively.

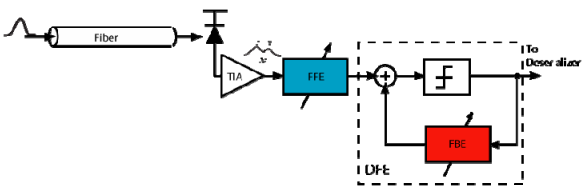

Fig. 12 Block diagram of electrical equalizer for polarization mode dispersion in optical fibers.

A. Feed Forward Equalizer

Fig. 13 describes the block diagram of a 7-tap 40-Gb/s FFE [28] implemented in a 180-nm SiGe BiCMOS process [4]. A differential, distributed topology is employed which is realized with M6-over-M2 microstrip lines and HBT-cascode taps with gain and sign control. The measured and modelled characteristics of the 9-ft SMA cable used in system-level simulations and experiments are illustrated in Figs. 14-16. The circuit is capable of compensating for more than 20dB loss at 20 GHz. Error-free operation was verified from 5 Gb/s to 40 Gb/s, and equalized eyes were obtained up to 49 Gb/s [28].

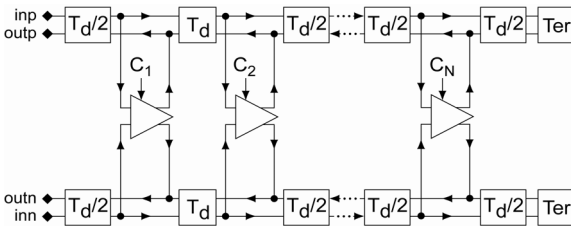

Fig. 13 Schematics of 7-tap FFE implemented in 180-nm SiGe BiCMOS.

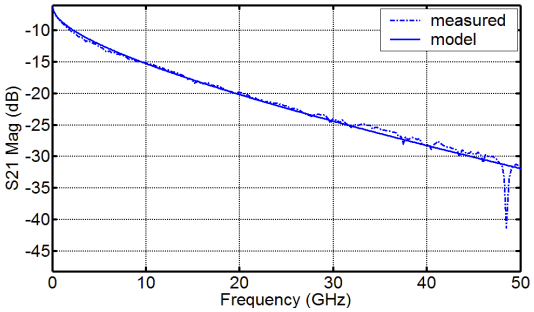

Fig. 14 Modeled vs. measured transmission loss of 9-ft SMA cable.

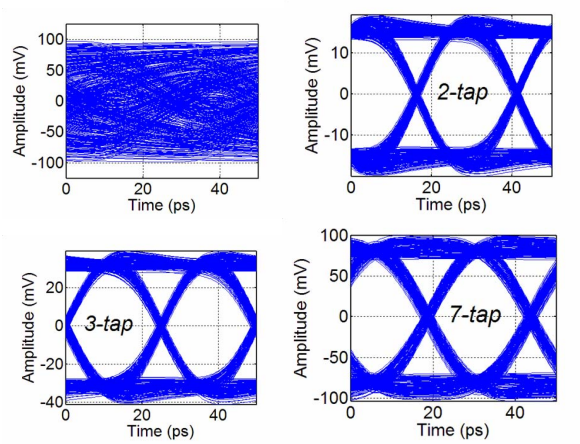

Fig. 15 Modelled 40-Gb/s equalized eye diagrams as a function of the number of equalizer taps. a) input signal after passing through the SMA cable and output of b) 2-tap, c) 3-tap, d) 7-tap equalizers.

B. 40 Gb/s DFE

The DFE whose block diagram is shown in Fig. 17, was implemented in the same technology [4] with 3.3-V ECL and verified to correctly equalize a PRBS

passing through a 9-ft SMA cable at data rates from 5 Gb/s to 39.5 Gb/s, Fig.18 [29].

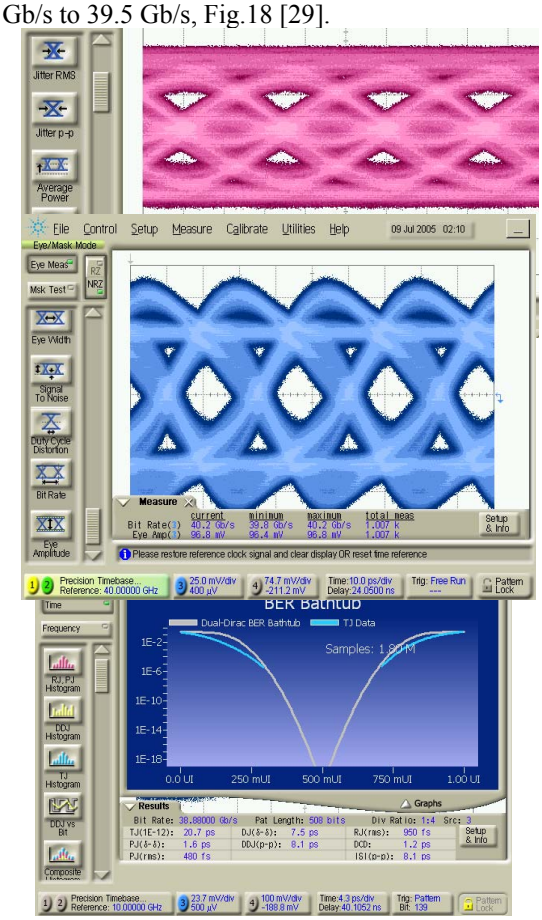

Fig. 16 FFE input/output 40-Gb/s eye diagrams and bathtub.

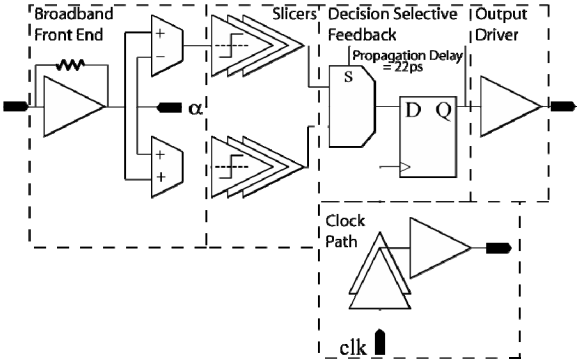

Fig. 17 1-tap look-ahead DFE architecture.

C. 40 Gb/s Digital Equalizer Blocks

When the technology has adequate speed, a digital DSP solution (Fig. 19) is preferred over an analog one due to its increased flexibility. In this architecture, the most critical block is the T&H amplifier (Fig. 20), which must simultaneously satisfy broad band, low noise and high linearity requirements. A T&H amplifier with over 40-GHz bandwidth (Fig. 21) and 4.5-bit linearity was reported in [30].

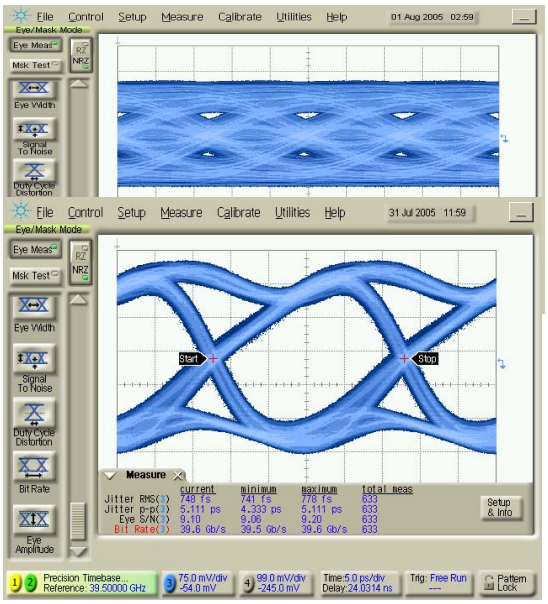

Fig. 18 39.5-Gb/s DFE input and output eye diagrams after passing through a 9-ft long SMA cable.

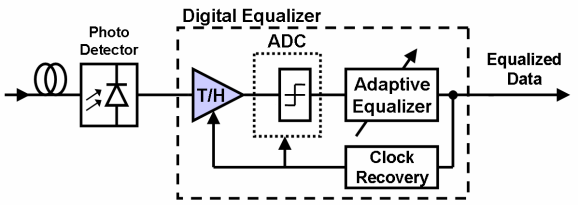

Fig. 19 Block diagram of a DSP based fiber optic equalizer.

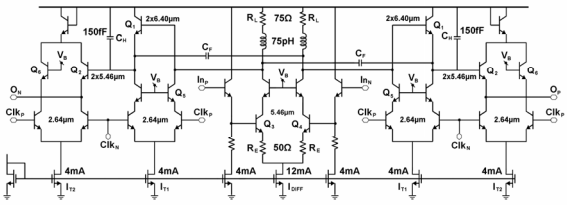

Fig. 20 Circuit diagram of the track & hold block in 180-nm SiGe BiCMOS [4]. Signals In_N and In_P are provided by a low-noise, broadband transimpedance amplifier [30].

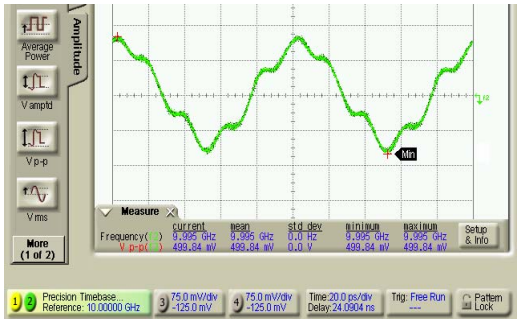

Fig. 21 Differential output of the T&H amplifier for an 10-GHz sinusoid sampled at 40GHz (70 mV/div) [30].

V. ADCs

The high intrinsic speed of both SiGe HBTs [1]-[8] and CMOS [11], [12] transistors provides an excellent

incentive for the introduction of digital signal processing techniques relying on high oversampling ratios and mm-wave clock frequencies. Such techniques typically require only simple circuit topologies, similar to those used in a fiberoptic SERDES, that can be designed to be robust to process variations, transistor leakage and non-linearity. The 2-GHz bandpass ΔΣ design described in [31] employs the g_m-LC transconductor from Fig. 8 and the BiCMOS cascode MSM flip-flop [22] as the 40-GSamples/sec quantizer. The IIP3 test in Fig. 23 shows an SFDR of 61 dB with an ENOB of 8.5 over a 120 MHz band centred at 2 GHz. The 40-Gb/s output stream, reproduced in Fig. 24, can be decimated with the same 2.5-V CML BiCMOS logic family [22]-[24].

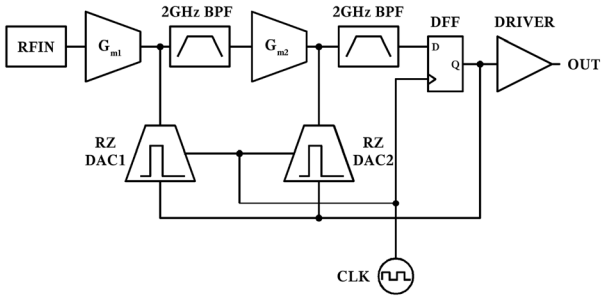

Fig. 22 System level ΔΣ ADC diagram [31].

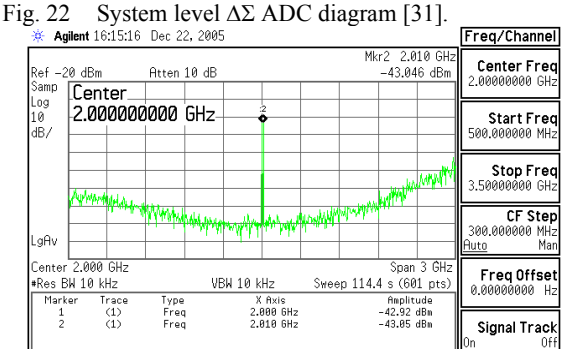

Fig. 23 IIP3 test for 40-GS/s 2-GHz bandpass ADC.

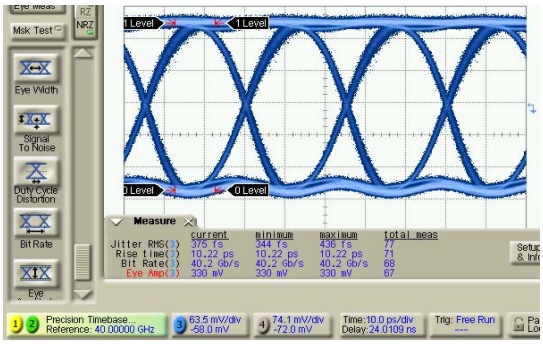

Fig. 24 ΔΣ bandpass ADC output eye diagram in open loop at 40Gb/s with a 2-GHz sinusoidal input.

VI. Millimetre Wave Transceivers

Figs. 25 and 26 reproduce the schematics and die photos of a 60-GHz WLAN transceiver chip set and of a 65-GHz Doppler sensor with on-die patch antenna [32], [33] implemented in a production 180-nm SiGe BiCMOS process with f_T/f_{MAX} of 160 GHz [4]. The transmitter has an image-reject architecture with stagger-tuned, two-stage, lumped poly-phase filters at 5 GHz and at 65 GHz. All three ICs include for the first time a low-phase-noise 60-GHz VCO with 10% tuning range [34] and rely on inductors and transformers to minimize die area. The VCO, downconvert mixer, LNA, and power amplifier employ SiGe HBT cascodes with inductive degeneration to improve isolation and simplify inter-stage matching. The entire design process was conducted using hand analysis and Spectre, as in the 2-10 GHz range [35], while inductors and transformers were designed using ASITIC.

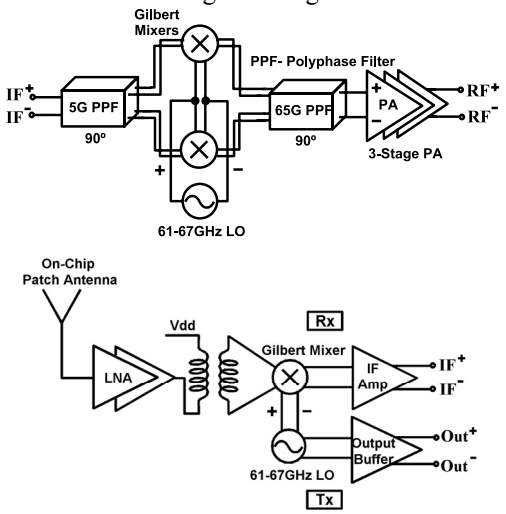

Fig. 25 Block diagrams of a) 60-GHz radio transmitter, b) Doppler radar implemented in 180-nm SiGe BiCMOS.

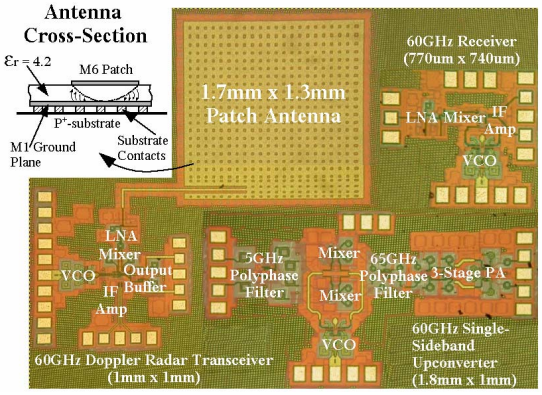

Fig. 26 Die photos of Doppler radar with patch antenna (left) WLAN transmitter (bottom) and receiver (top right).

Fig. 27 shows the measured conversion gain of the WLAN receiver measured on wafer, and of the Doppler sensor with and without the on-die antenna. The Doppler sensor with antenna was tested either by placing a horn antenna, or a GGB probe at different elevations above the on-die antenna. The double-sideband (DSB) noise figure, typically 12 dB, and the corresponding single-ended down-conversion gain of the WLAN receiver, 15 dB at 2.5 V, and 20 dB at 3.3 V supply, are compiled in Fig. 28. More than 45 dB of image rejection has been measured in the WLAN transmitter, Fig. 29.

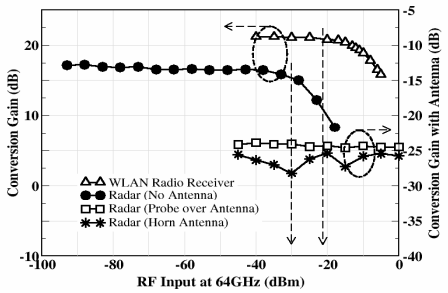

Fig. 27 Single-ended conversion gain for radar and WLAN receiver with radio IF at 1 GHz and radar IF at 730 MHz.

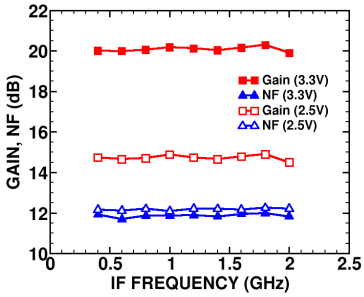

Fig. 28 Measured WLAN receiver gain and noise figure.

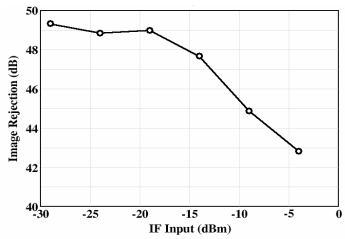

Fig. 29 SSB WLAN radio transmitter image rejection vs. IF input power with 61-GHz LO and 5-GHz IF.

Even though prototype SiGe HBTs and production 65-nm MOSFETs [12] now have adequate performance for automotive radar and imaging at 94 GHz [36],[37], on-chip isolation remains a major concern and will influence the choice of system architecture. For example, beyond 100 GHz, antennas are small enough for phase arrays to be integrated in silicon but crosstalk will limit their applicability. Alternatively, rectangular waveguide arrays are reasonably small, have excellent isolation and, in conjunction with finlines, provide more efficient radiation. For mm-wave medical imaging, where arrays of tens of transceivers are required, *low* (*phase) noise* [36], *isolation* and *power dissipation* are the most important design goals. Fig. 30 reproduces the measured NF_{MIN} at 5 GHz and at 65 GHz in HBTs with f_{MAX} of 200 GHz and 300 GHz, respectively. NF_{MIN} was obtained from Y-parameter measurements as in [35],[39]. The impact of transistor vertical profile scaling on NF_{MIN} is negligible at 5 GHz but becomes significant at 65 GHz. Furthermore, since the transit time through the collector space charge region is significantly larger than the base transit time, correlation between the collector and base shot noise currents increases, pushing the optimum noise current density at mm-waves close to the peak f_T/f_{MAX} current density and changing the value of the optimum noise impedance. The latter has important implications for LNA and VCO design, and allowed us to achieve a record phase noise of -101.3 dBc/Hz at 1 MHz from the 103.6 GHz carrier, as shown in Fig. 31 [36].

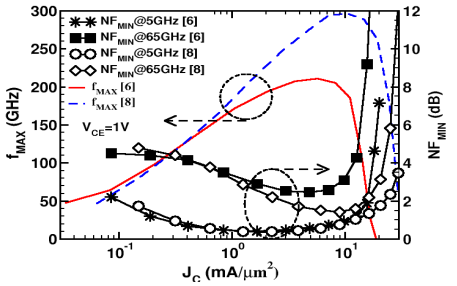

Fig. 30 Measurements of NF_{MIN} scaling in SiGe HBTs.

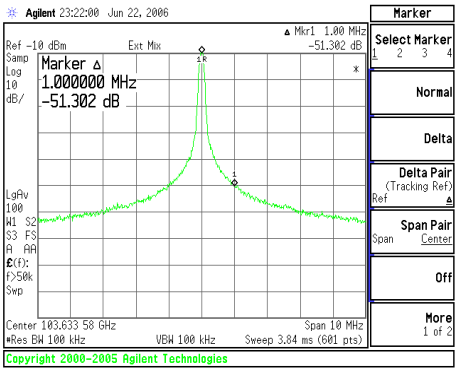

Fig. 31 Measured spectrum, phase noise of 103-GHz VCO.

VII. Conclusions

Low-frequency analog figures of merit such as g_m/I, g_m/g_o, lower *1/f* noise and the larger $f_T \times BV_{CEO}$ product remain the main strengths of SiGe HBTs well into the mm-wave regime. However, historical data, moderate volume markets and relentless pressure from more aggressively scaled CMOS point to the importance of pairing next generation 250/500GHz SiGe HBTs with 90-nm CMOS as a viable and economical way to capture all applications demanding fast HBTs and at least some of the 90/65-nm CMOS market. In that scenario the discontinued supply-voltage scaling of 65-nm CMOS will help release most of the pressure off SiGe. Stand-alone SiGe HBT technology, stripped of its CMOS advantage, will have a difficult time competing with InP or CMOS.

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