SiGe BiCMOS for Analog, High-Speed Digital and Millimetre-Wave Applications Beyond 50 GHz

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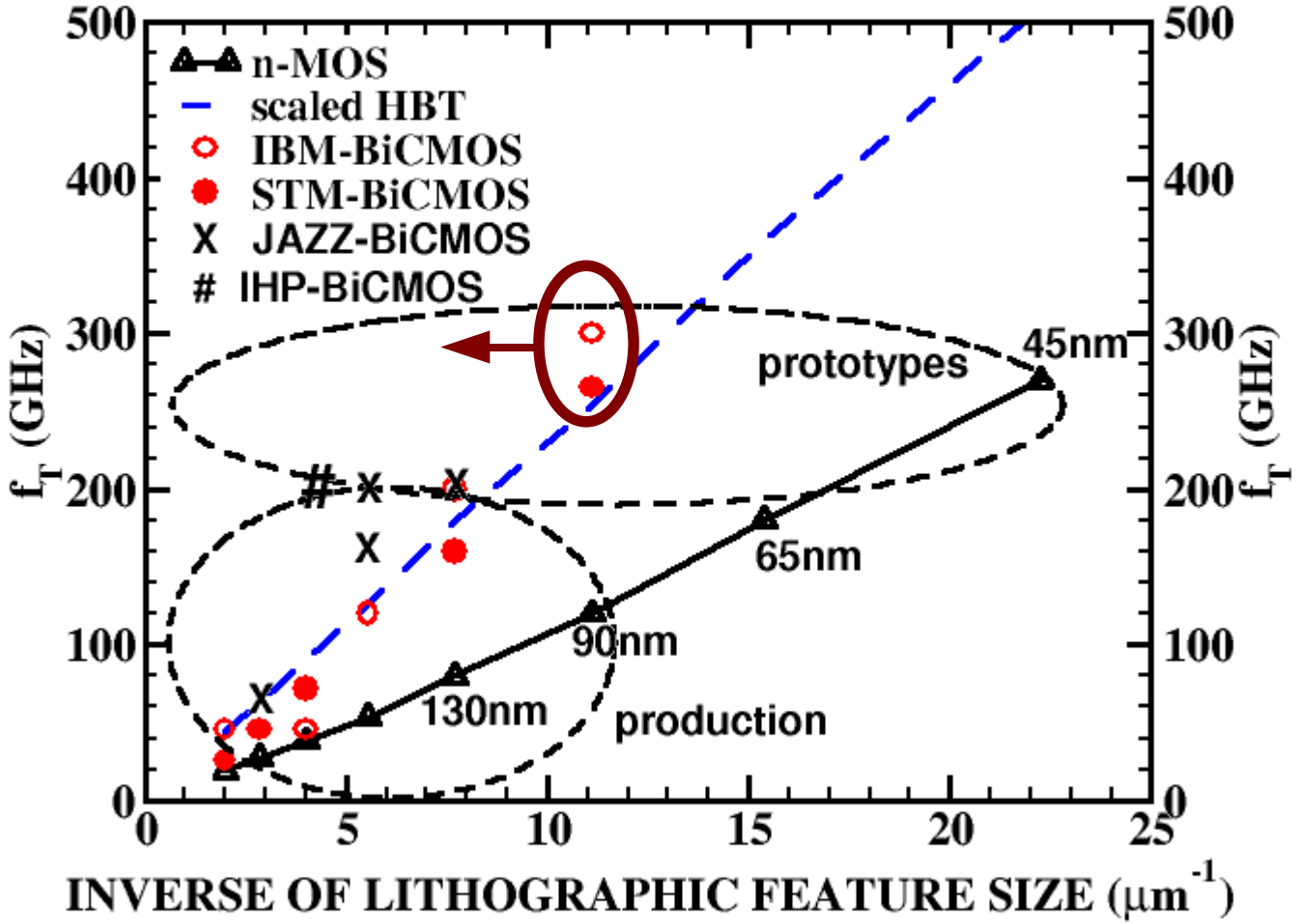
Outline

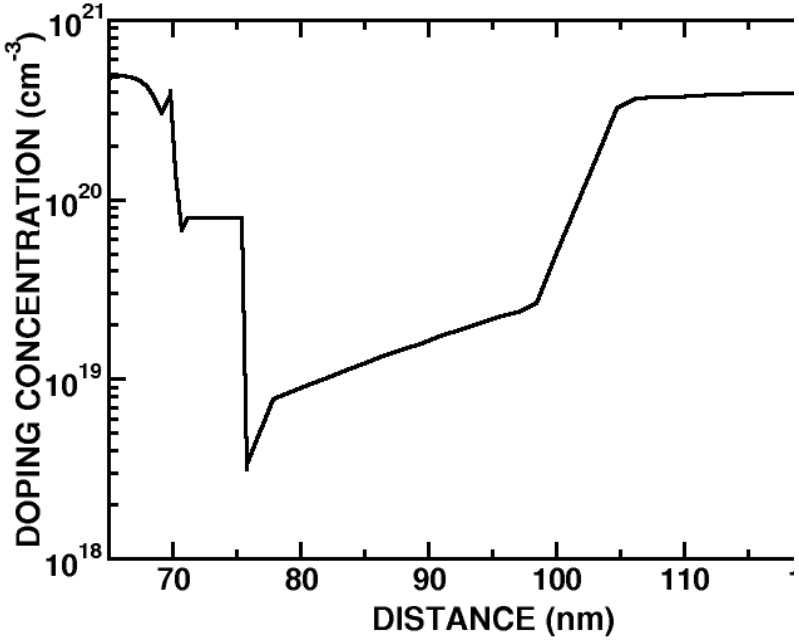
- Introduction
- SiGe HBT Scaling
- SERDES Performance Scaling
- Analog Applications
- Analog and Digital Signal Processing at mm-waves
- Mm-wave Radio and Radar

BiCMOS vs. CMOS Scaling

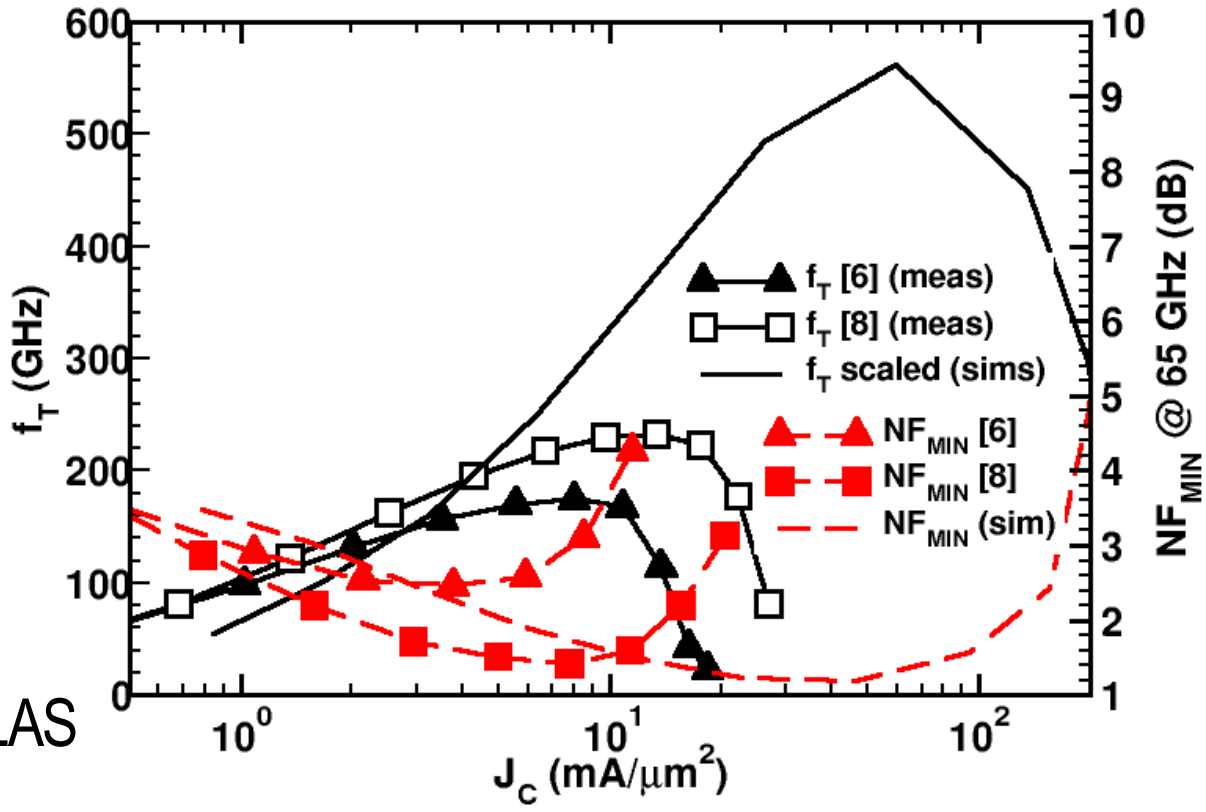


- SiGe HBT is typically 2 generation ahead of CMOS in speed
- Minimum feature size does not generally follow lithography scaling

Is the SiGe HBT Scalable to a New Generation?

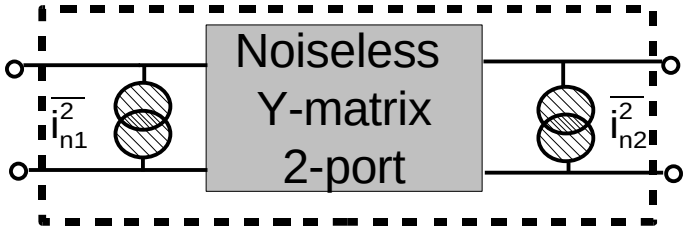


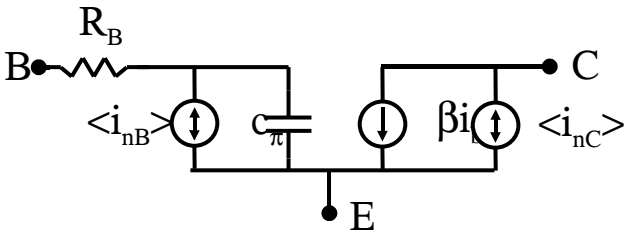
2-D process/device sims with ATLAS



- Scaling to 500 GHz is possible: W_E= 90 nm, W_B= 5 nm, W_C= 25 nm
- *NF_{MIN}* improves at 65 GHz and *J_{opt}* approaches *J_{pfT}*
- *J_{pfT}* exceeds 50 mA/μm^2 (scales by almost *S^2*)

Noise Correlation Fundamentals





$$R_n = \frac{\langle I_{n2}^2 \rangle}{4kT\,\Delta f\,|(y_{21})|^2}$$

$$\langle i_{nB} i_{nC}^* \rangle = 2qI_C[\exp(j\omega\tau_n) - 1]$$

$$G_u = \frac{\langle I_{n1}^2 \rangle}{4kT\,\Delta f} - \left| \frac{\langle I_{n1} I_{n2}^* \rangle}{4kT\,\Delta f\,R_n |Y_{21}|^2} \right|^2$$

$$G_{sopt} = \sqrt{\frac{G_u}{R_n} + G_{cor}^2}$$

$$Y_{cor} = y_{11} - \frac{\langle I_{n1} I_{n2}^* \rangle}{4kT\,\Delta f\,R_n\,y_{21}^*}$$

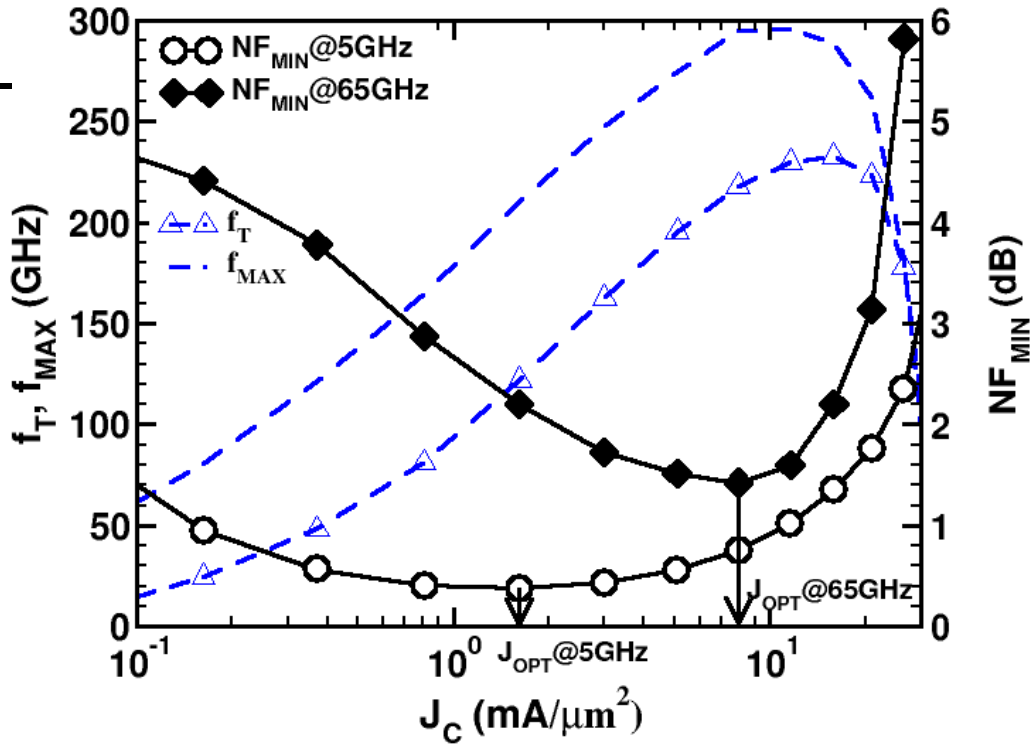
$$F_{MIN} = 1 + 2R_n(G_{cor} + G_{sopt})$$

G_u, G_{sopt} decrease with correlation, R_{sopt} increases

F_{MIN} decreases with correlation

Issues Related to Noise Correlation

- J_{OPT} increases due to correlation
- Larger I_C needed to noise match to 50 Ω
- Neither trend is captured by commercial HBT models
- Noise parameter measurements at mm-waves are "noisy" and a physical τ_n is difficult to extract.
- HBT noise params with correlation can be extracted from S/Y-params (K.Yau et al. SiRF-06)



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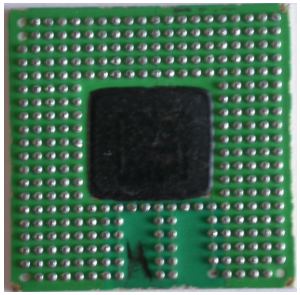
100-Gb/s Ethernet Transceiver

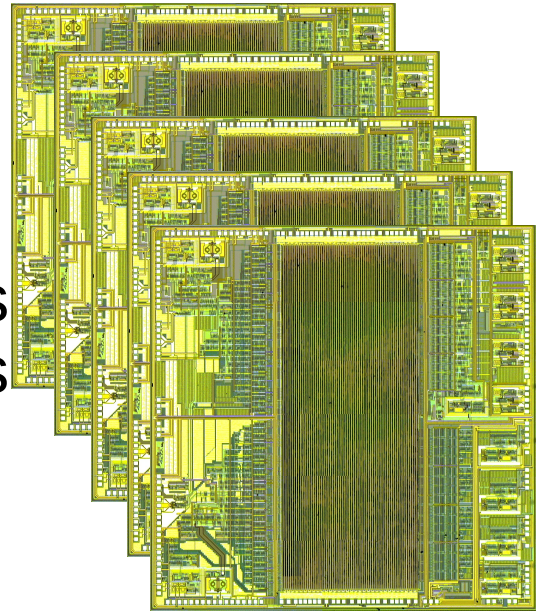
100 Gb/s

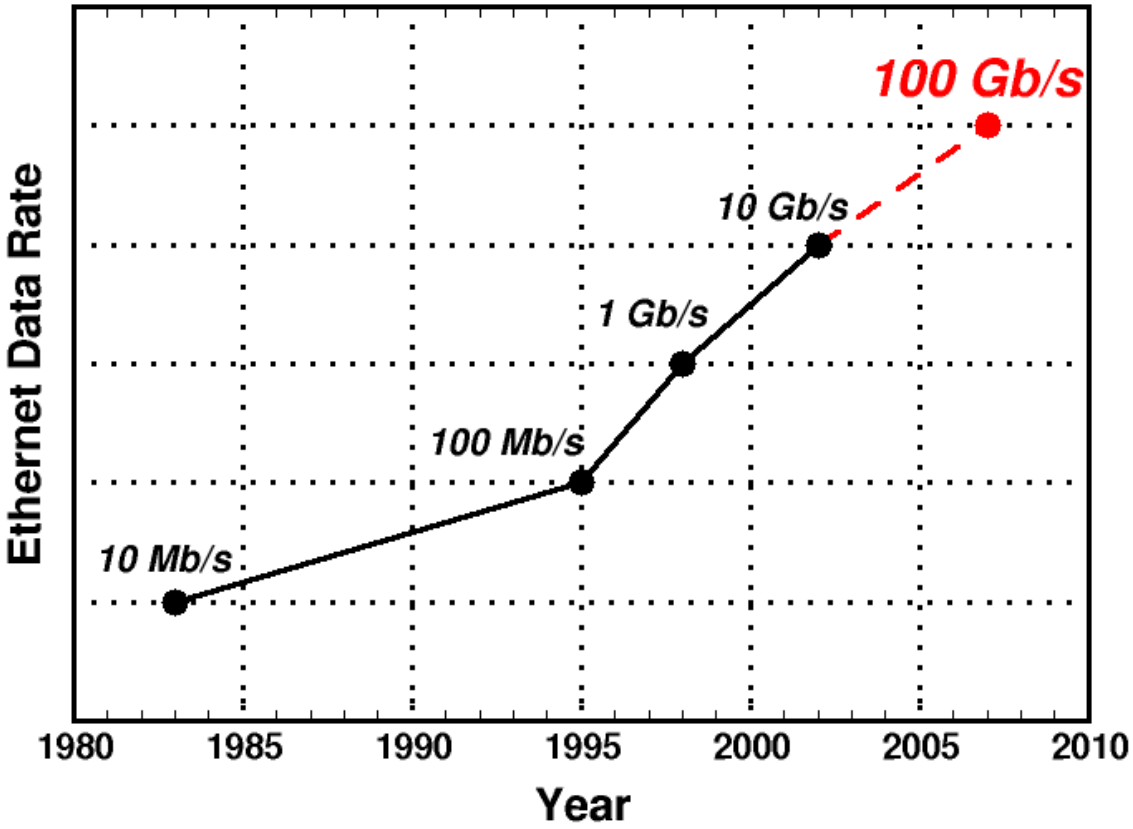


should consume less power and cost less than

3W, $250

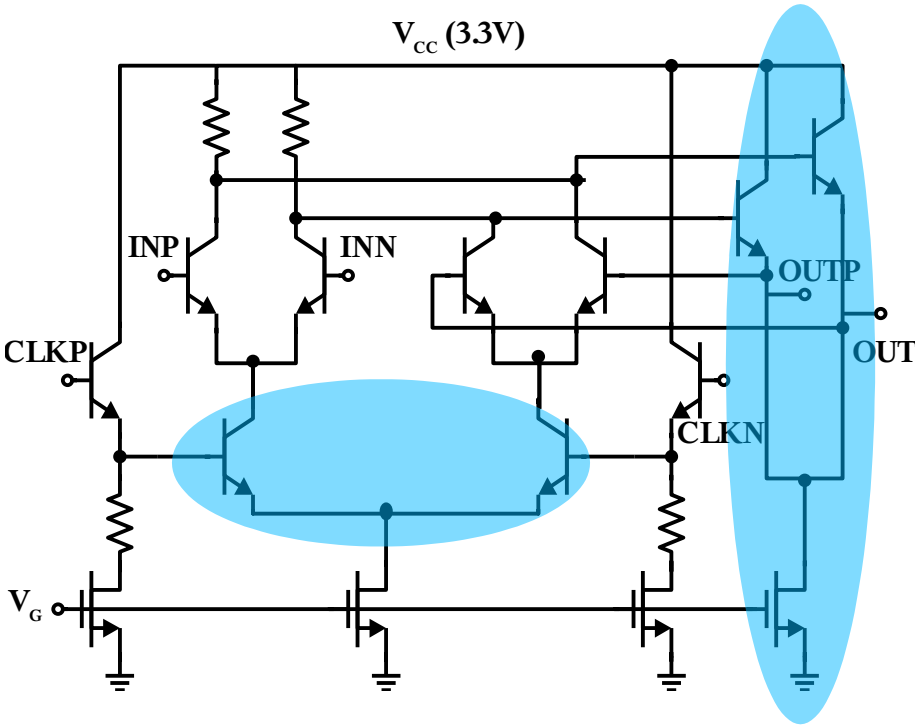
5 x 10 Gb/s
2 x 40 Gb/s

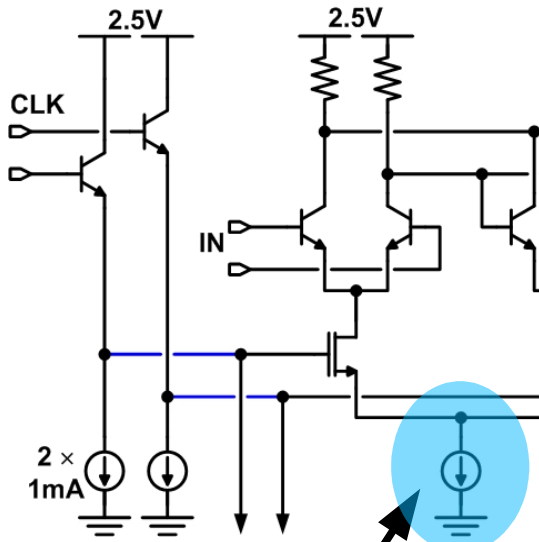




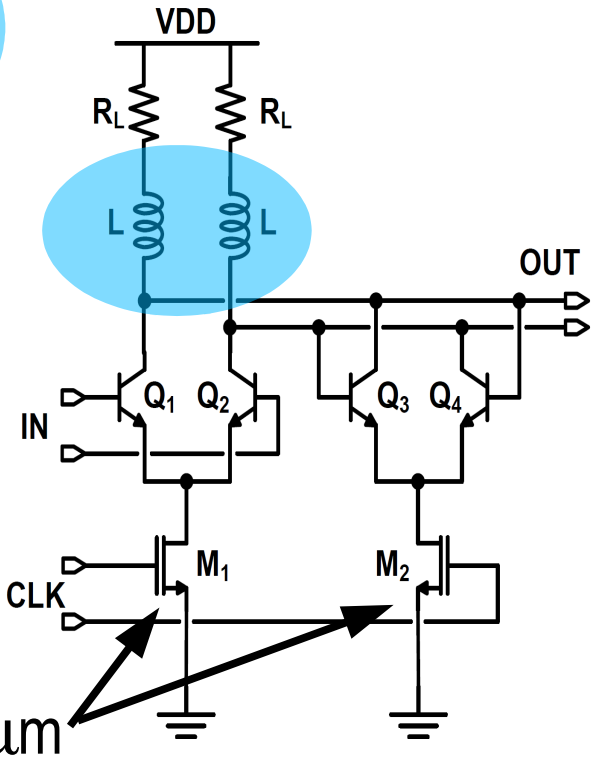
- 10 GE CMOS transceiver dissipates 0.8W from 1.2 V and costs < $50
- 40+ Gb/s SiGe-HBT ICs too power hungry and 3.3V supply
- Need lower supply logic with fewer and lower tail currents per gate

High-Speed, Low-Power Latch (E. Laskin JSSC-Oct. 06)





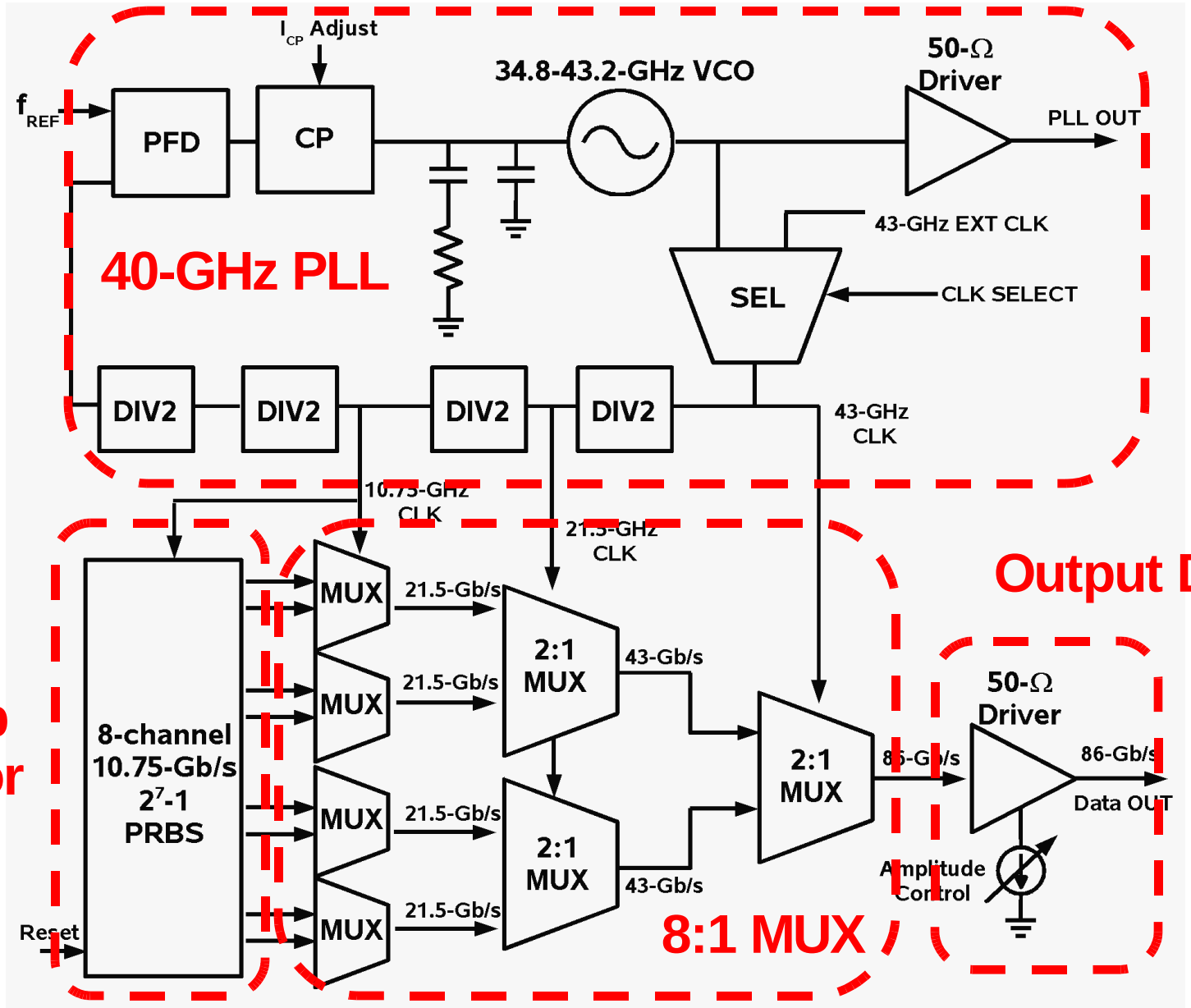
0.3 mA/μm



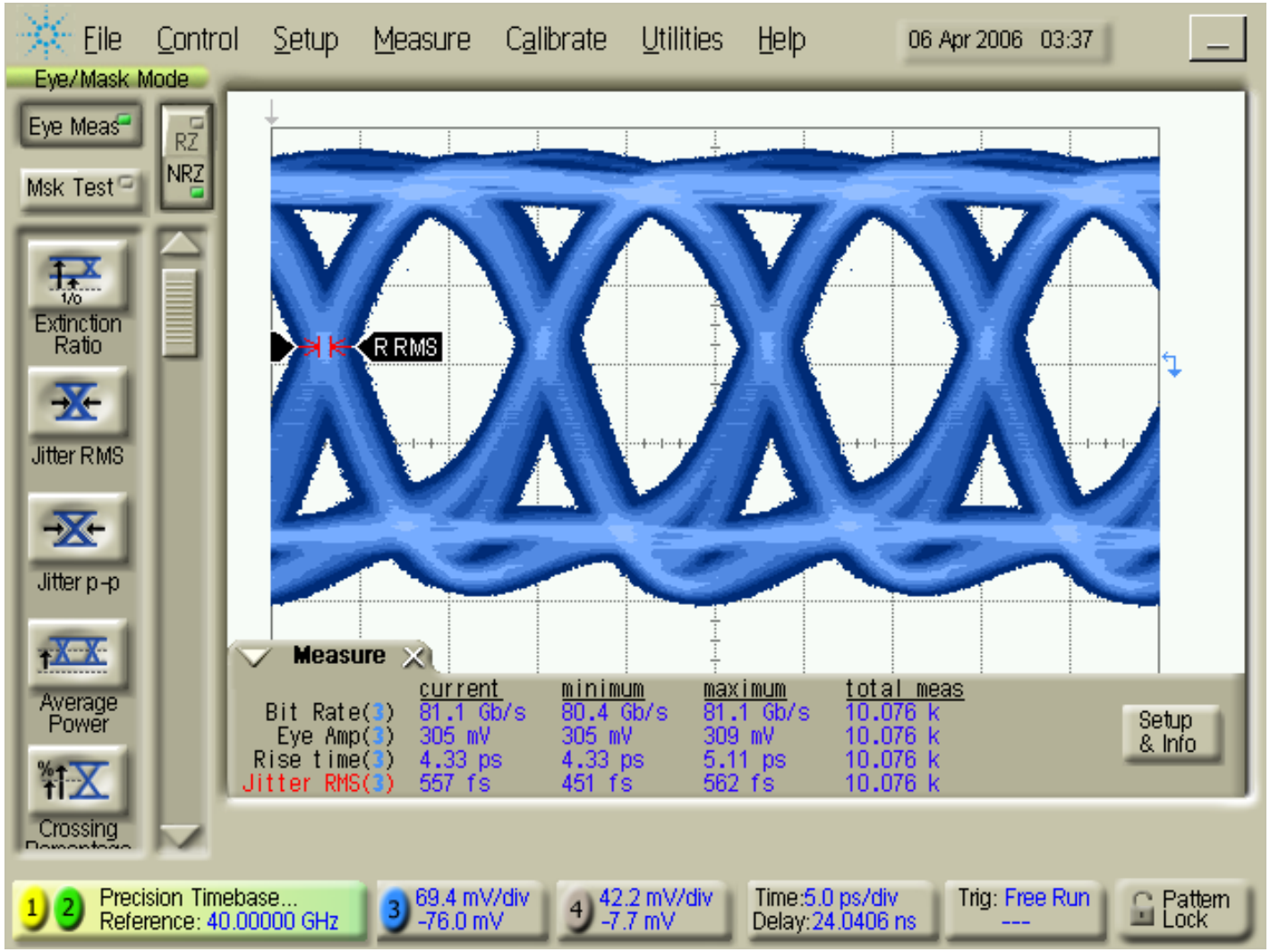
0.15 mA/μm

- HBT ECL to BiCMOS CML
- 3.3 V to 2.5 V and reduced number of tails
- 1.8 V (lower power) at same speed
- Inductive peaking to increase speed

2.5-V, 1.4-W, 80-Gb/sTransmitter (T.Dickson et al. CSICS-06)



Measured Results: 80-Gb/s



- Running for more than 1 hour continuously in the lab.
- Jitter: 560 fs (rms) , Rise/fall time: 4-5 ps, Amplitude: 300 mV_{pp} per side

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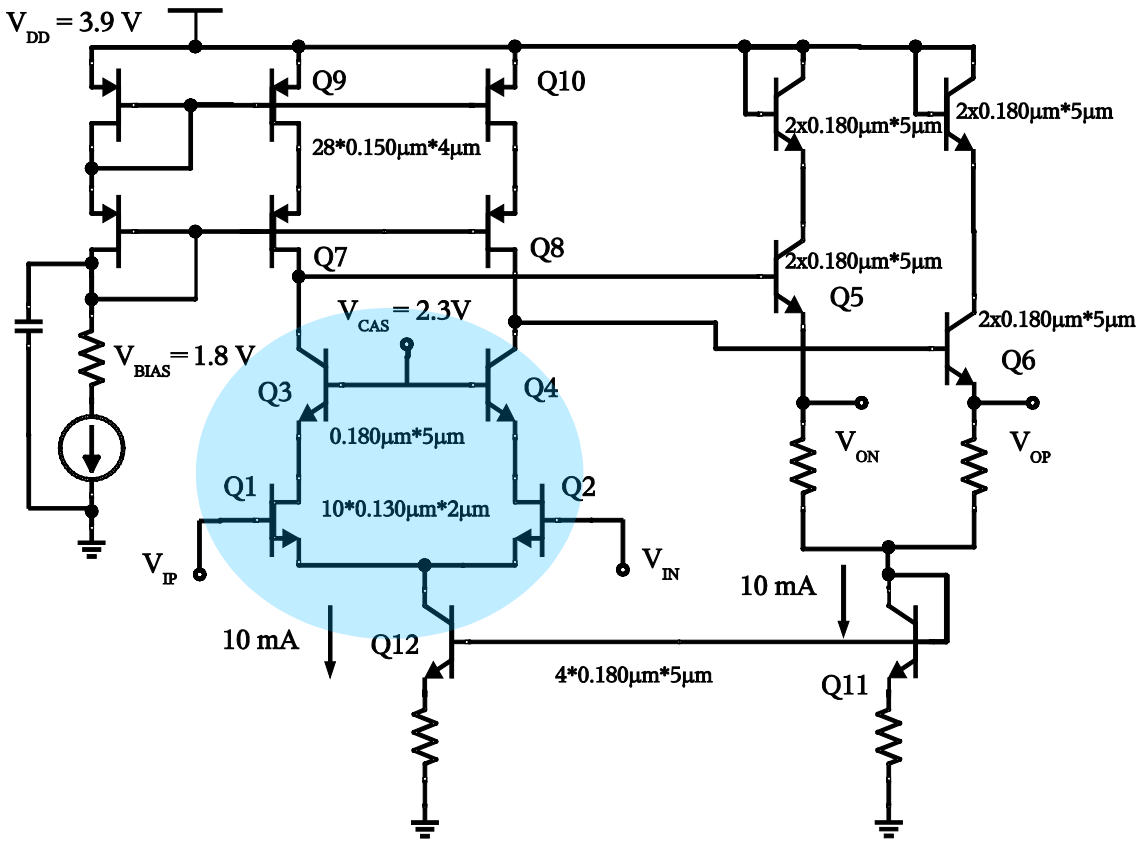
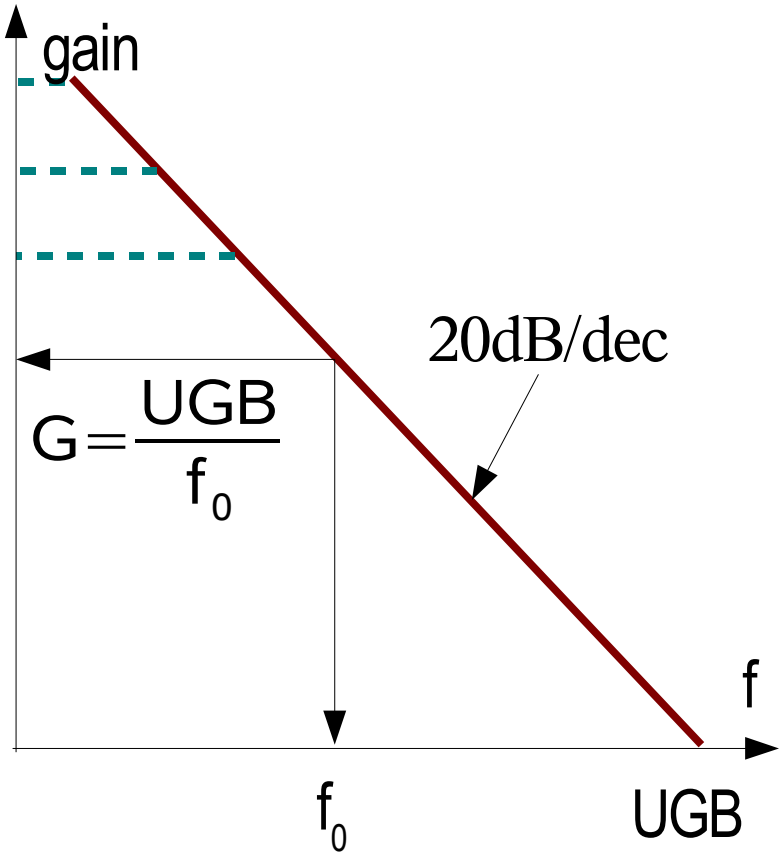
High Unity-Gain-Bandwidth Opamps (S. Voinigescu et al. CSICS-05)



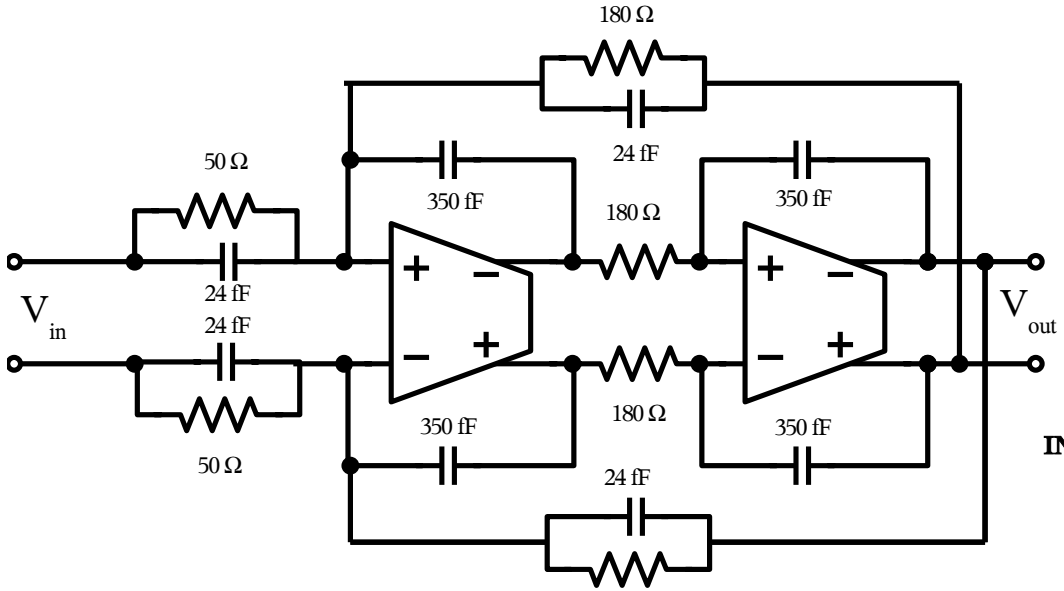


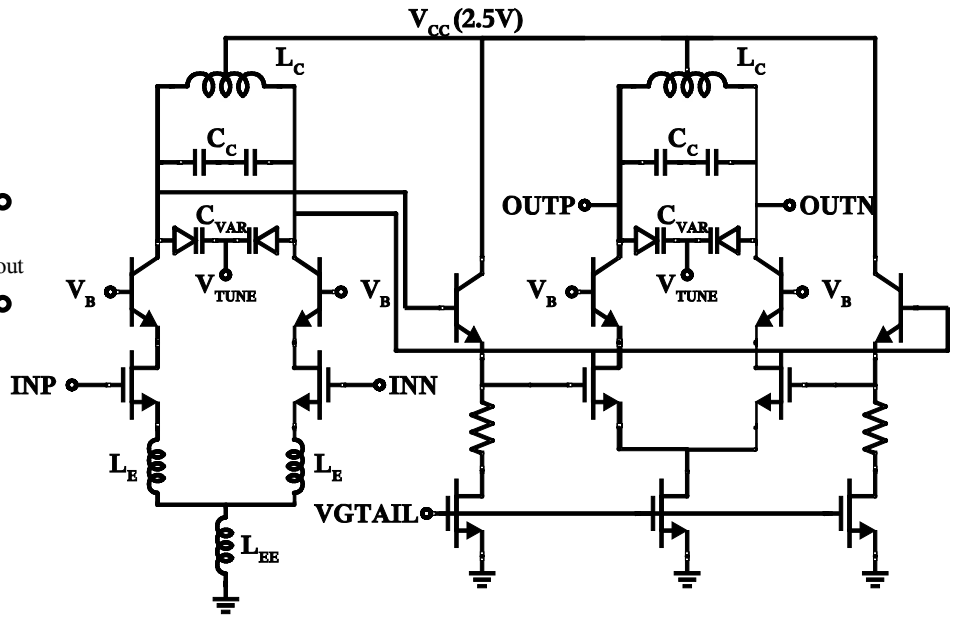
- MOS-HBT cascode ensures single-pole function, unconditional stability
- UGB dictated by f_T of HBT: 37 GHz with 160-GHz f_T HBT
- UGB, filter gain at f_0 insensitive to bias current/voltage and LF OpAmp gain variation

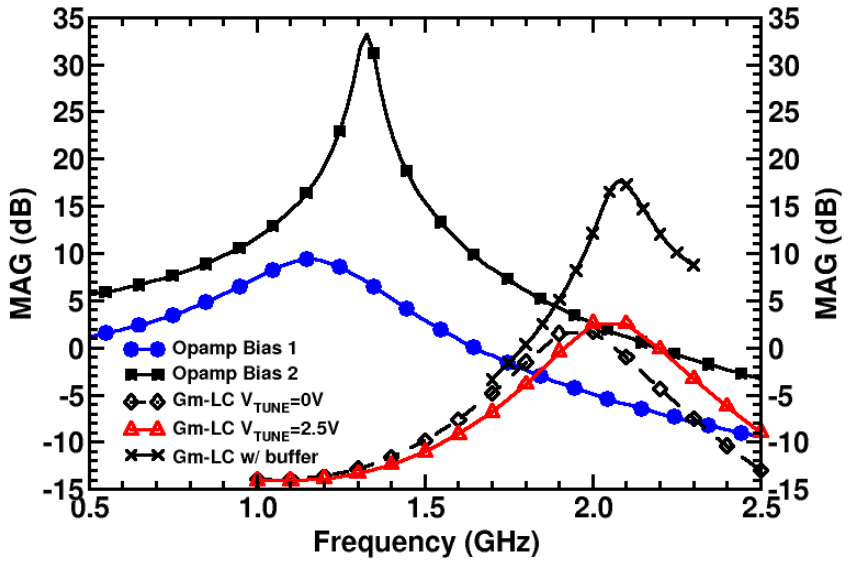
OpAmp vs. gm-LC filter

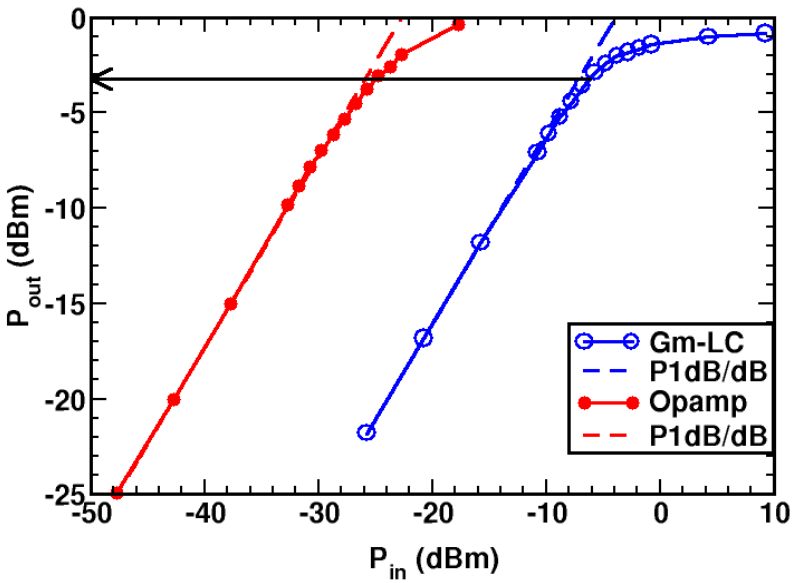
10 x smaller area

similar power dissipation









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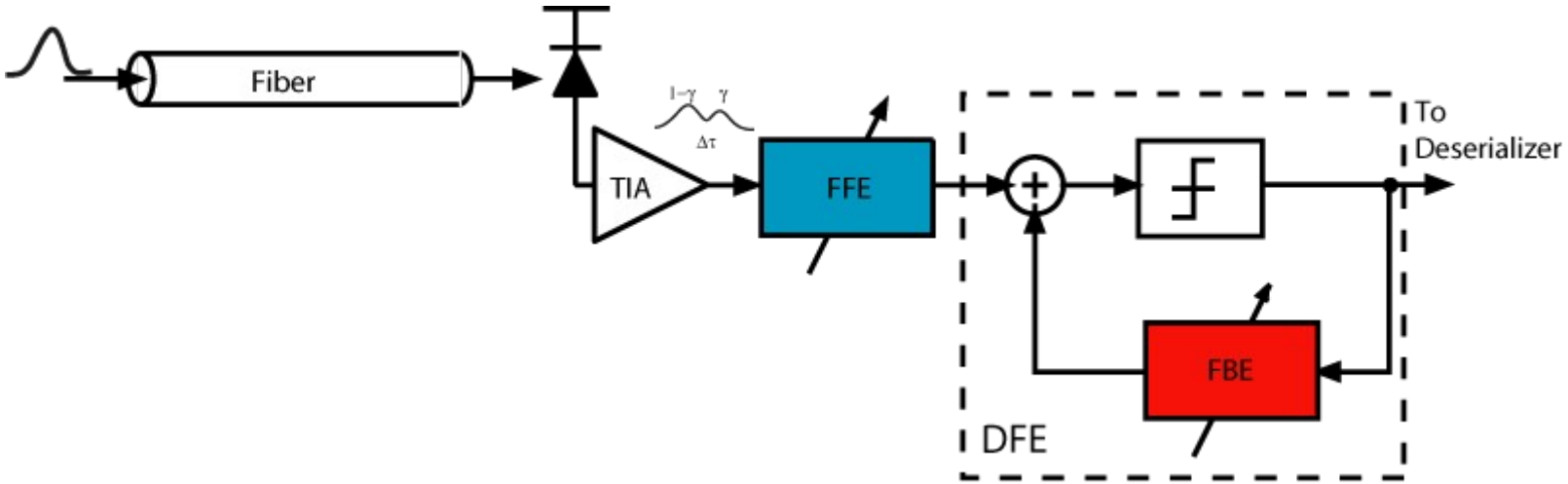
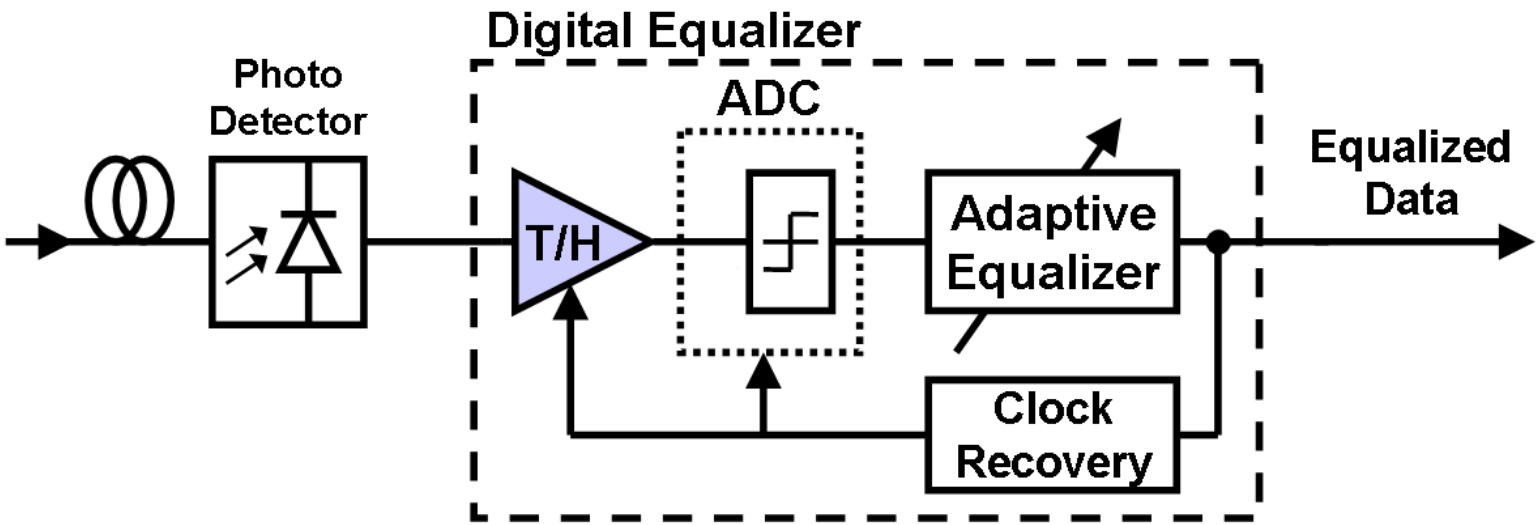
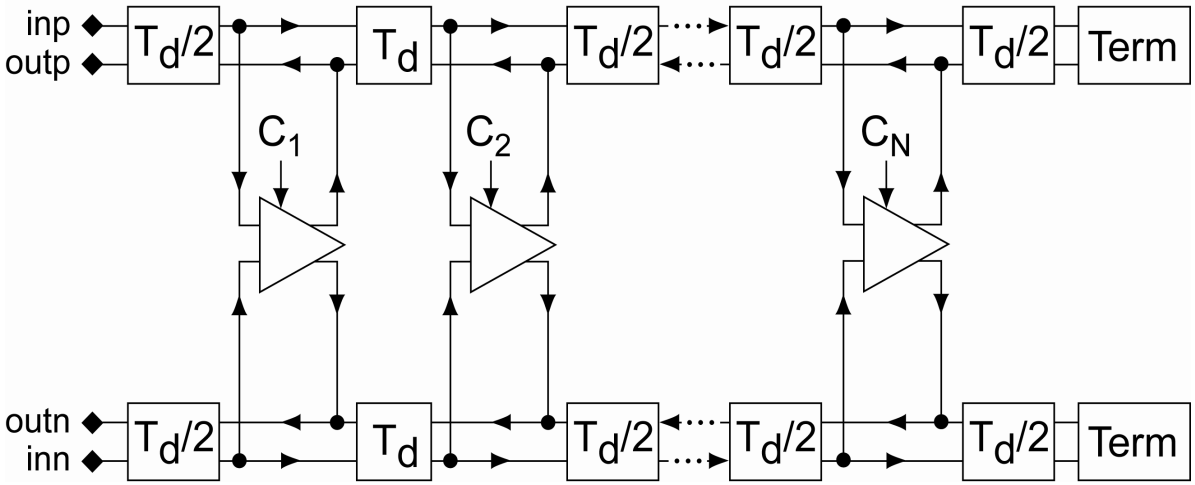
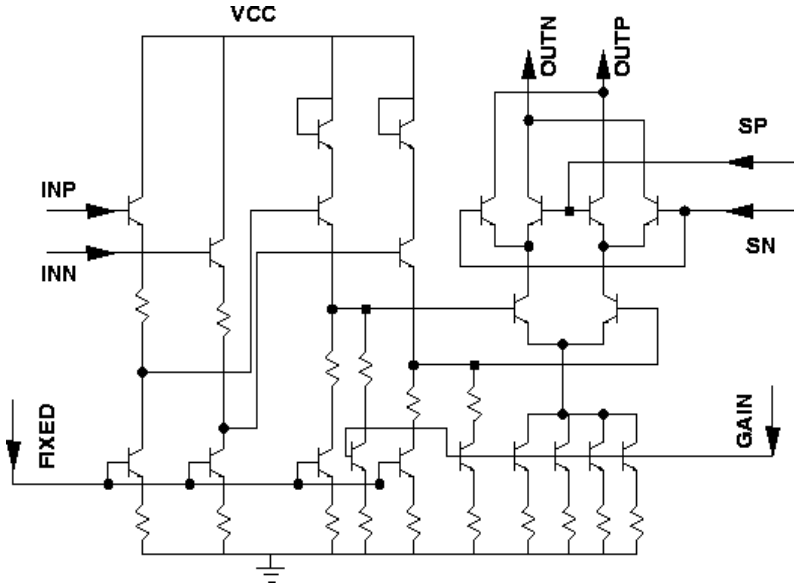
Analog and Digital Equalization at 40 Gb/s

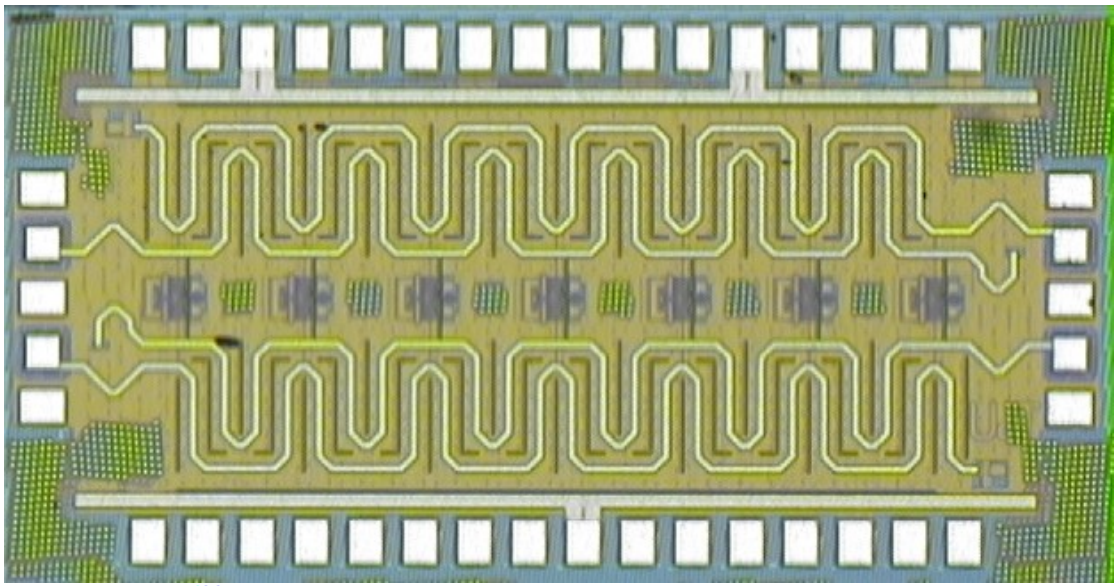




40 Gb/s Feed Forward Equalizer (A. Hazneci et al. CSICS-04)

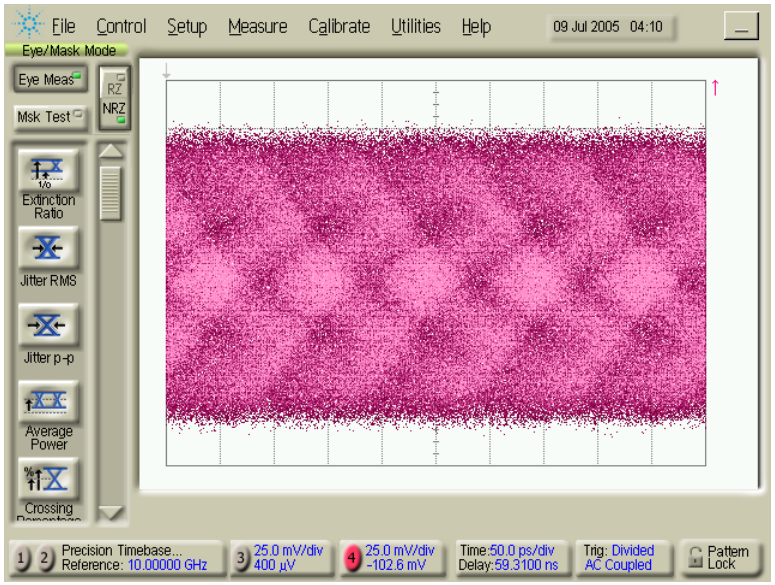


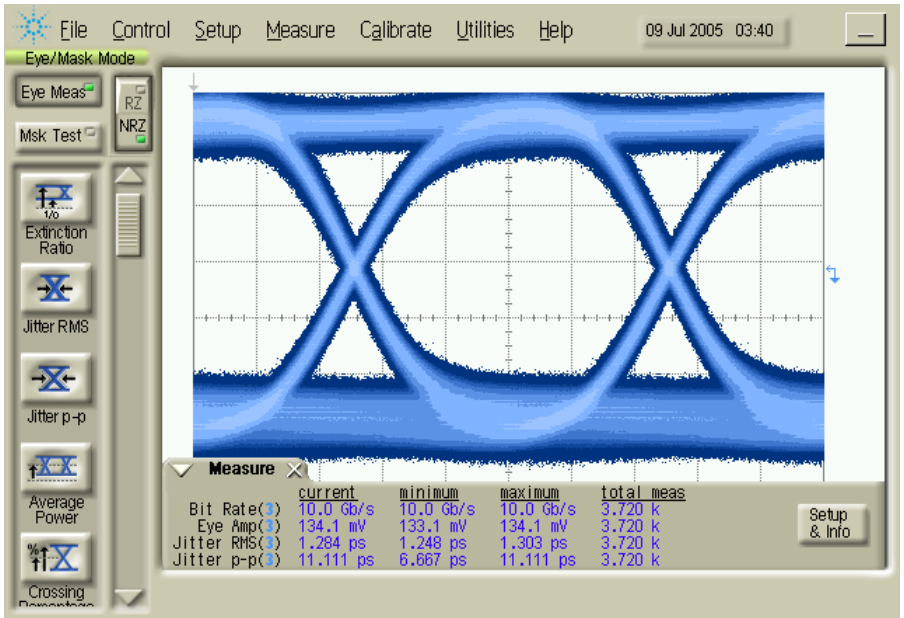


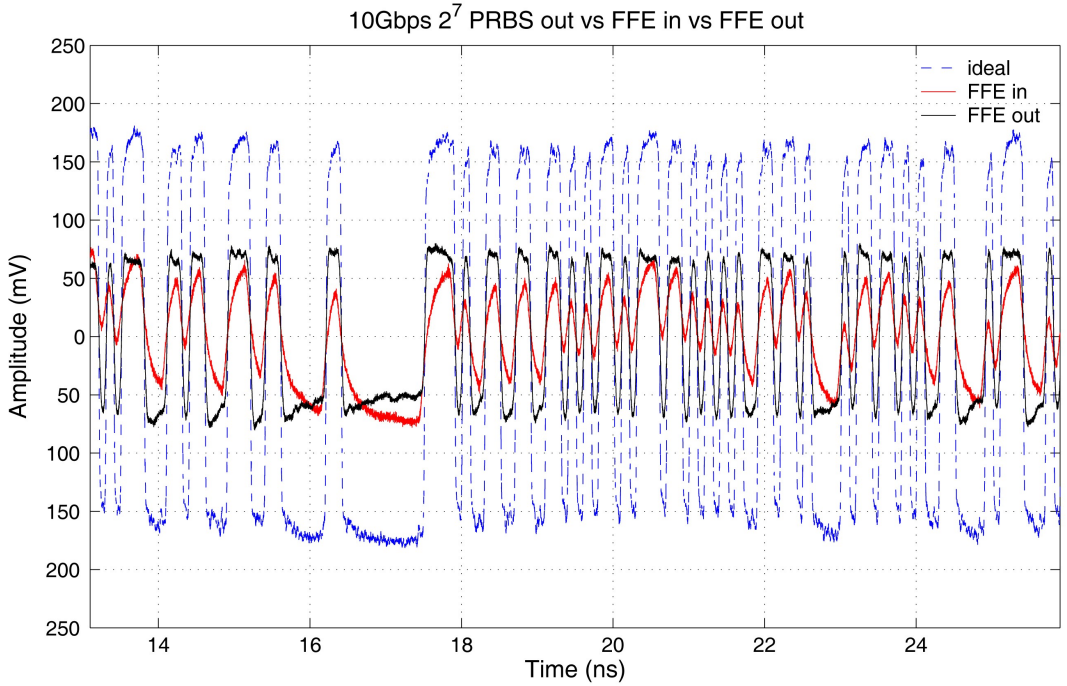


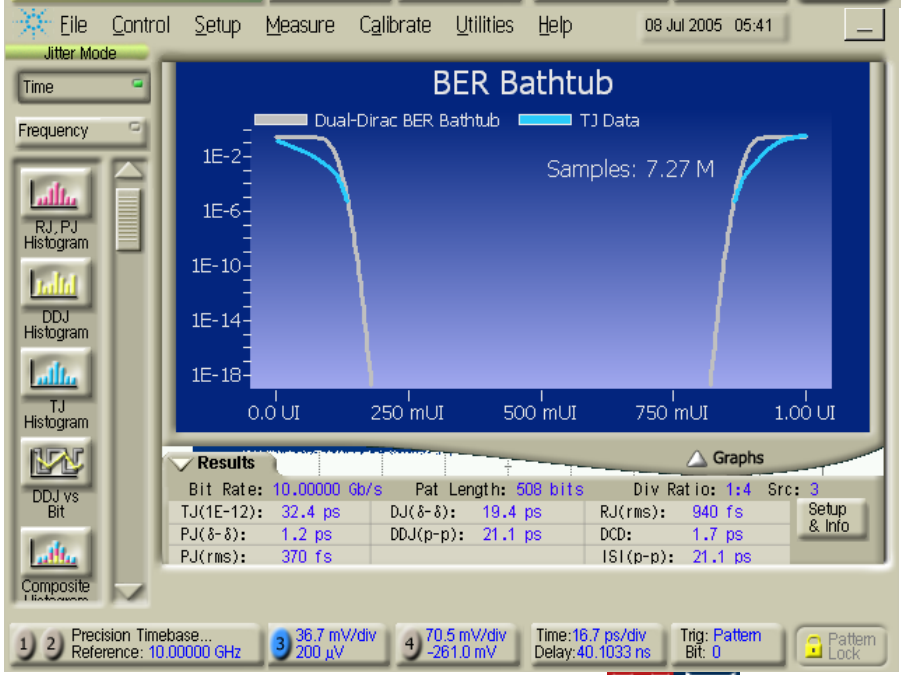
- core of each gain stage is a Gilbert cell
- tail current of the differential pair controls the tap weight (GAIN pad)
- SP/N pads control the tap sign

10 Gb/s Equalization over 24-ft SMA cable +6dB attn.

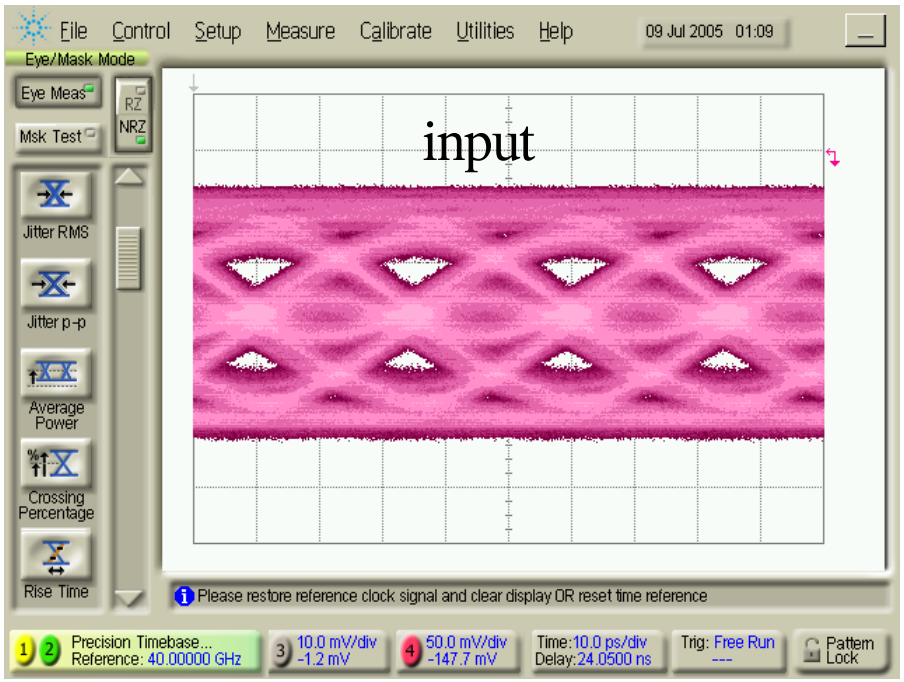


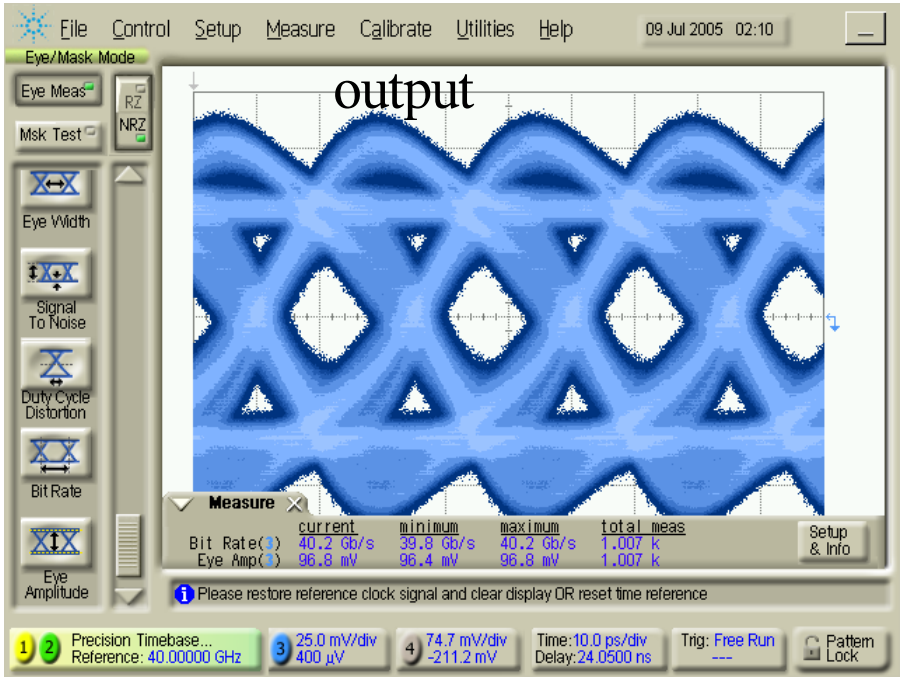


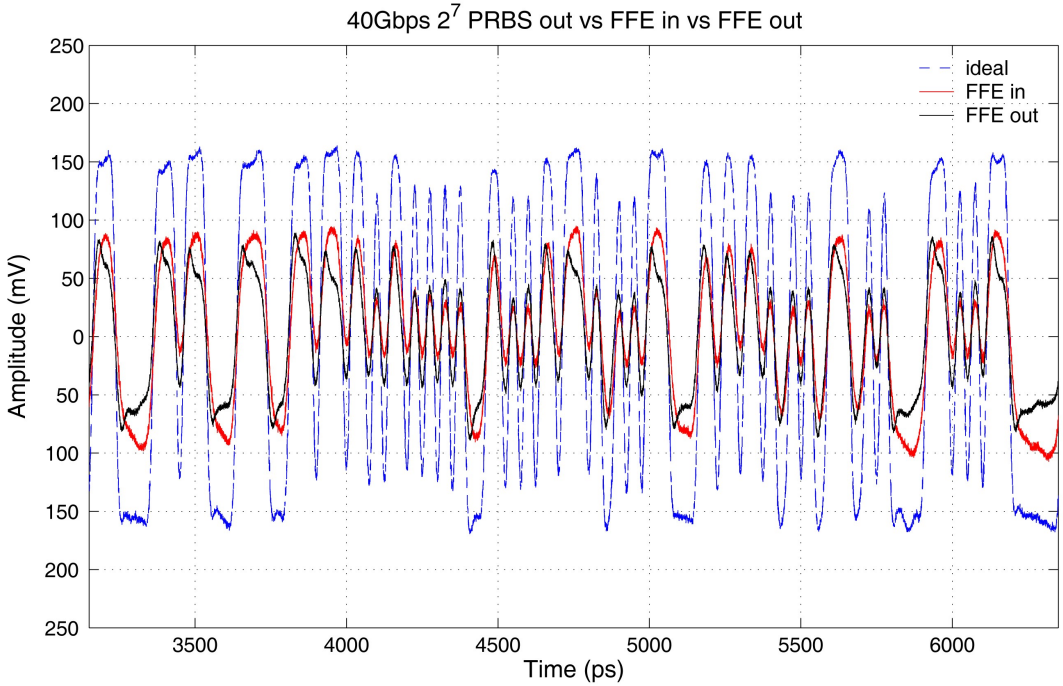


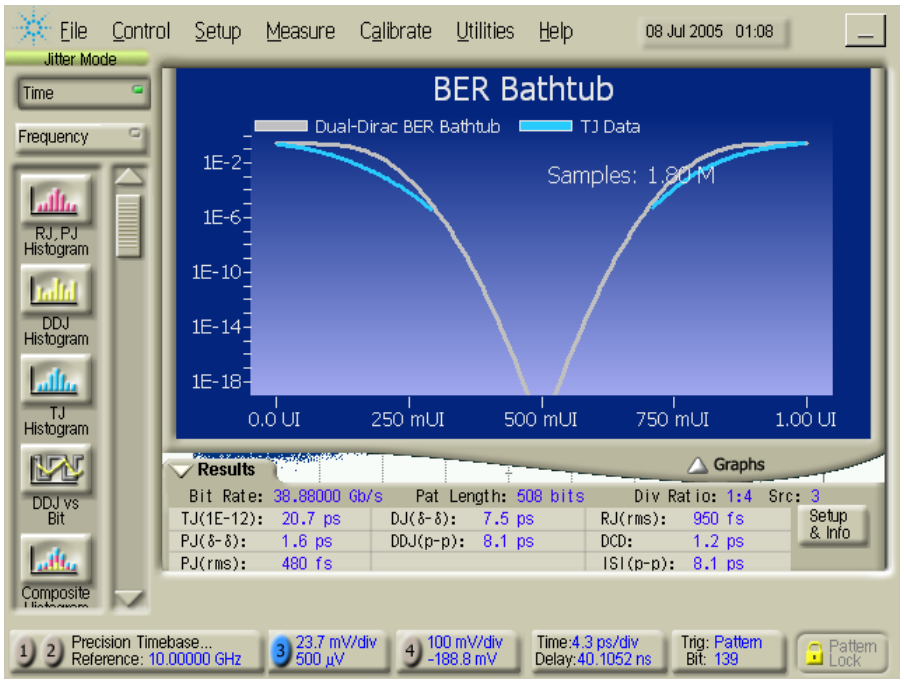


40 Gb/s over 9-ft SMA cable + 3dB attn.

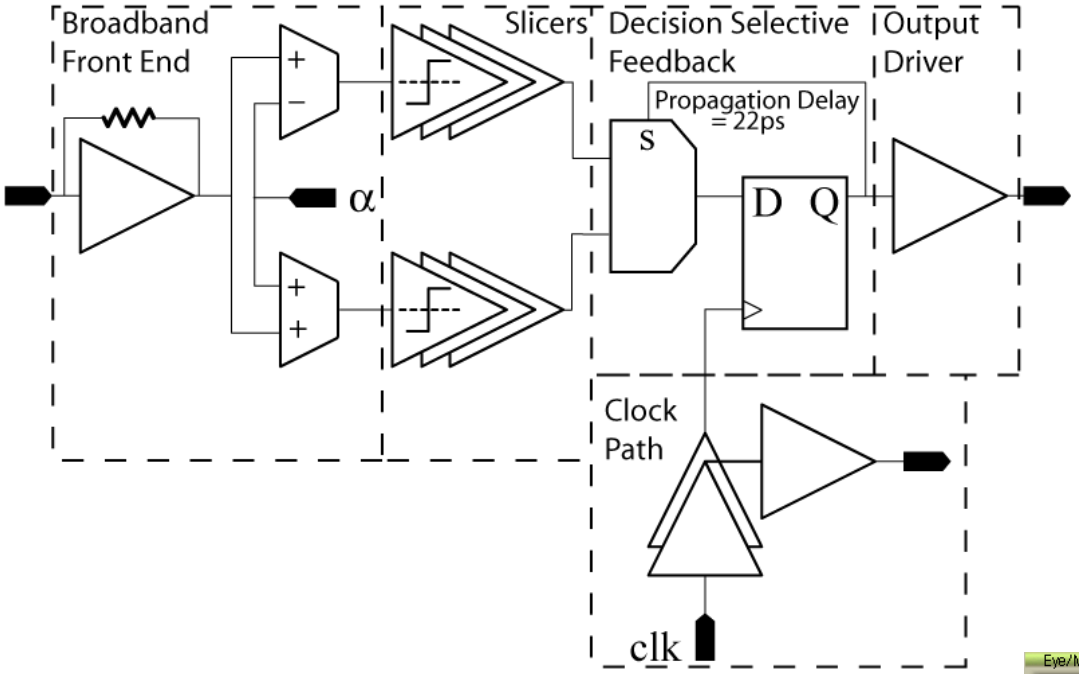


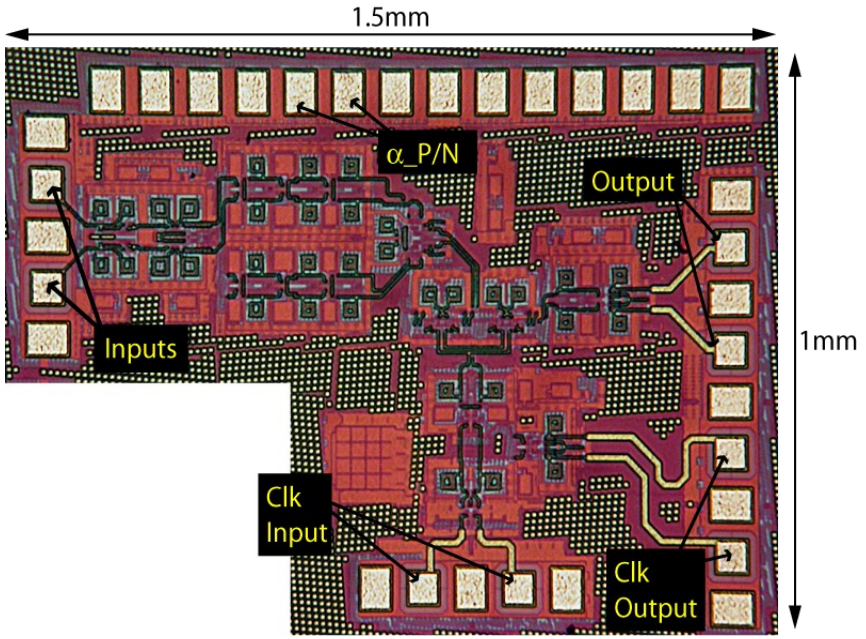


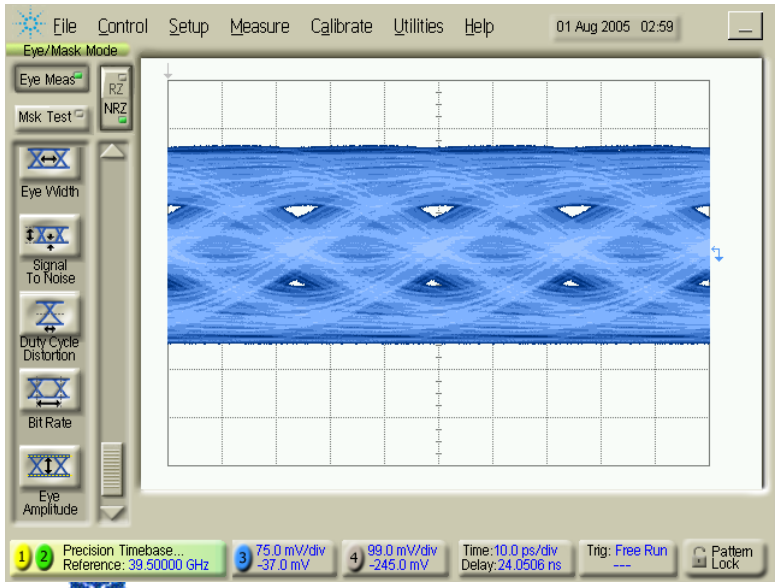




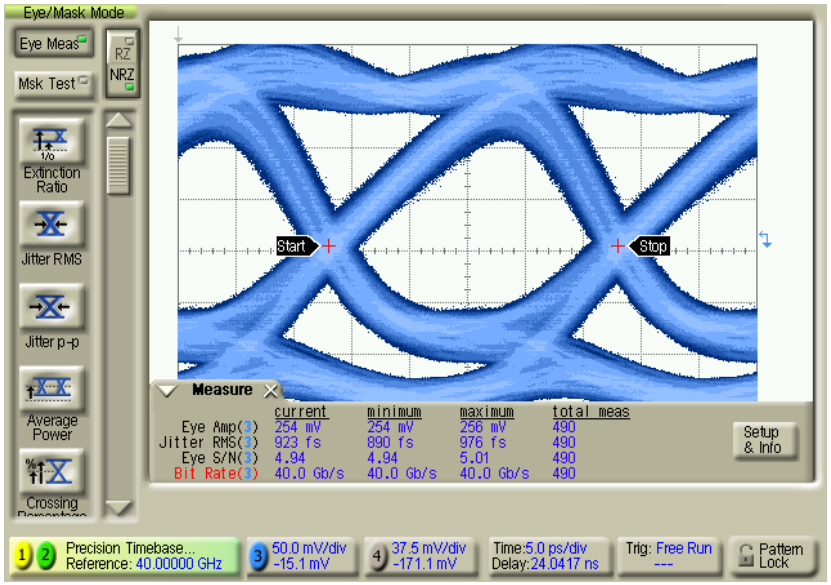
1-Tap, 40 Gb/s DFE (A. Garg et al. JSSC Oct.-06)





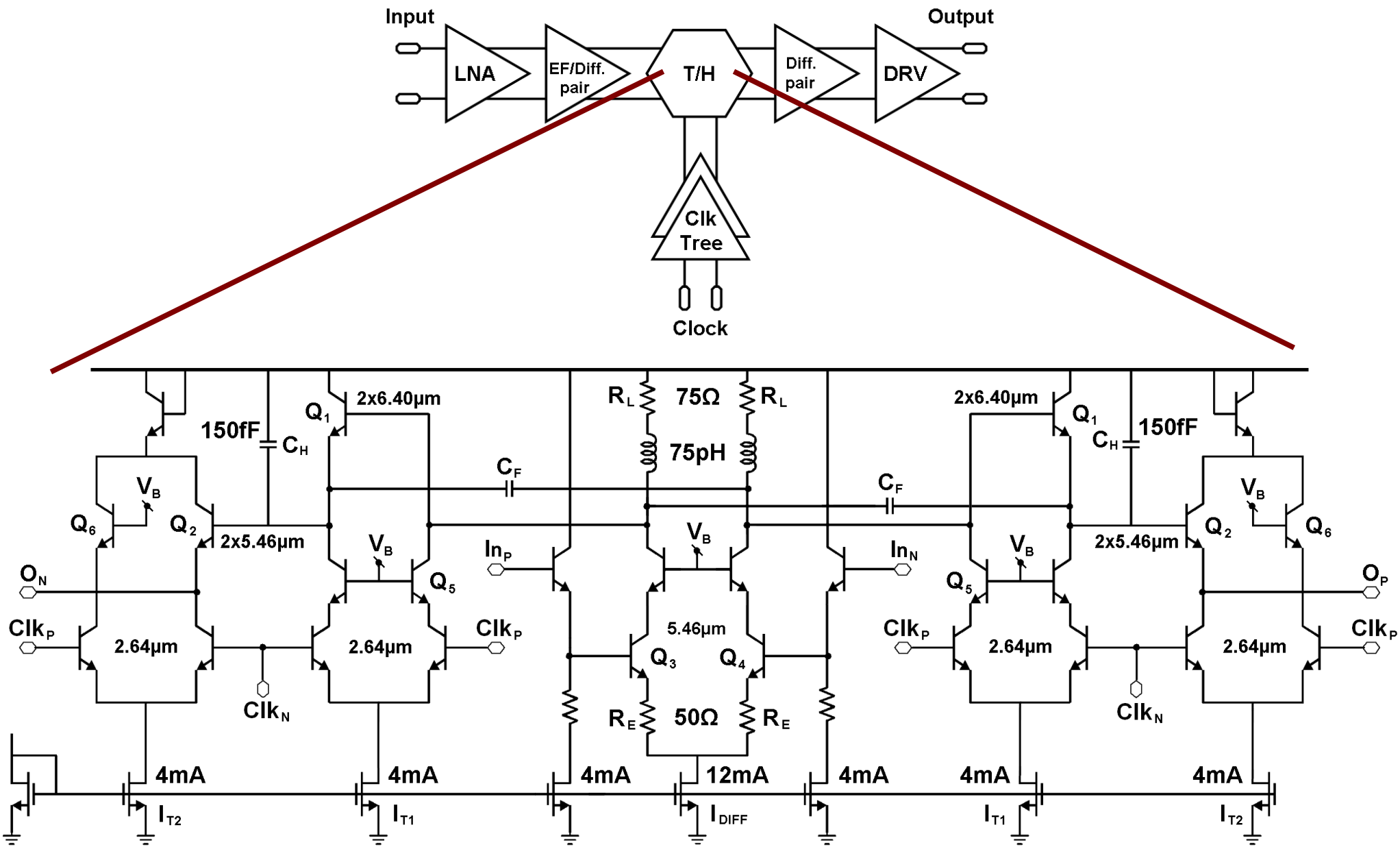


39.5 Gb/s input

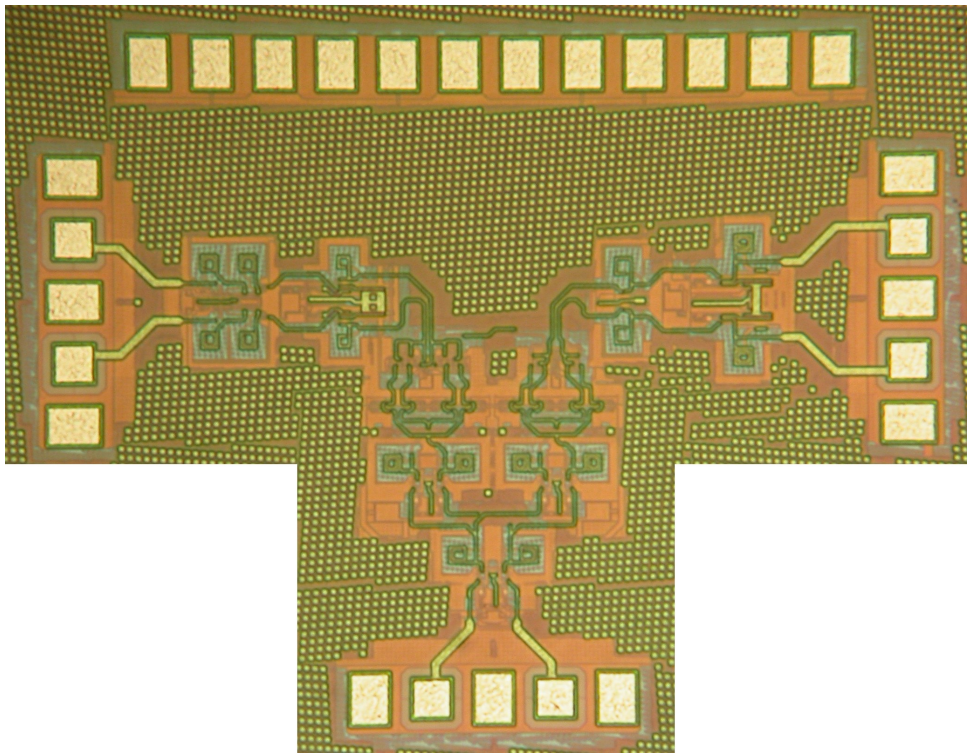


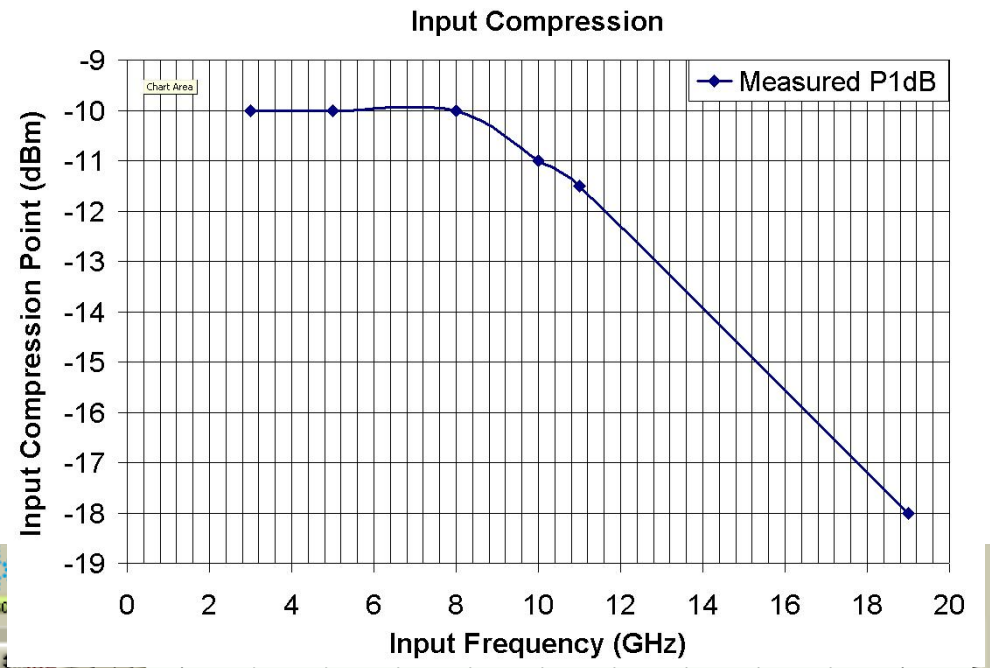
39.5 Gb/s output

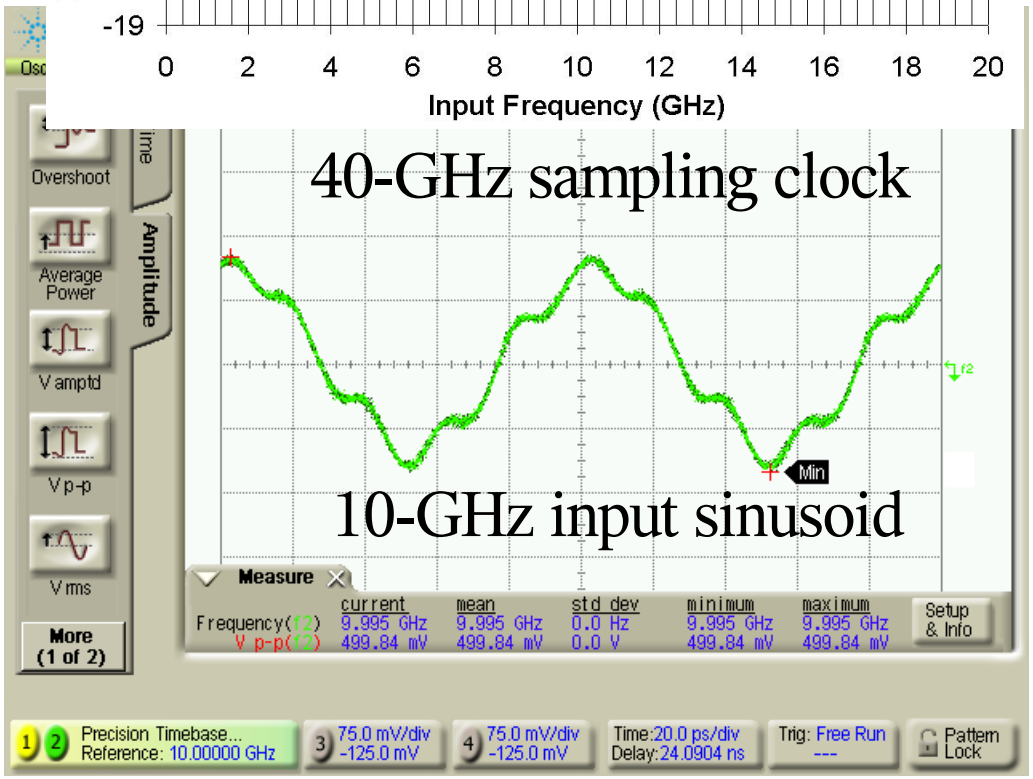
40-GS/s T/H Amplifier (S. Shahramian et al. JSSC Oct.-06)



40-GS/s T/H Amplifier Measurements

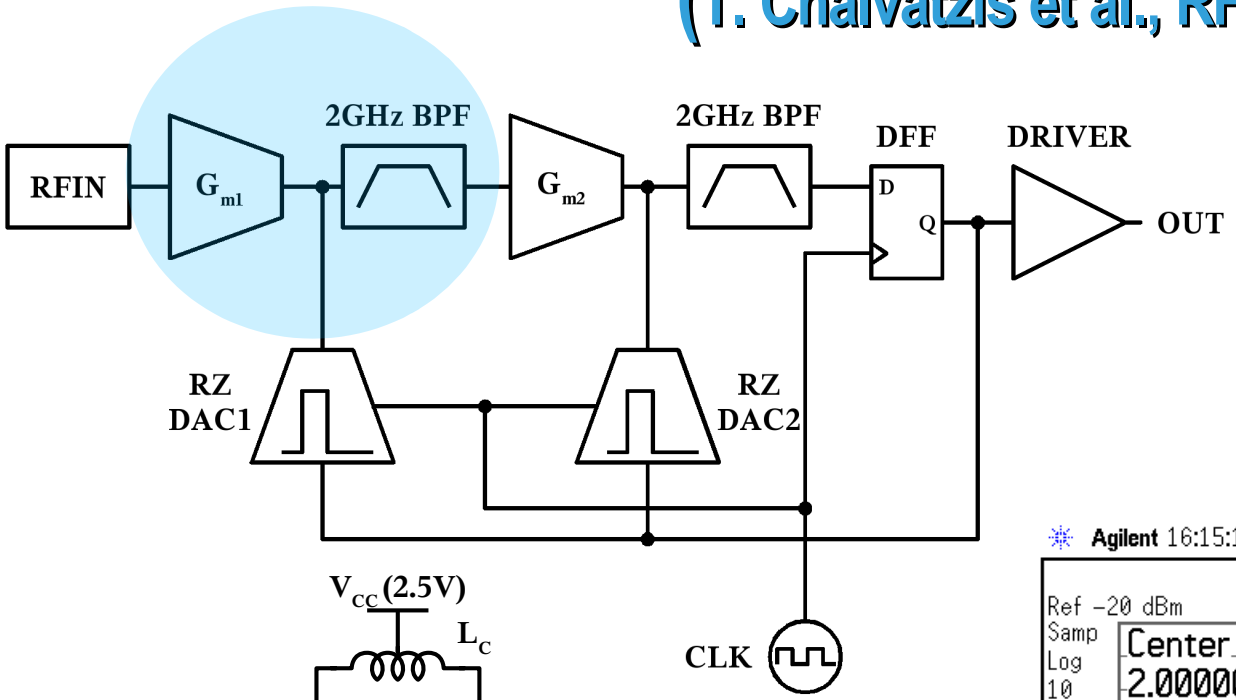


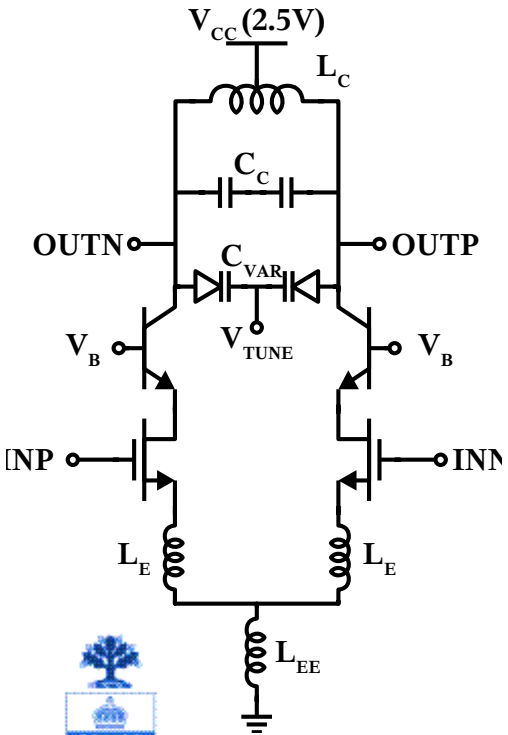




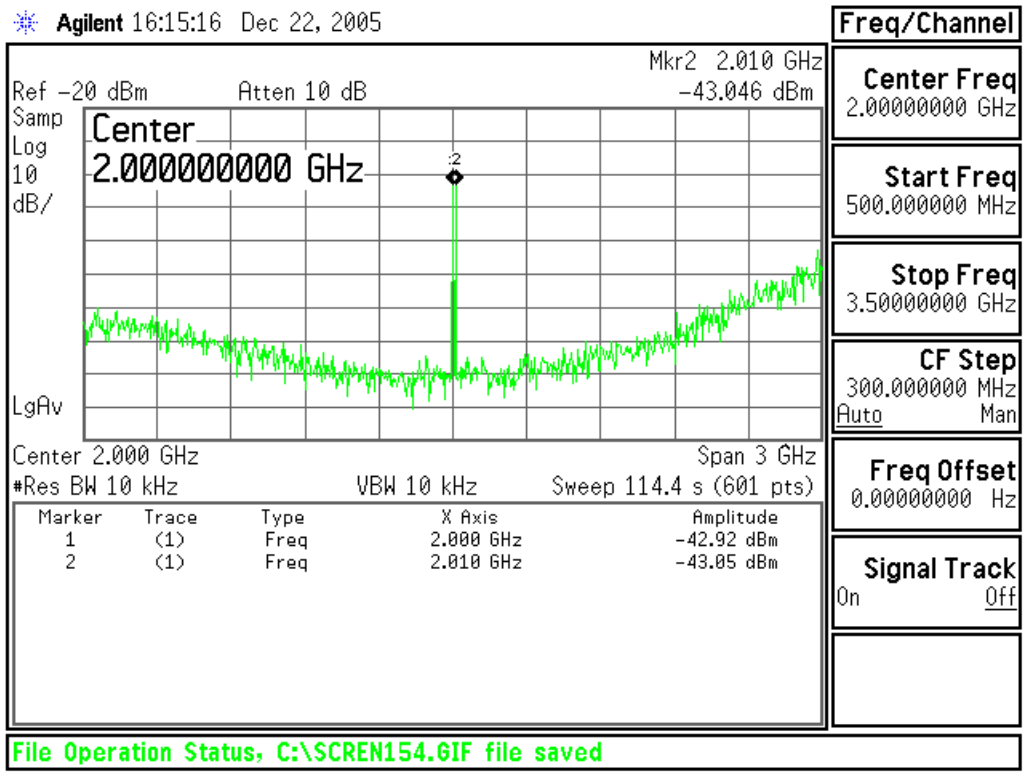
40 GS/s, Bandpass ΔΣ ADC Centred at 2-GHz

(T. Chalvatzis et al., RFIC-06)





- BiCMOS cascode in g_m-LC_{var} filter for linearity, noise
- BiCMOS ECL quantizer and DACs for speed and metastability



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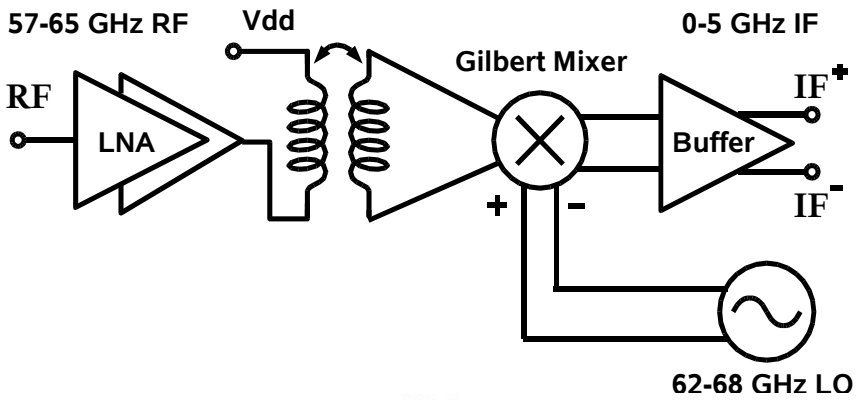
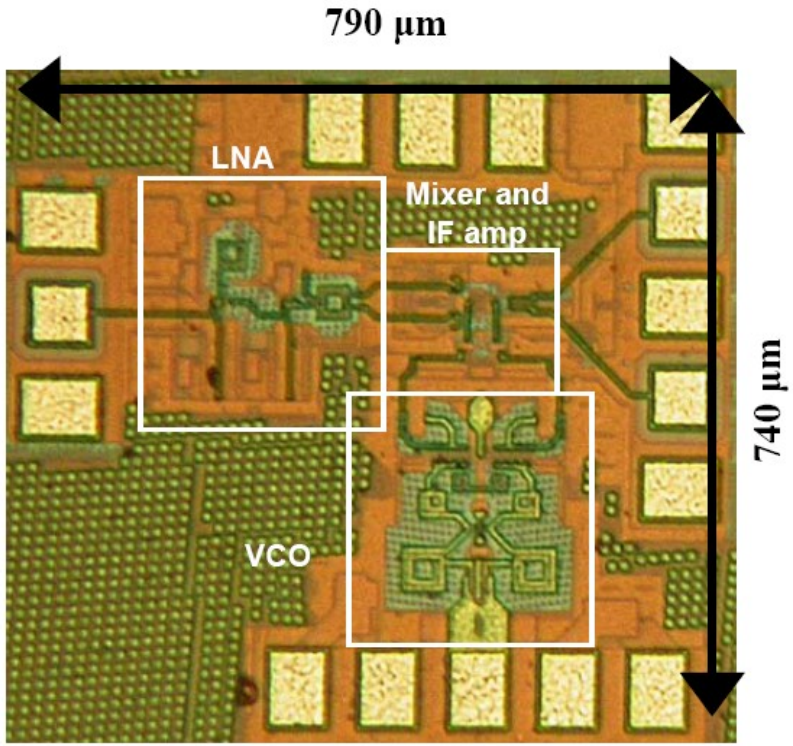
65-GHz SiGe BiCMOS Receiver (M.Gordon et al. SiRF-06)





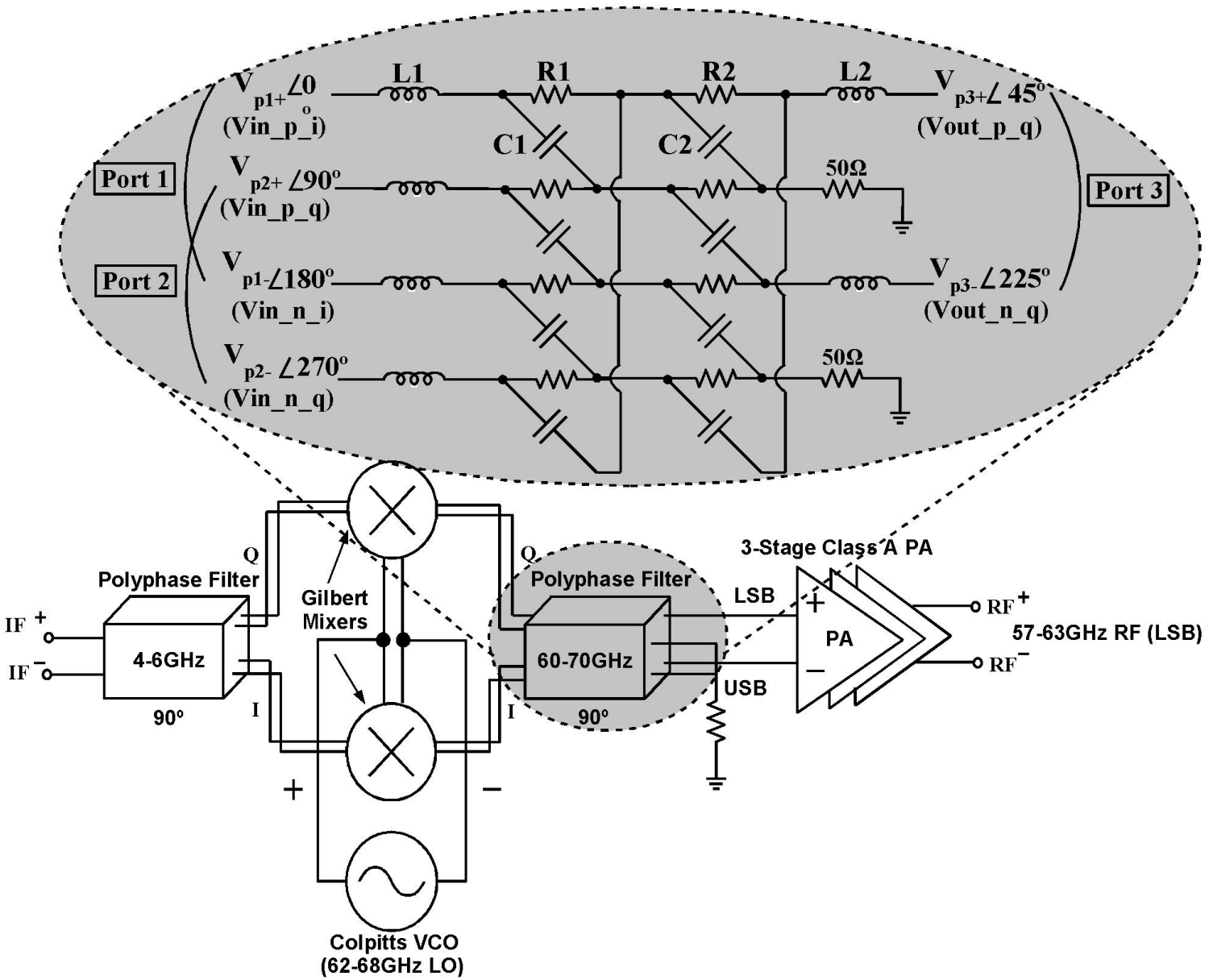
- First 65-GHz receiver in silicon to integrate VCO
  - Total power is 540 mW
- LNA + Mixer = 80 mW
- VCO + Buffer = 360 mW
- IF Amp = 100 mW
  - Core is 550µm x 440µm
- Compact passives
- Tight layout important to reduce parasitics at 65 GHz

Comparison with State-of-the-Art Receivers

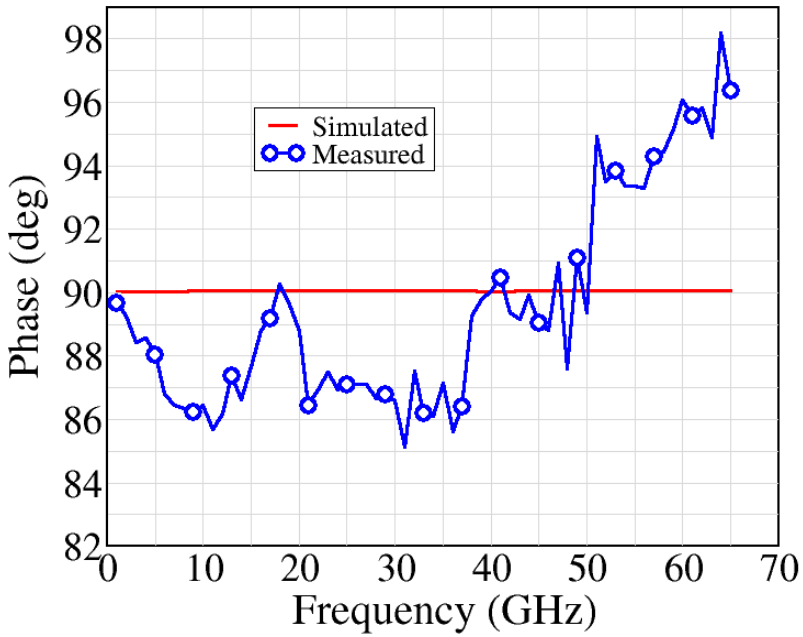
Table 1. Comparison of 60-65 GHz Receivers

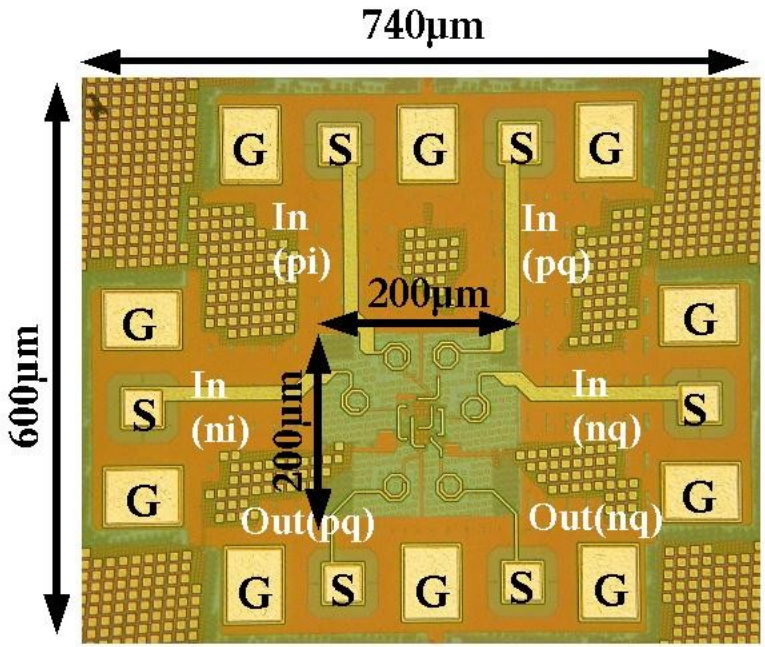
Technology	0.18µm SiGe BiCMOS	0.13µm CMOS	0.13µm SiGe BiCMOS	0.09µm CMOS
Frequency	65 GHz	60 GHz	60 GHz	60 GHz
Integration Level	LNA, mixer, VCO, IF amplifier	LNA, mixer, IF buffer	LNA, superheterodyne receiver, BB amplifier	LNA, mixer, LO and IF buffer
Power Gain	24 dB	28 dB [V/V]	40 dB	16 dB
NF_{MIN}	12 dB	12.5 dB	5 dB	6 dB
P_{1dB}	-22 dBm	-22.5 dBm	-36 dBm	-21 dBm
P_{diss}	540 mW	9 mW (excluding IF buffer)	195 mW	60 mW
Isolation	--	--	< -77 dB	< -90 dB
Area	0.79x0.74 mm^2	0.4x0.3 mm^2 (core area)	3.4x1.7 mm^2	0.6x0.48 mm^2
Reference	U of T- SiRF06	Razavi ISSCC-05	IBM ISSCC-06	U of T - CSICS-06

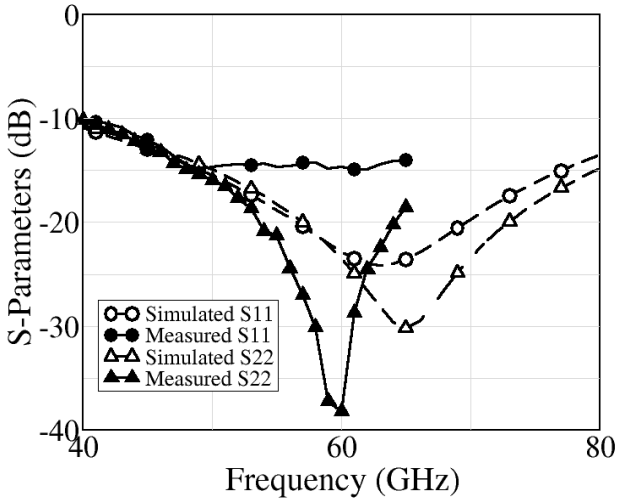
60-GHz Single-Sideband Transmitter

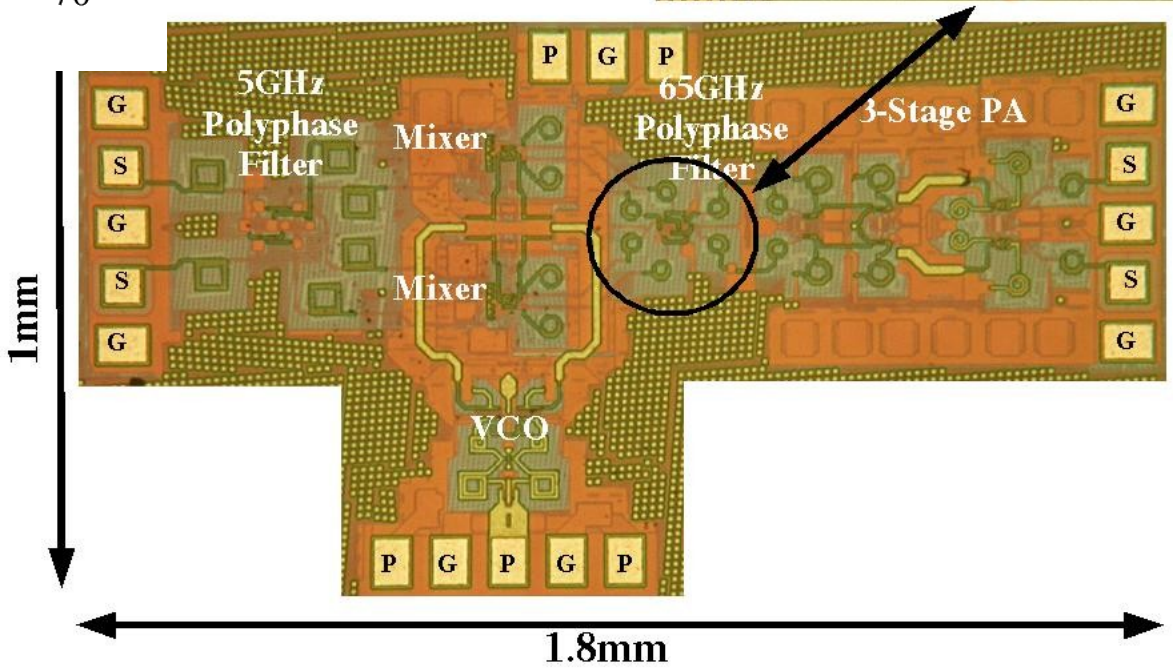


60-GHz Polyphase Filter

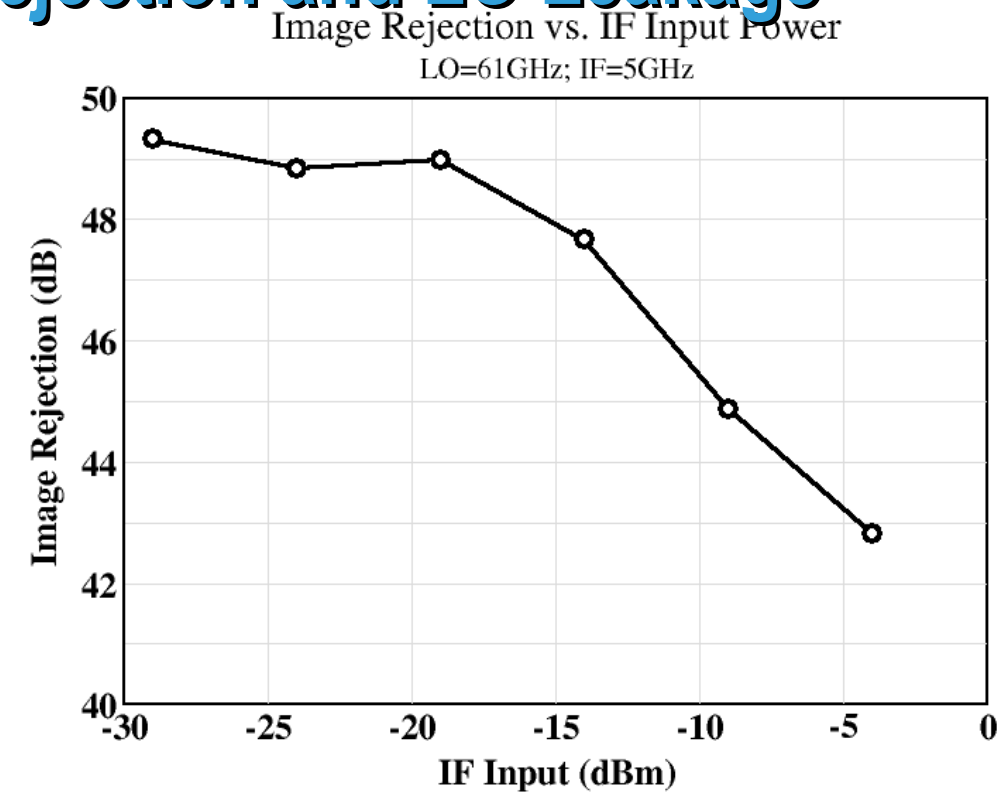


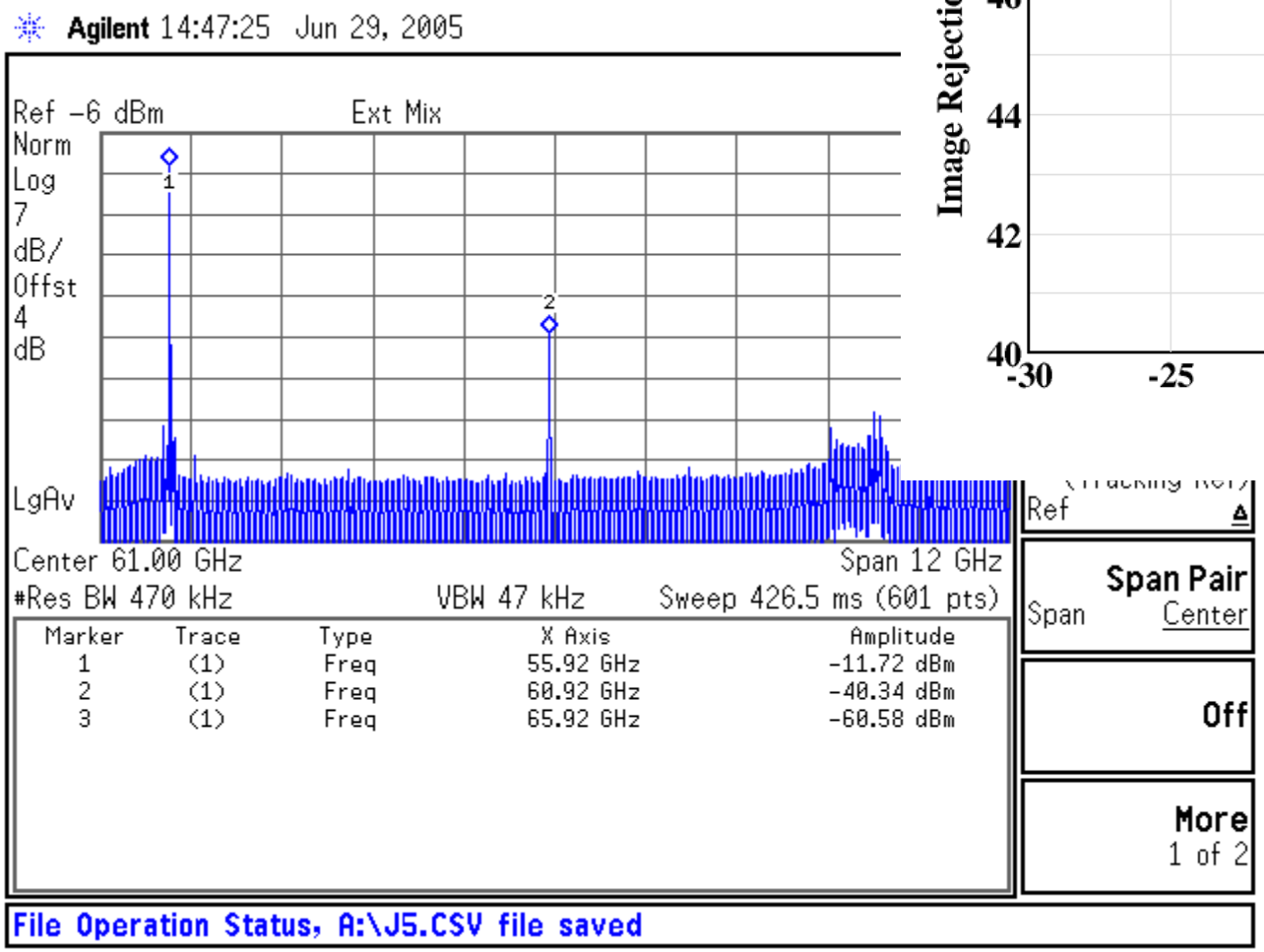




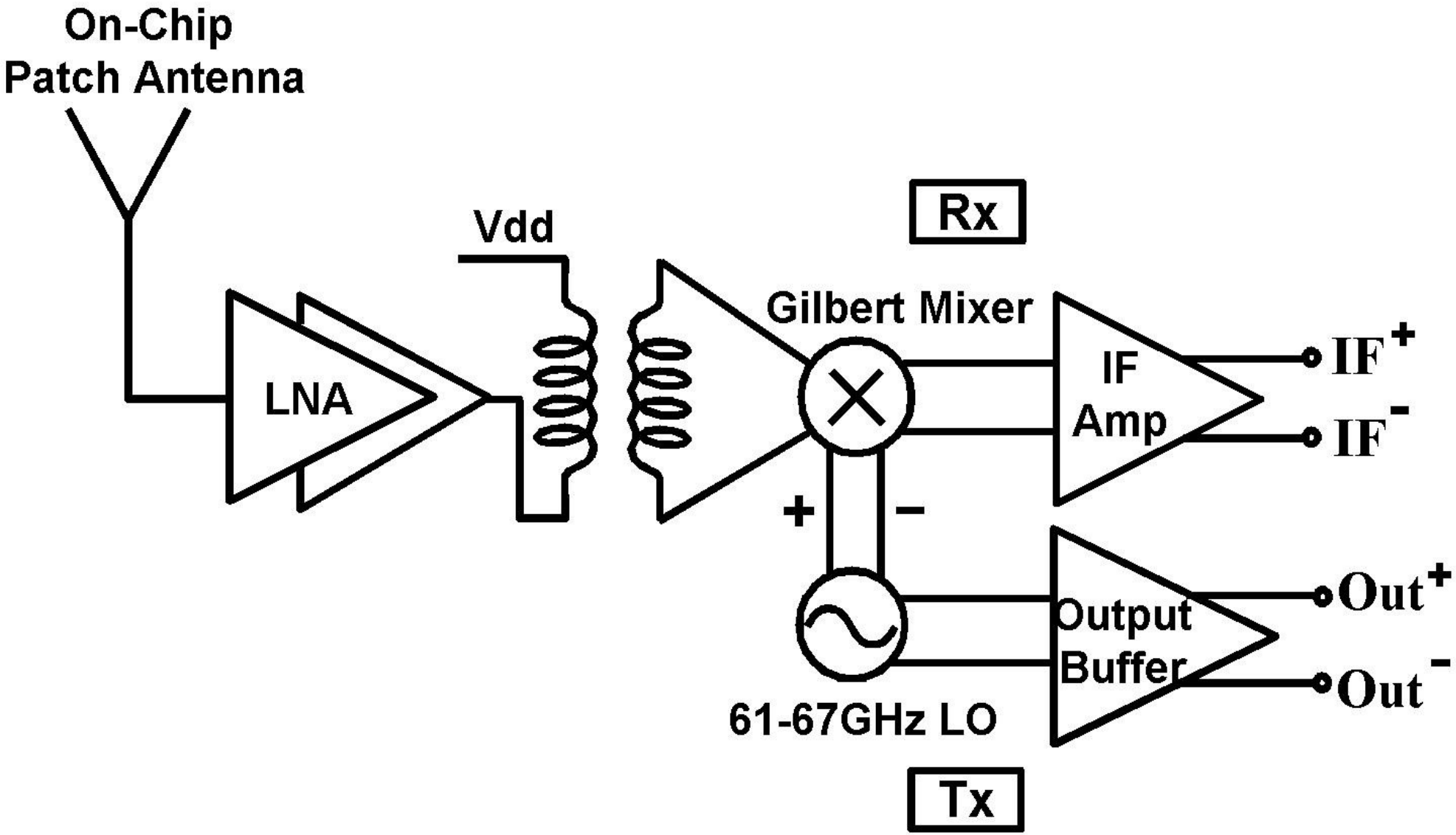


Trasmitter Image Rejection and LO Leakage

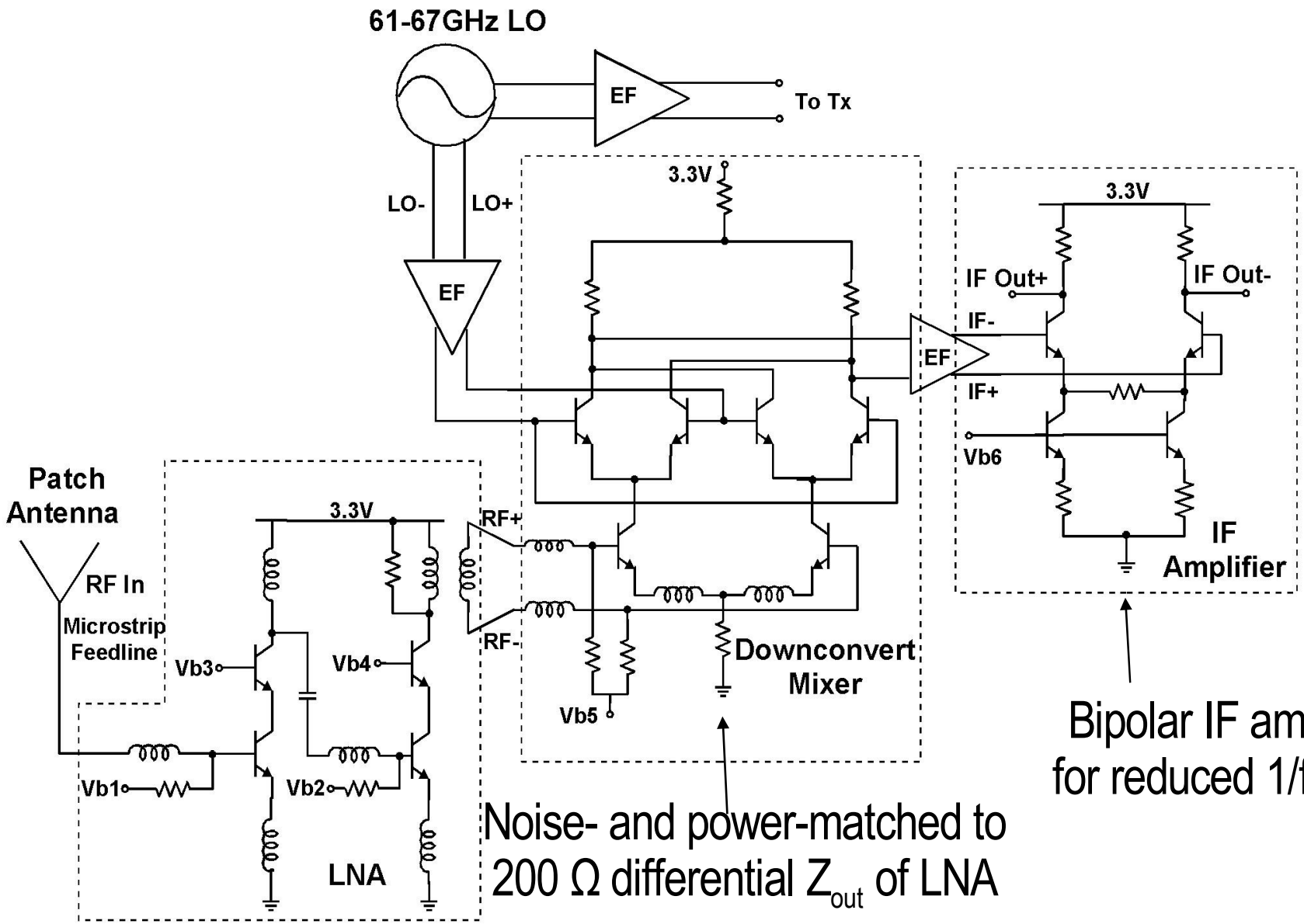




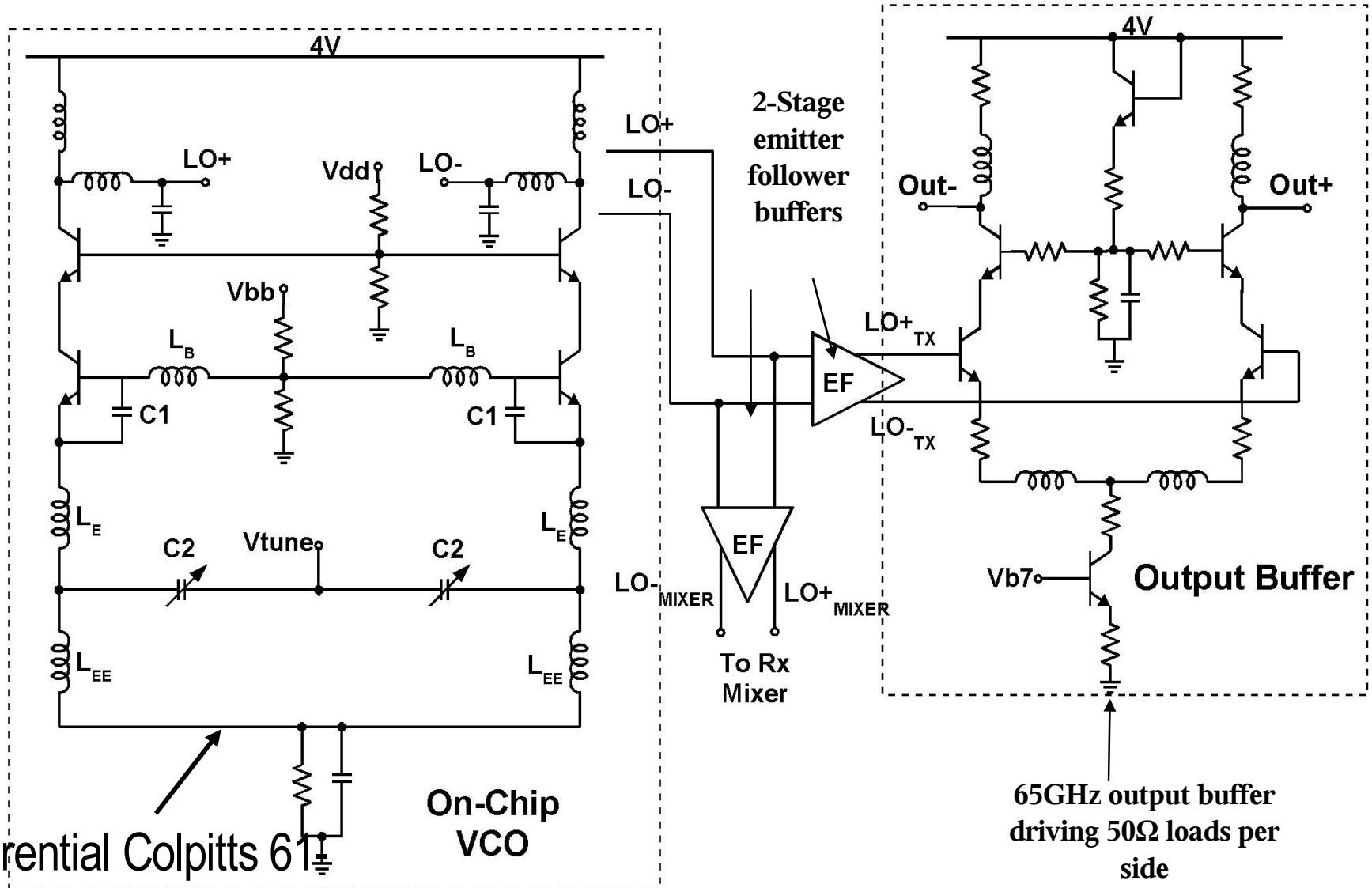
65-GHz Doppler Radar in SiGe BiCMOS (T.Yao et al. IMS-06)



Receive Path

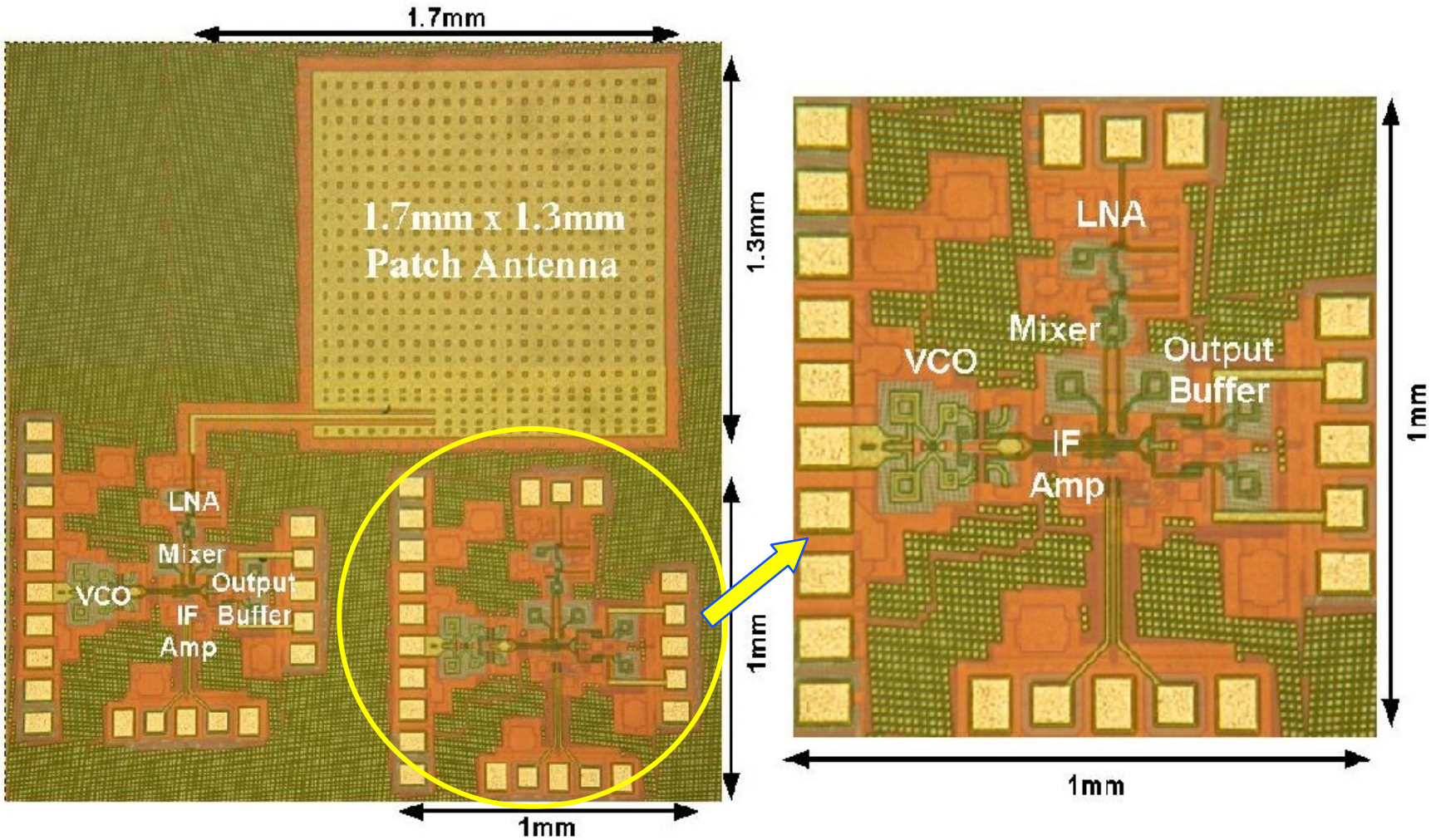


Transmit Path



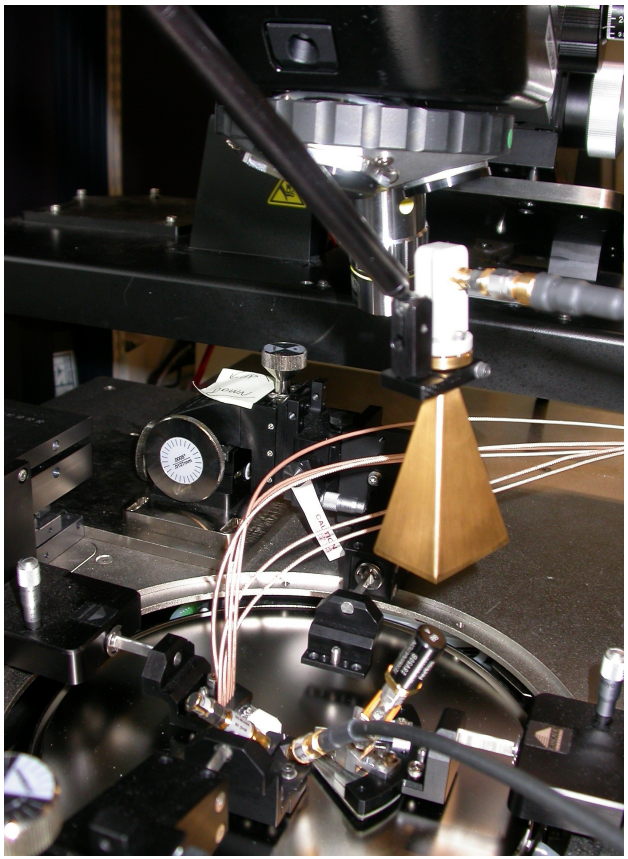
Differential Colpitts 61-67GHz VCO (shared with receive path)

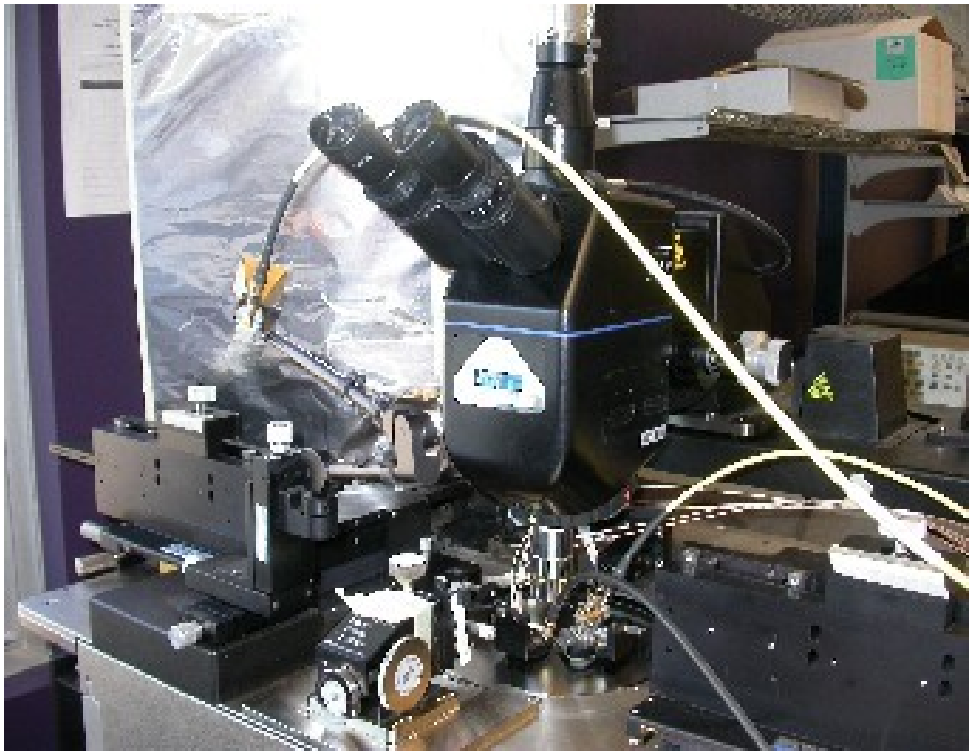
Die Photos



- Total Die Area: 2.5 x 2.5 mm^2
- Total Transceiver Area (without patch antenna): 1 x 1 mm^2
- Total Power: 640 mW

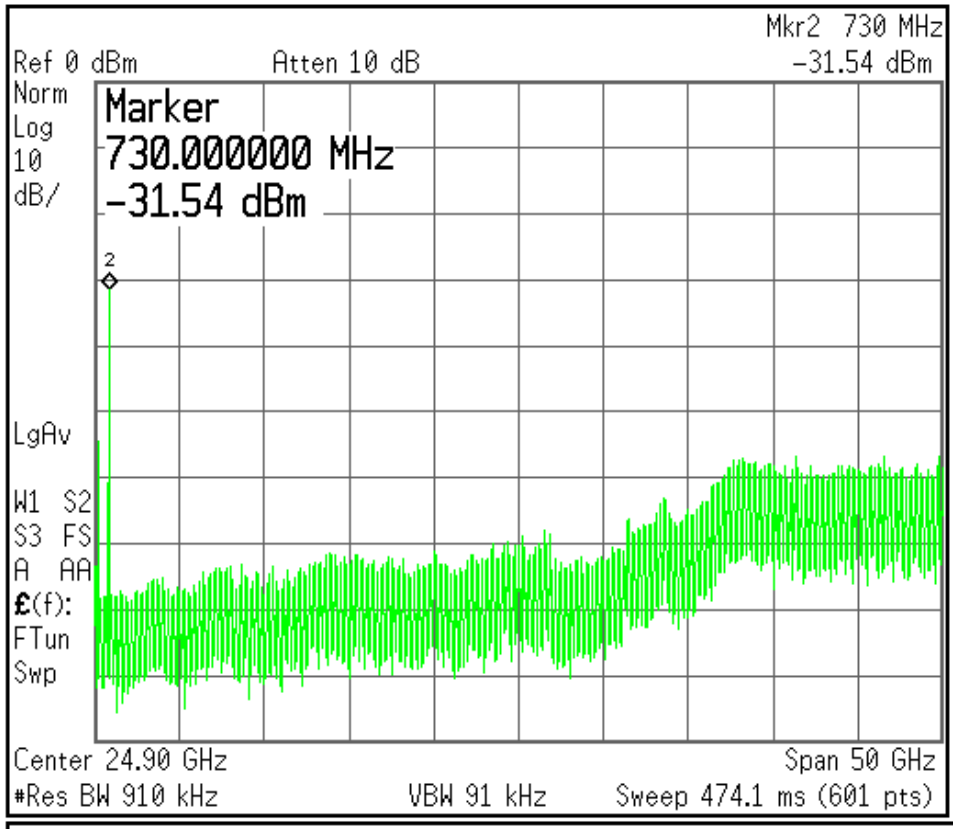
Experimental Results

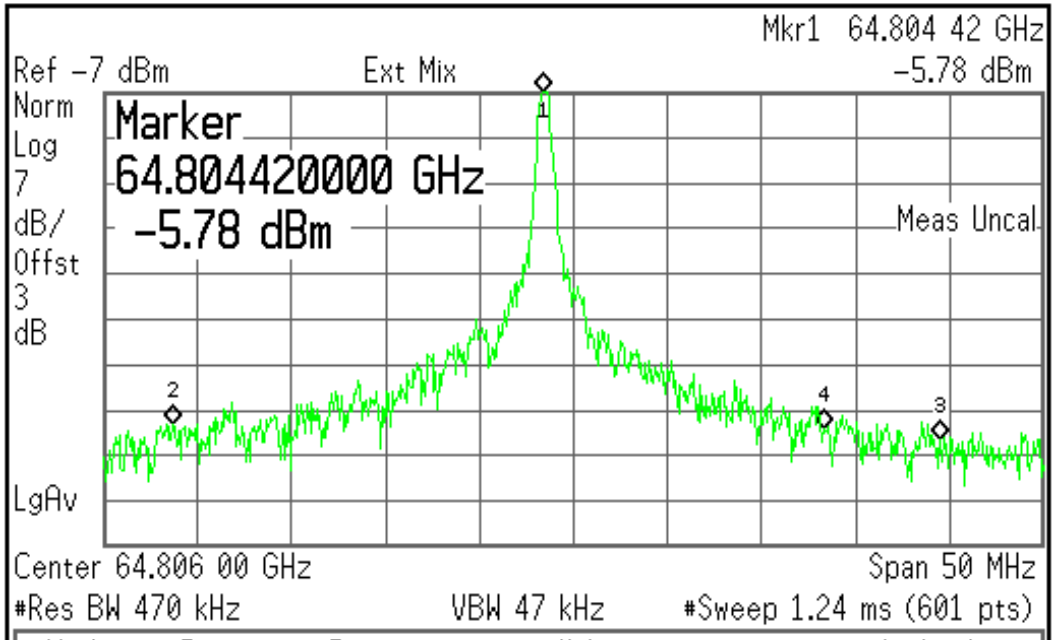




- 2 types of system characterizations:
  - on-wafer probing of sensor without on-chip antenna
  - measurement of full sensor using horn antenna/suspended probe and adjustable metal reflector

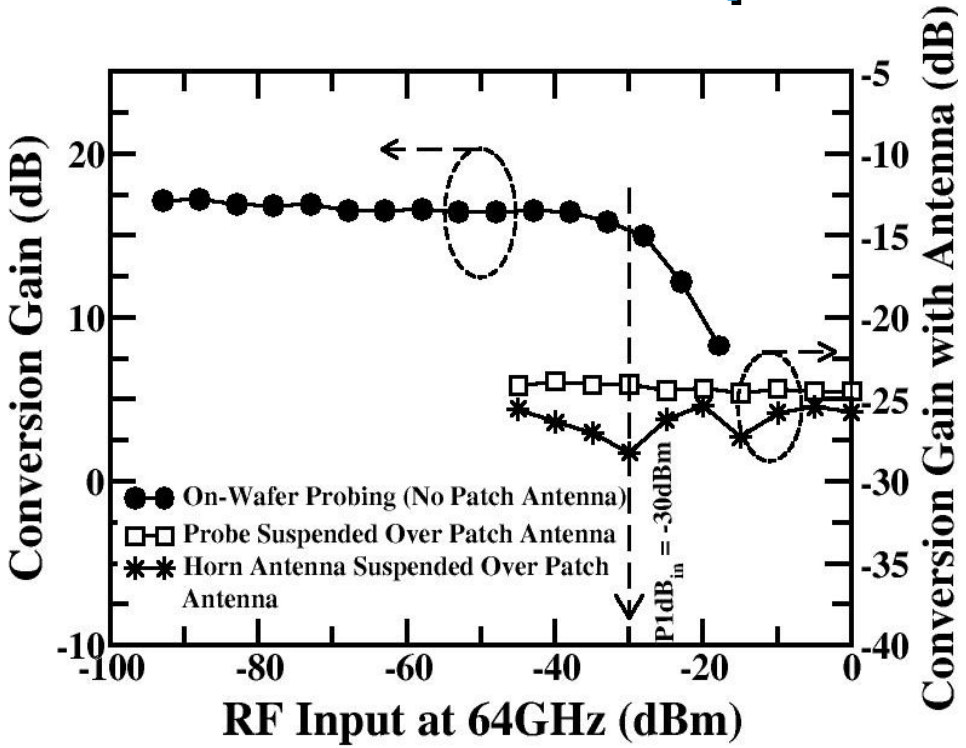
Experimental Results

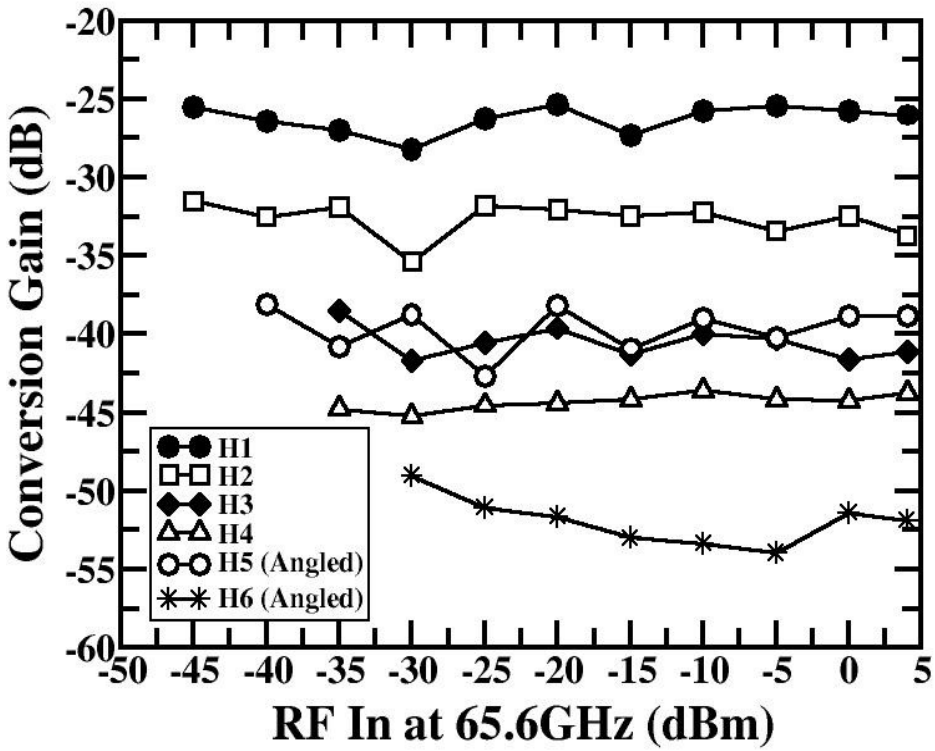




- Externally applied RF signal of -48 dBm at 64 GHz
- Single-ended down-conversion gain of 16.5 dB
- Single-ended output power of +1.3 dBm (+4.3 dBm differential) measured after de-embedding losses

Experimental Results





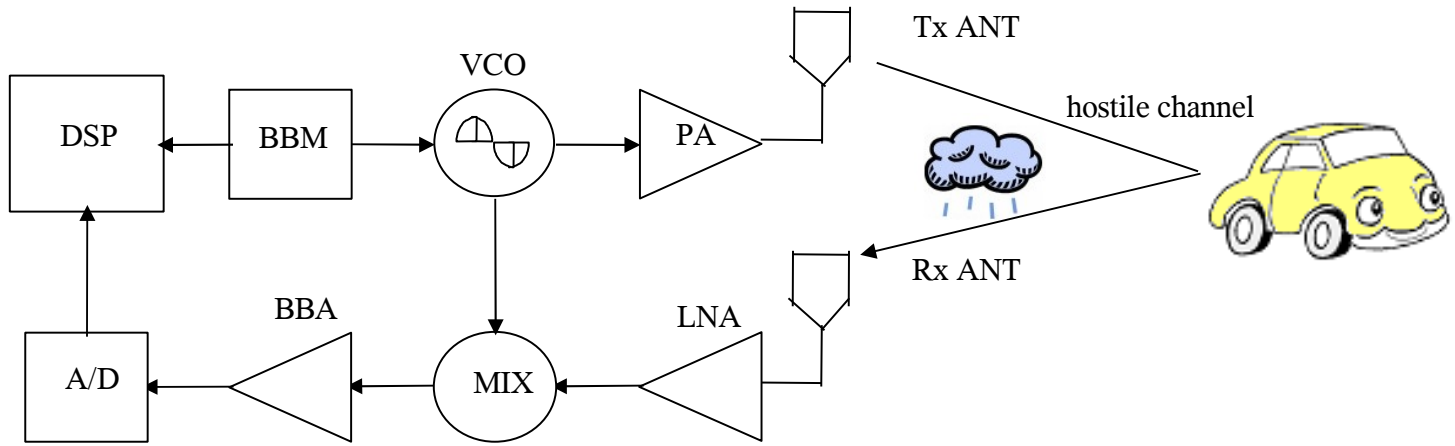
Single-ended conversion gain

- 16.5 dB without patch antenna
- -24.5 dB for suspended probe over patch antenna
- -26 dB for V-band horn over patch antenna

- Single-ended conversion gain for different elevations of V-band horn antenna over receive patch antenna

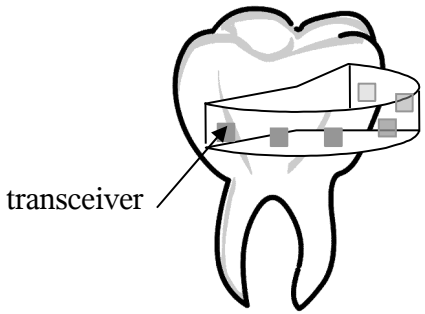
80-GHz Transceiver Platform for Radio, Imaging & Radar

- An FMCW Doppler radar = a direct conversion radio by any other name.



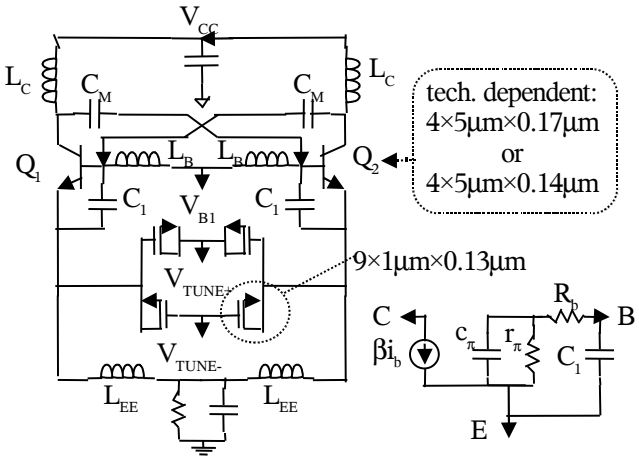
- Inverse scattering imager = an array of synchronized (or scanned) network analyzers

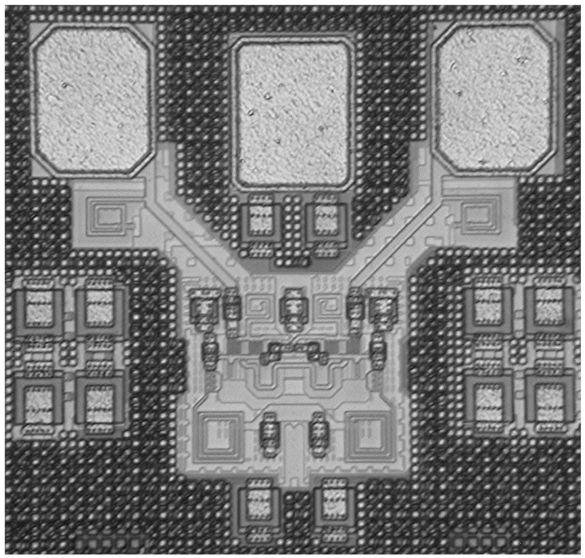
20 antenna-transceivers can be placed around the tooth, to check for cavities.

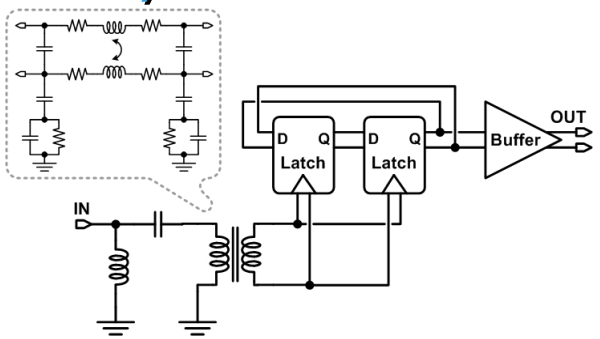


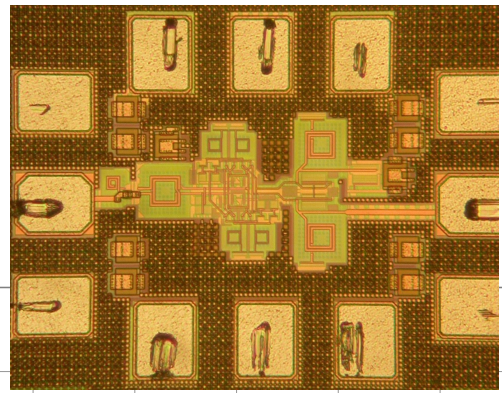
100-GHz SiGe-HBT VCO and Static Divider

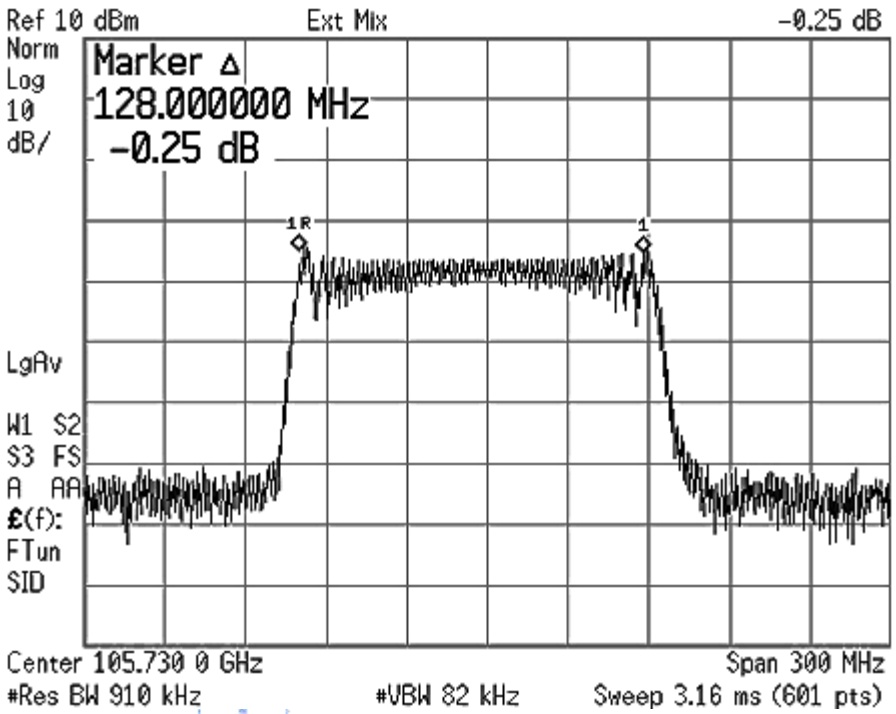
(S. Nicolson, E. Laskin, STM @ BCTM-06)

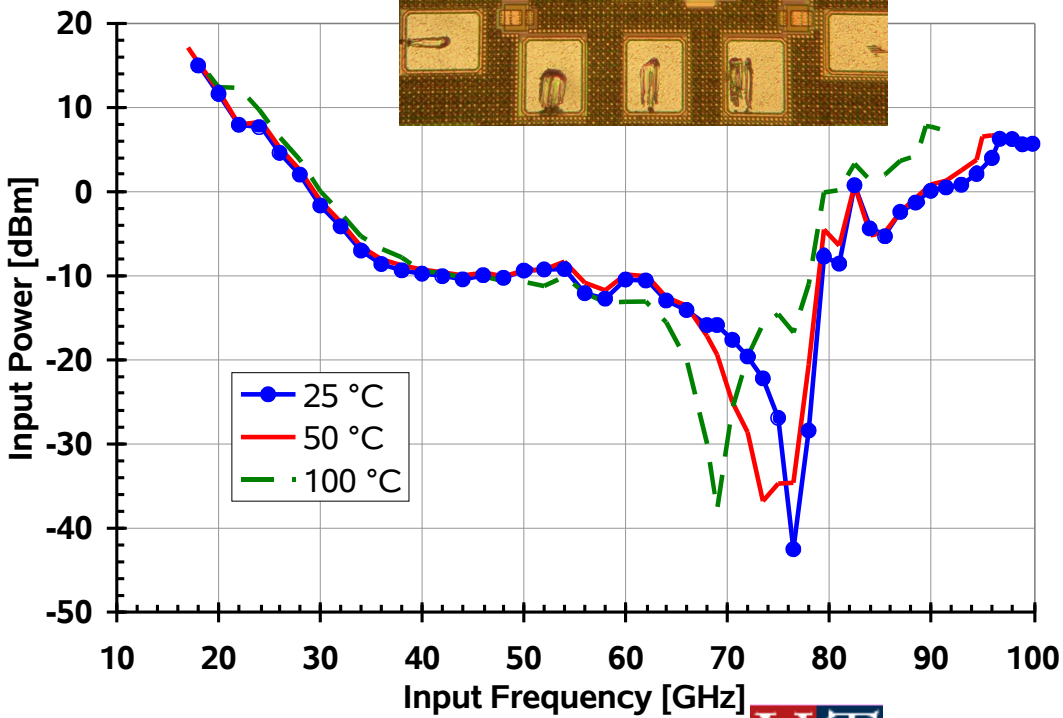




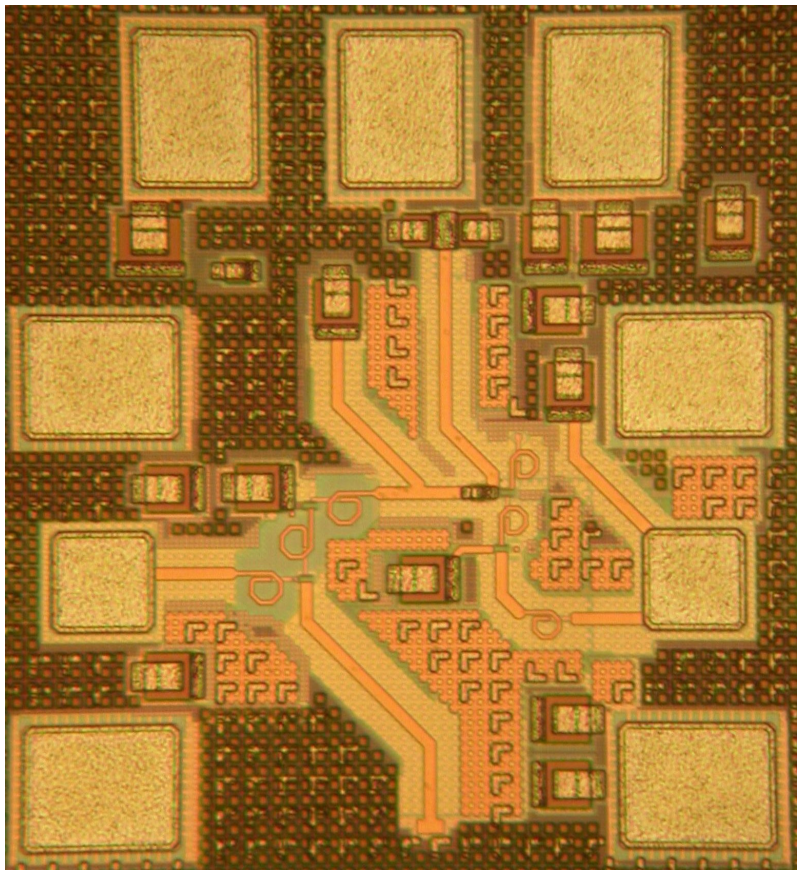




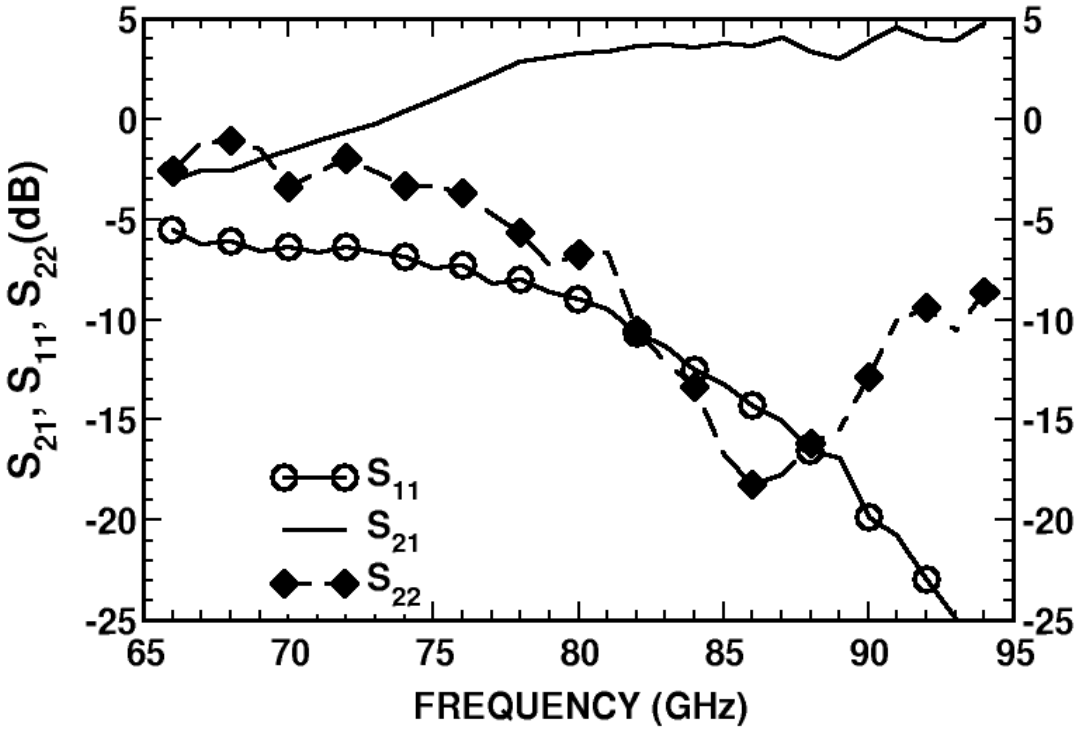




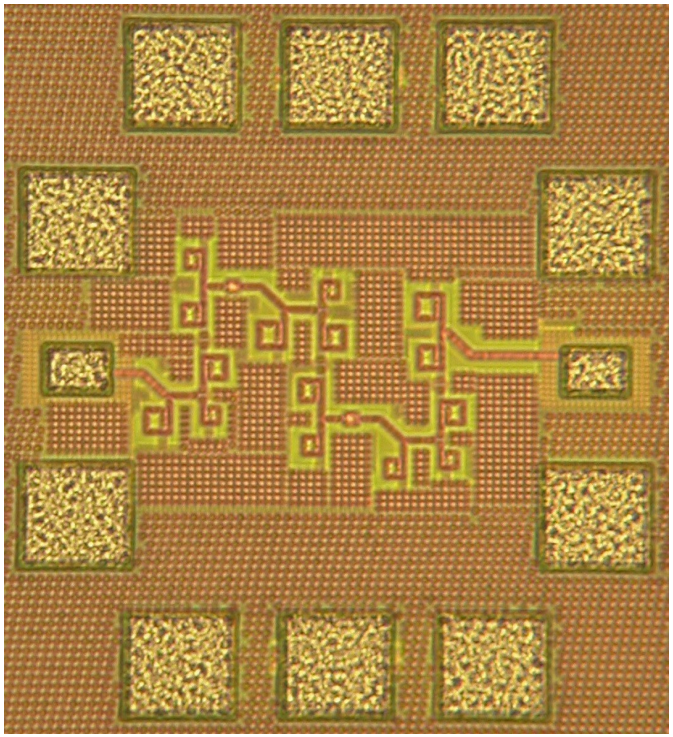
75-94 GHz LNA in (digital) 90-nm CMOS
(S. Nicolson, CSICS-06)

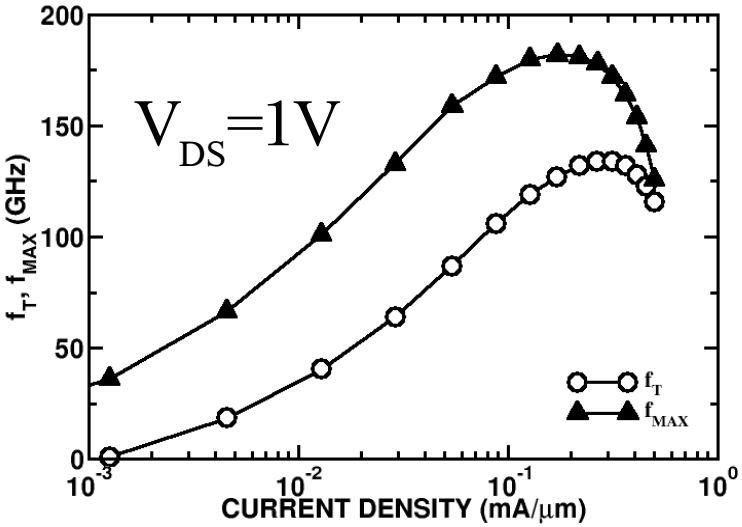


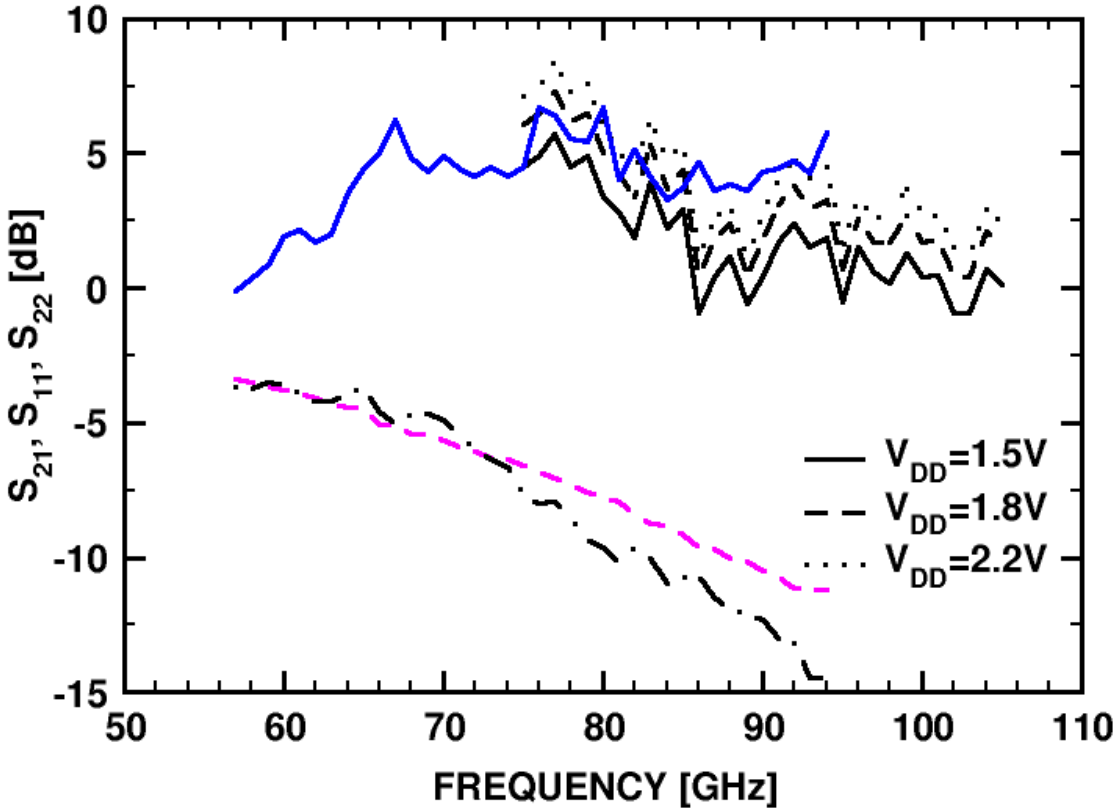
- 2-stage cascode
- Peak gain = 4.8 dB (94GHz)
- BW_{3dB}>20 GHz
- S_{11}, S_{22}<-10 dB
- Isolation > 30 dB
- 1.5 V supply, 22 mA



..and in 65-nm LP RF-CMOS (S. Nicolson)





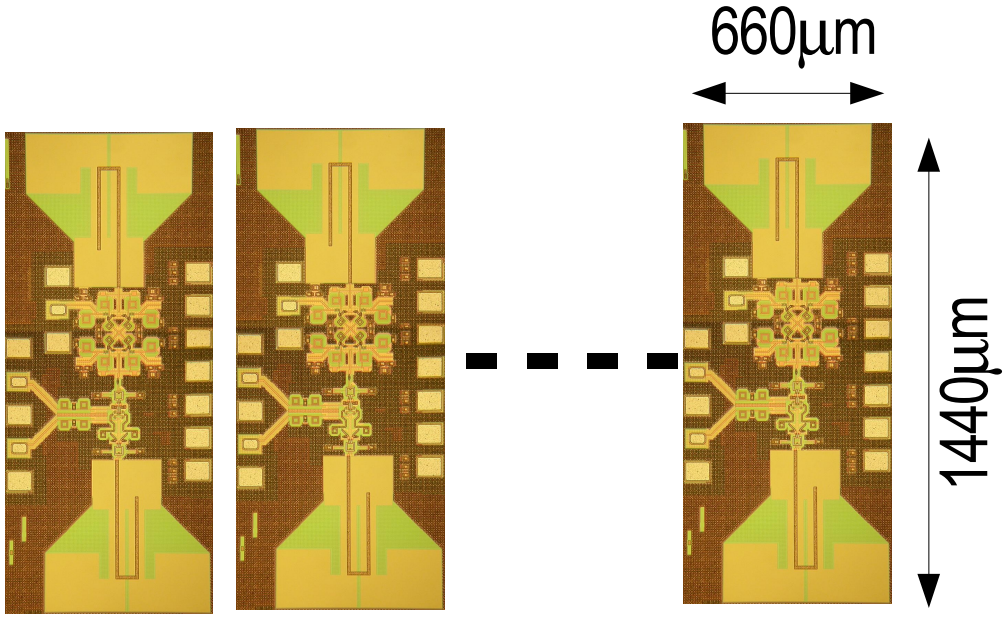


- f_T/f_{MAX} = 140/180 GHz (W_f=2μm)
- 3-stage cascode
- Peak gain = 9 dB (80 GHz)
- S_{11}, S_{22}<-10dB
- Isolation > 30 dB

mm-wave Imaging Beyond the ITRS Horizon of 100 GHz

- Arrays of low power mm-wave transceivers on a die with lumped components

  (Gordon Moore, Electronics 1965)

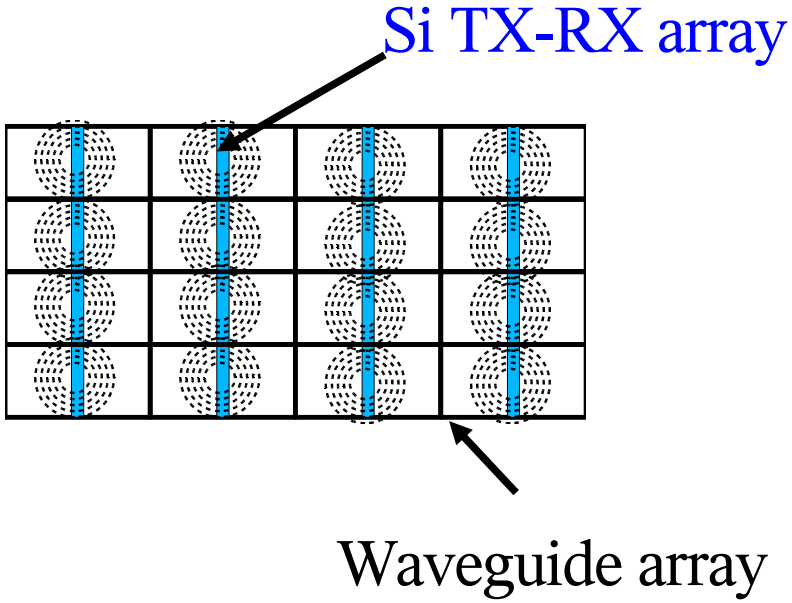


- Isolation between single-chip transceivers and/or antennas: Faraday Cage

  At 160 GHz => 1.2mmx0.6mm

  waveguide cross-section =

  transceiver size



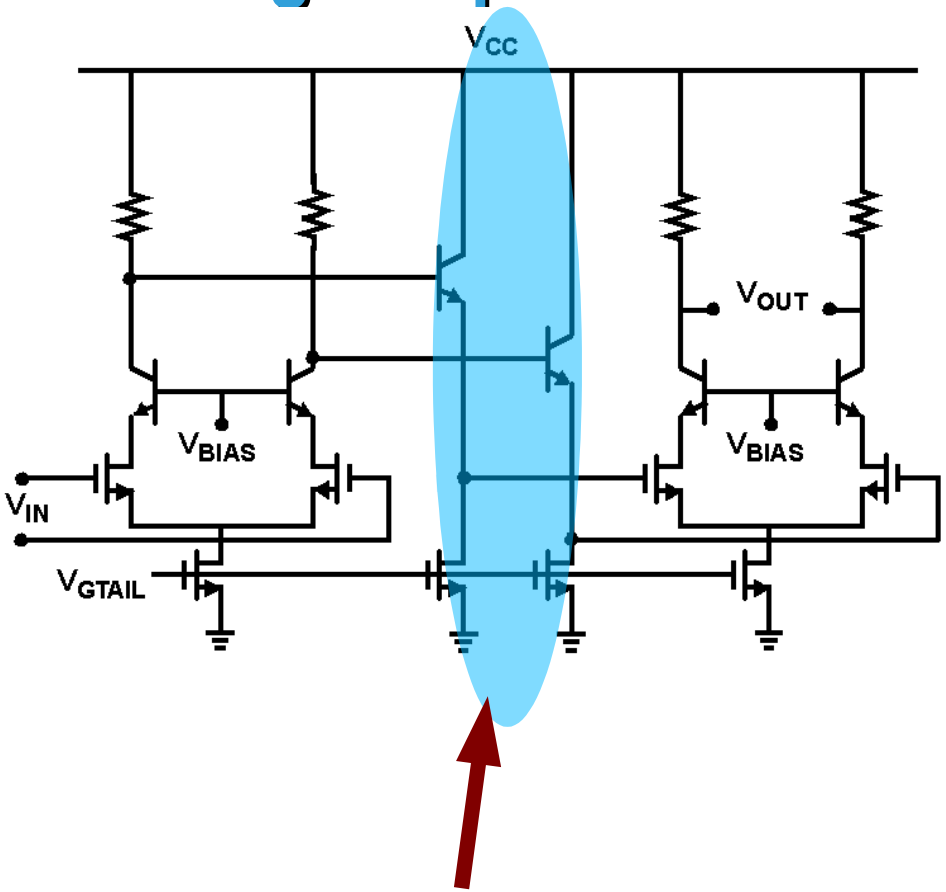
Summary

- Noise correlation modelling and J_{pfT} reduction need to be addressed
- Sub 90-nm emitters are unavoidable for HBTs with 500 GHz f_T/f_{MAX}
- At and above 40 Gb/s there is no power dissipation advantage for 65-nm MOS-CML over 1.8-V, 130-nm SiGe BiCMOS CML
- 90/65nm CMOS is competitive in 60-100 GHz LNAs and receivers
- 60-GHz PLL unlikely in 65-nm CMOS. Only multiplier or 2nd. harmonic VCO approach will work.
- 300-GHz, 130-nm SiGe BiCMOS has cost, performance, and robustness edge over 65-nm CMOS in mm-wave applications

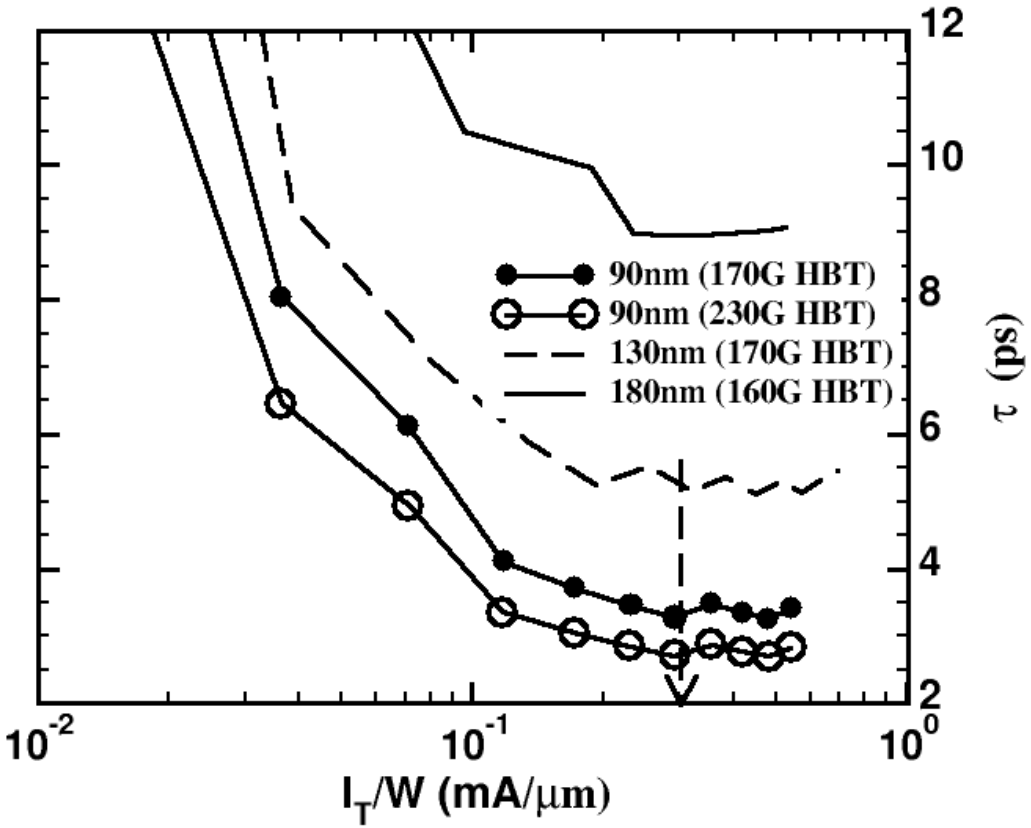
Acknowledgments

- Dr. P. Chevalier, B. Sautreuil at STM
- Dr. M. Racanelli, P. Kempf at Jazz Semiconductor
- Dr. M.T. Yang at TSMC
- Dr. Peter Schvan at NORTEL
- CITO, NSERC, STM, NORTEL, Gennum, Jazz Semi for funding
- STM, Jazz Semiconductor, TSMC, NORTEL and CMC for fabrication
- Jaro Pristupa and CMC for CAD support
- OIT, CFI, ECTI for equipment

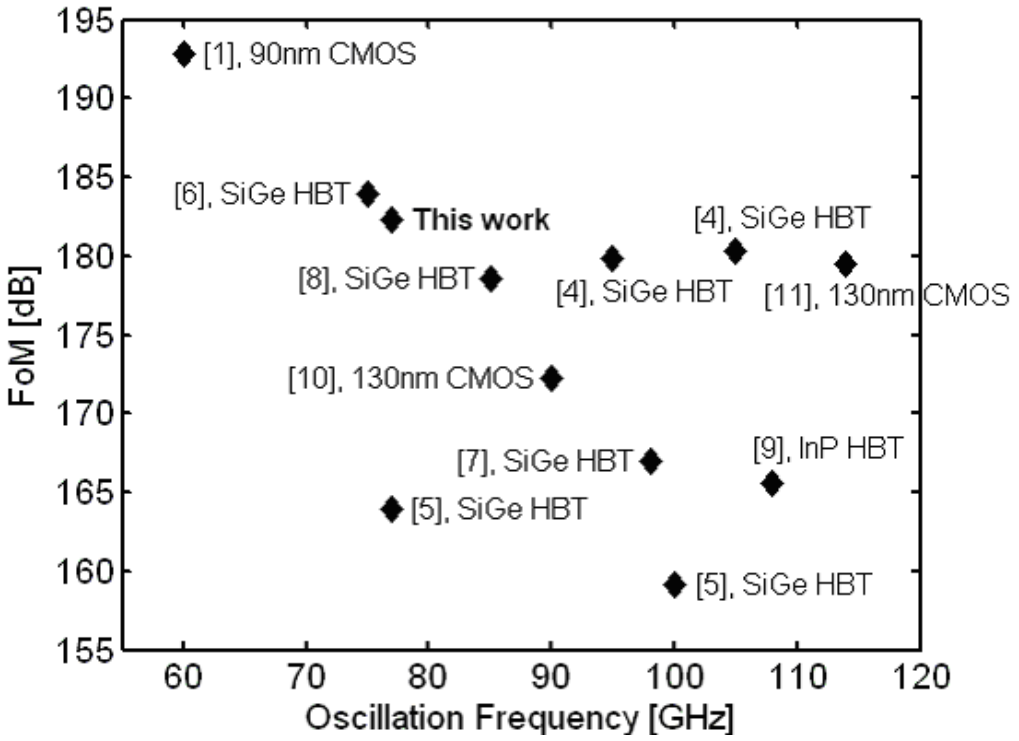
Adding 90-nm CMOS to a SiGe HBT has significant impact on gate speed while allowing operation from <2.5 V

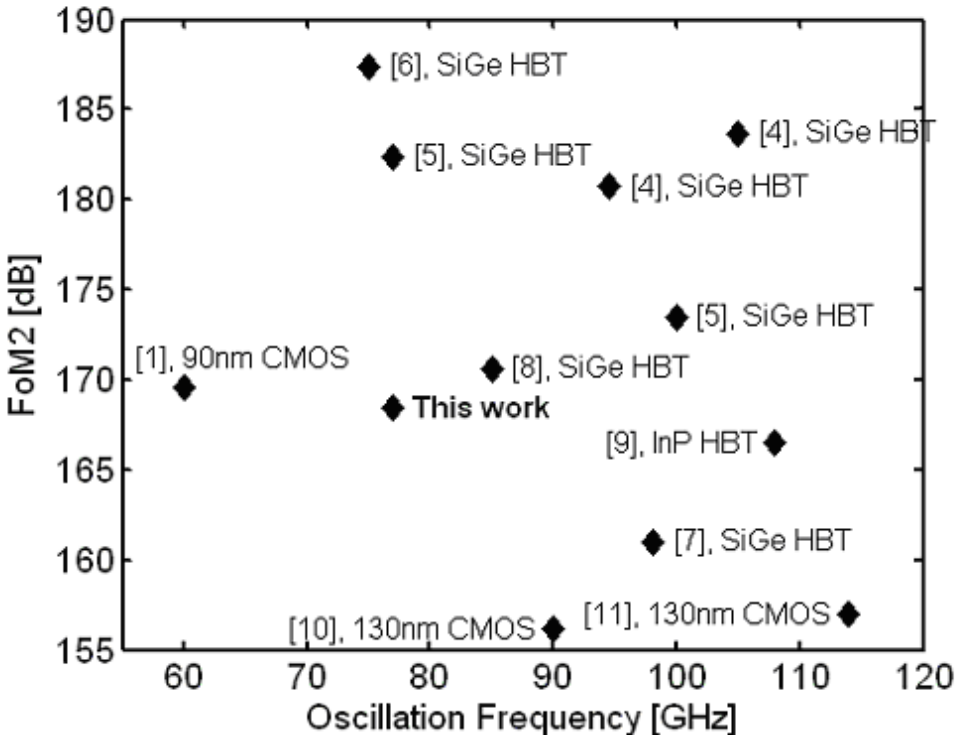


- For level-shifting only
- Not accounted for in delay



Comparison of State-of-the-Art SiGe & CMOS VCOs





$$\left(\frac{f_o}{\Delta f}\right)^2 \frac{1}{L(\Delta f)P_d}$$

$$\left(\frac{f_o}{\Delta f}\right)^2 \frac{P_{out}}{L(\Delta f)P_d}$$

[4] S. Nicolson et al. (U of T & STM) @ BCTM-2006

This work: 90-nm CMOS K.Tang et al. @ CSICS-2006