Quake | Technologies Inc

Circuits and Technologies for Highly Integrated Optical Networking ICs at 10Gb/s and 40Gb/s

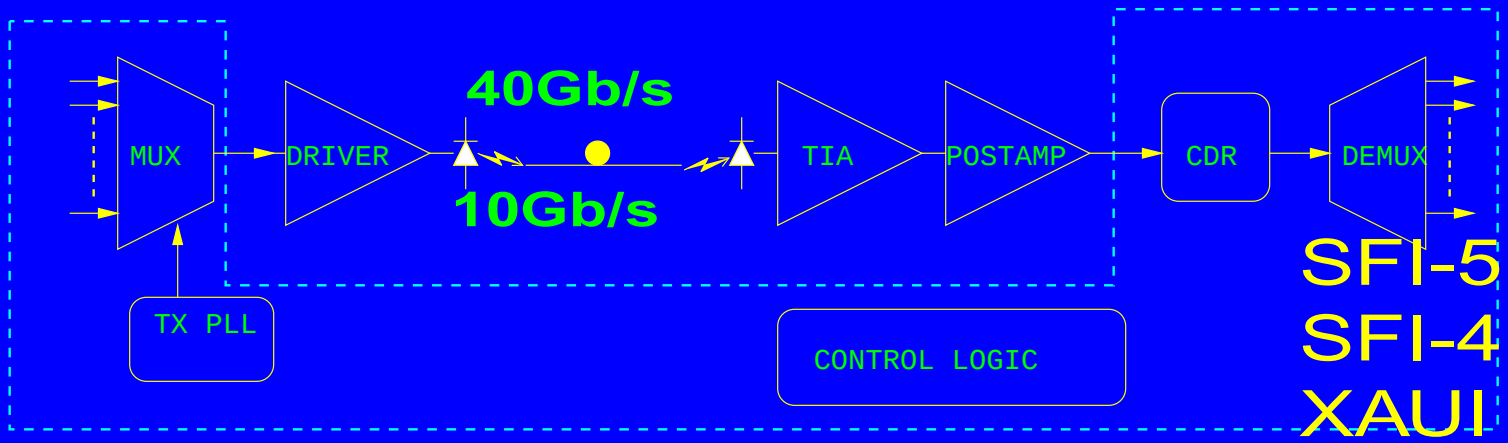
S.Voinigescu, P.Popescu, P.Banens, M.Copeland, G.Fortier, K.Howlett, M.Herod, D.Marchesan, J.Showell, S.Szilagyi, H.Tran, and J.Weng

SHAKE THINGS UP

Outline

- Introduction
- Device Technologies
  - Si/SiGe vs. GaAs vs. InP; FET vs. Bipolar
- 10Gb/s and 40Gb/s Building Blocks
  - VCOs
  - Output Drivers
  - Limiting Amplifier
- **Highly Integrated 10Gb/s ICs**
  - 10.7Gb/s TIALA
  - 10Gb/s OIF-compliant SERDES

Introduction



- SFI-5 (OIF standard): 17x(2.5Gb/s .. 3.125Gb/s)
- SFI-4 (OIF standard): 16x(622Mb/s .. 666Mb/s)
- XAUI (10GBE IEEE802.3ae): 4x3.125Gb/s
- SerDes:10K analog transistors, 100K..500K gates

Goal

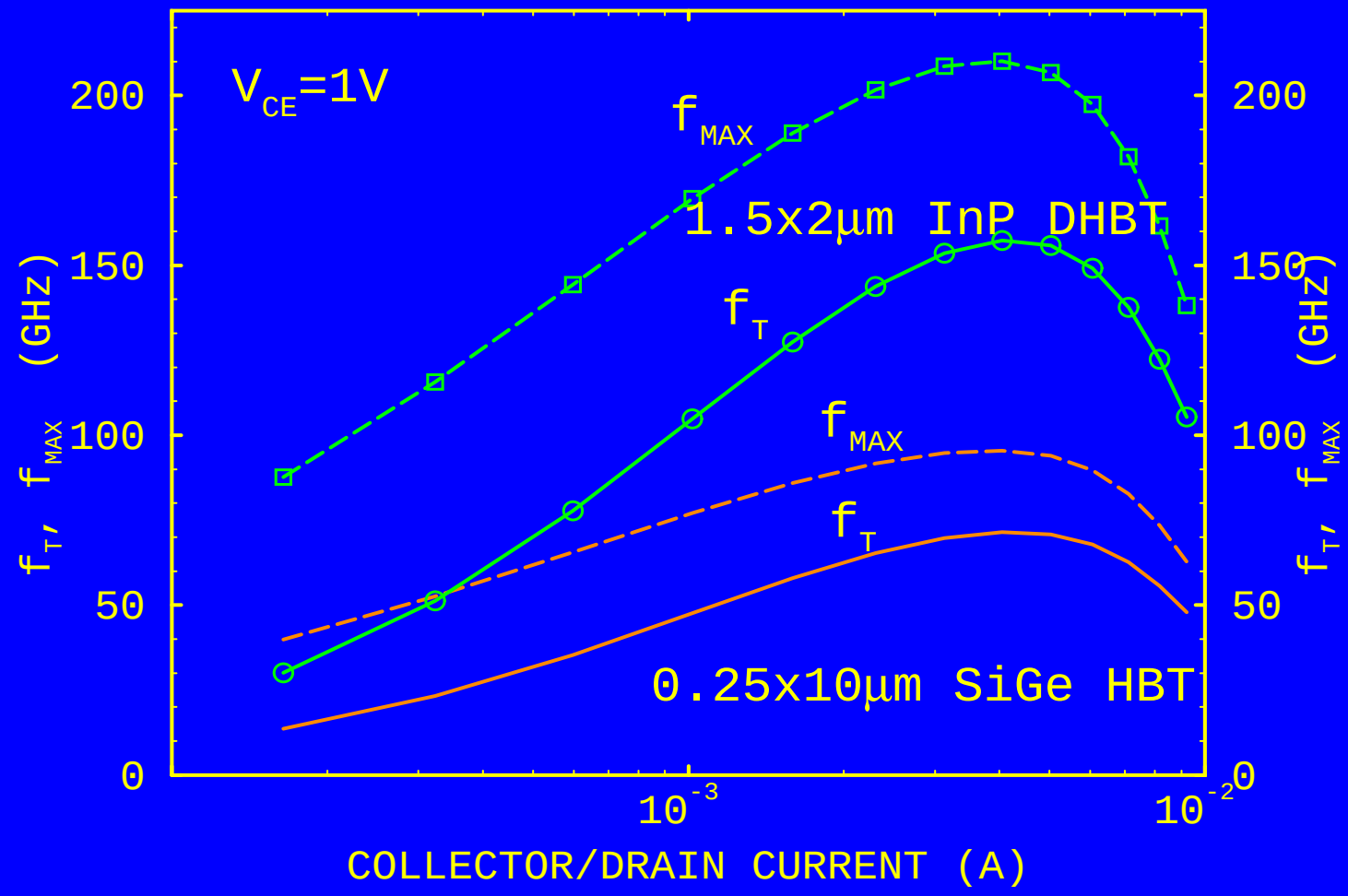
- Define technology requirements for highly integrated PHY ICs at 10Gb/s and 40Gb/s
- Compare competing technology performance
- Examine basic circuit building blocks
- Demonstrate a highly integrated, OIF-compliant 2-chip PHY solution for 10Gb/s applications

Technology Requirements

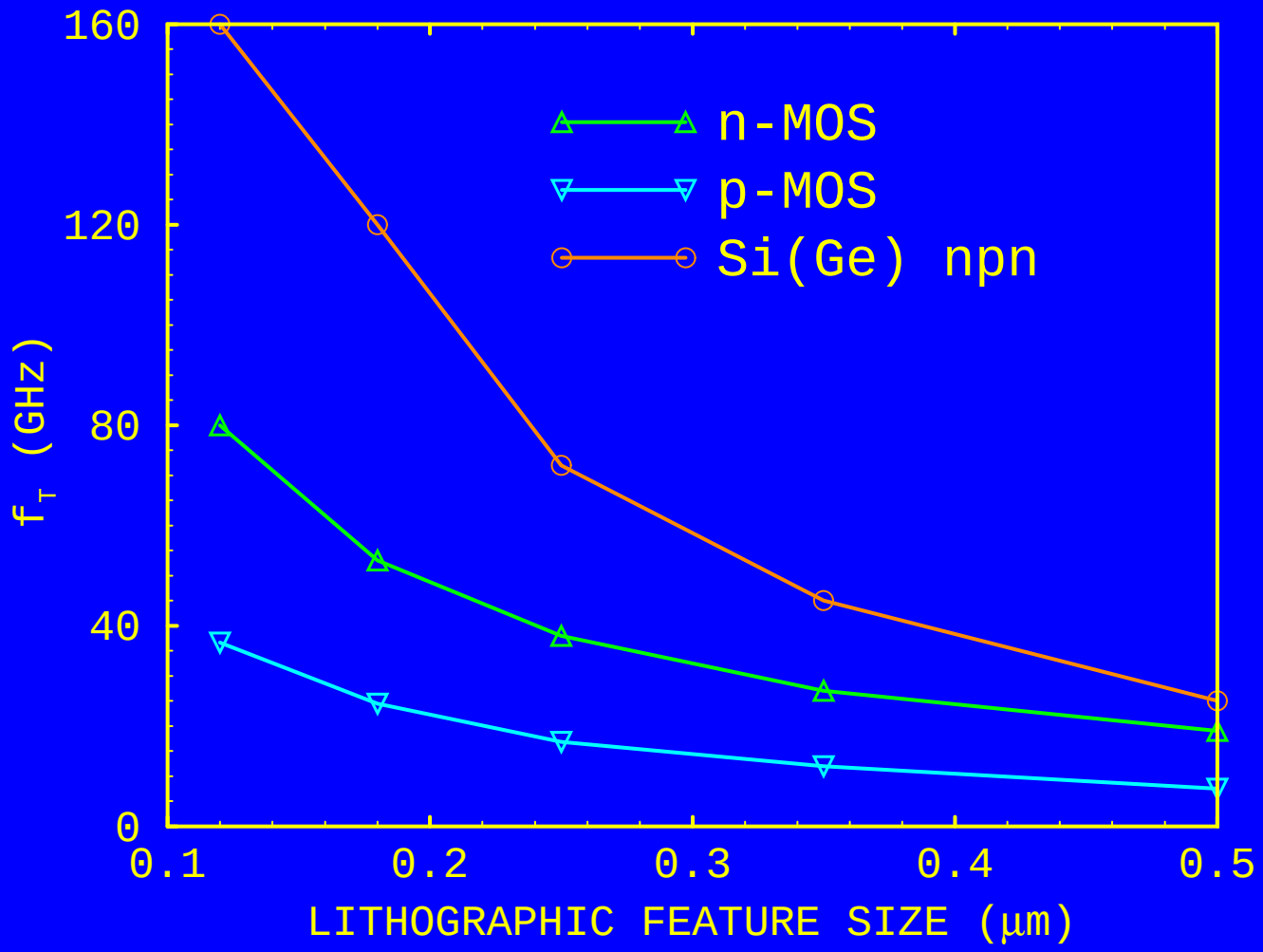
- f_T, f_{MAX} @V_{CE}=1V, T=100 °C > 4x Bit Rate
- low peak f_T current density but high intrinsic slew-rate (SL_I)
- small feature size
- high Q inductor and varactor
- low turn-on voltage
- high breakdown (for drivers)
- fine metal pitch and large metal layer count

Transistor Performance

InP vs. SiGe HBT



f_T Scaling of Si Technologies

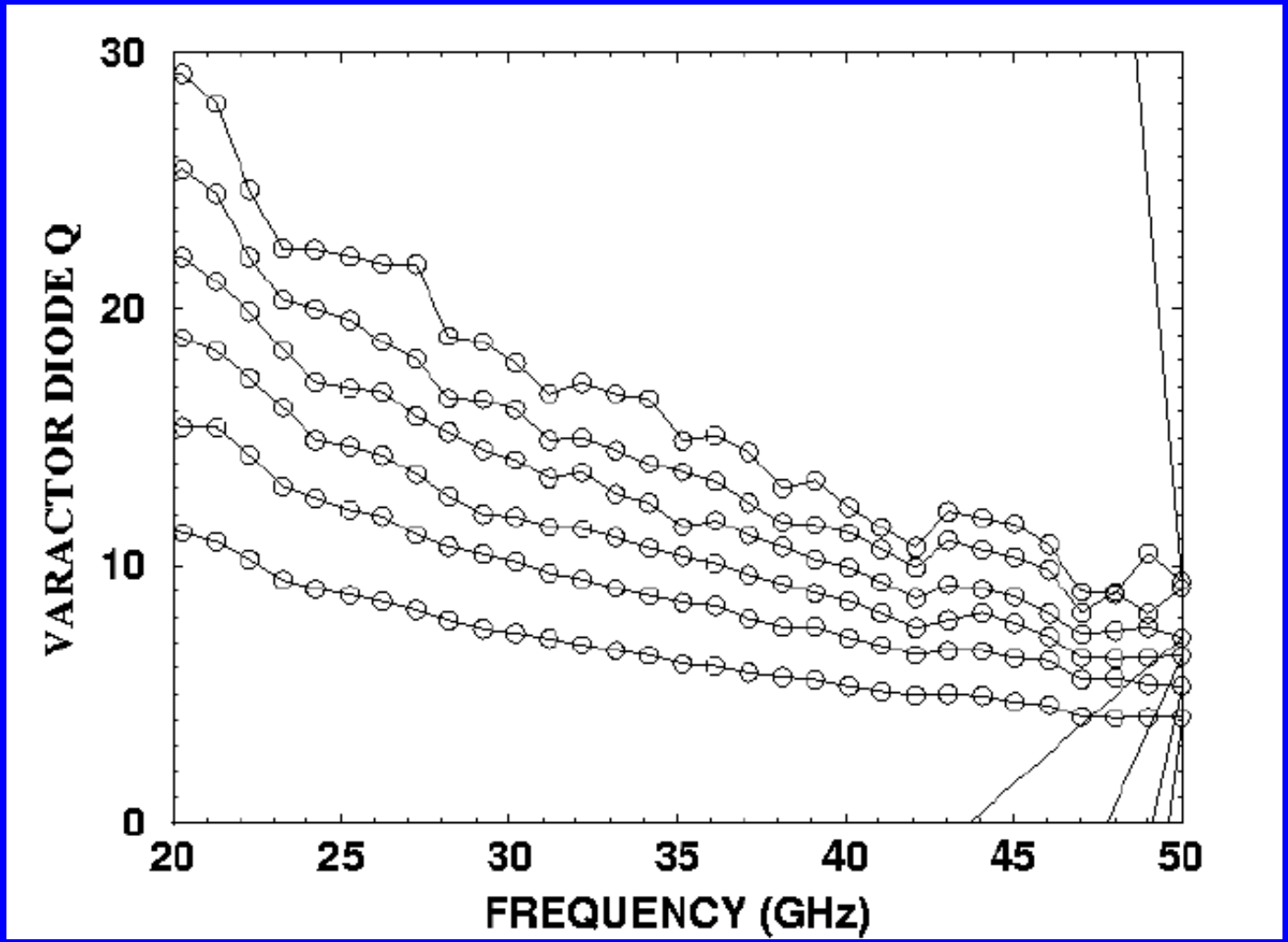


Transistor Technologies

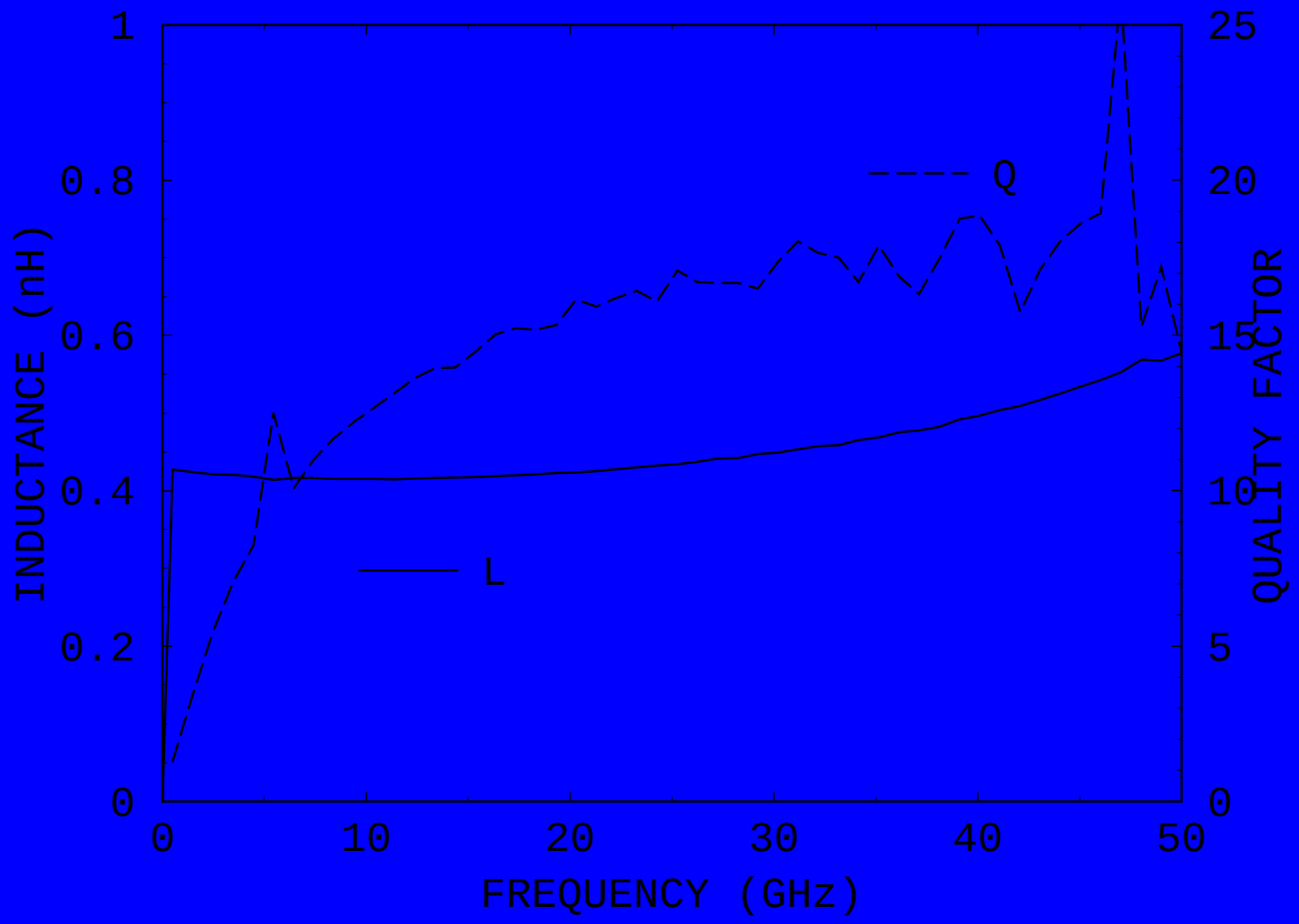
Device param	InP DHBT	GaAs HBT	SiGe HBT	n-MOS	p-MOS
size (μm)	1	2	0.25	0.12	0.12
f_T (GHz)	160	70	70	80-90	40
f_{MAX} (GHz)	200	70	90	70-90	40-50
J_{CPfT} (mA/μm^2)	1.2	0.8	3	2.6	1.3
SL_I (V/ps)	1	0.5	0.35	1.4	0.7
BV_{CEO} (V)	>6	>10	2.8	>1.2	>1.2
V_{BE}/V_T (V)	0.8	1.4	0.9	0.35	-0.35

Passive Device Performance

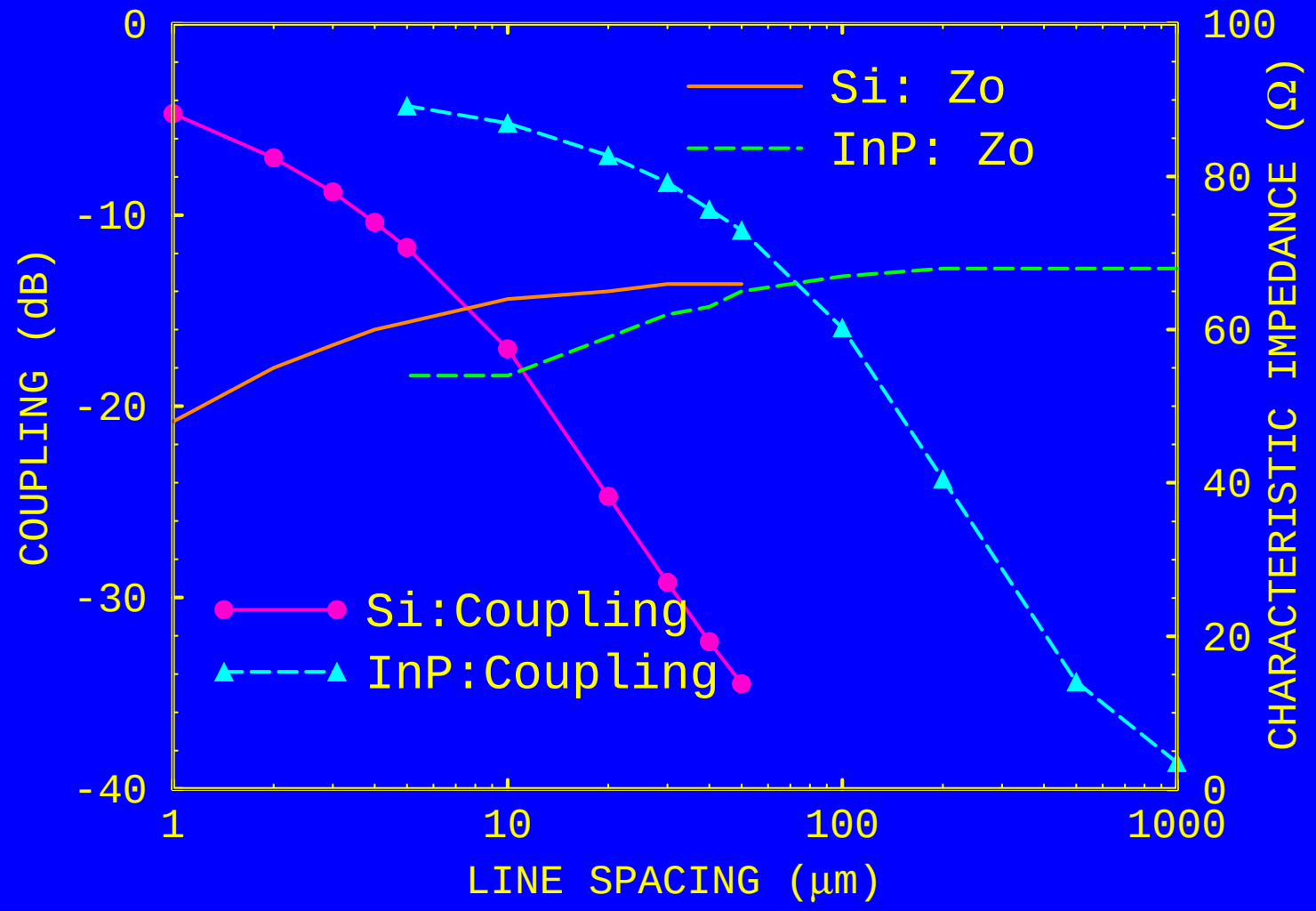
100fF Si Varactor Diode Q



0.425nH Si Inductor



On-Wafer Coupling/Isolation

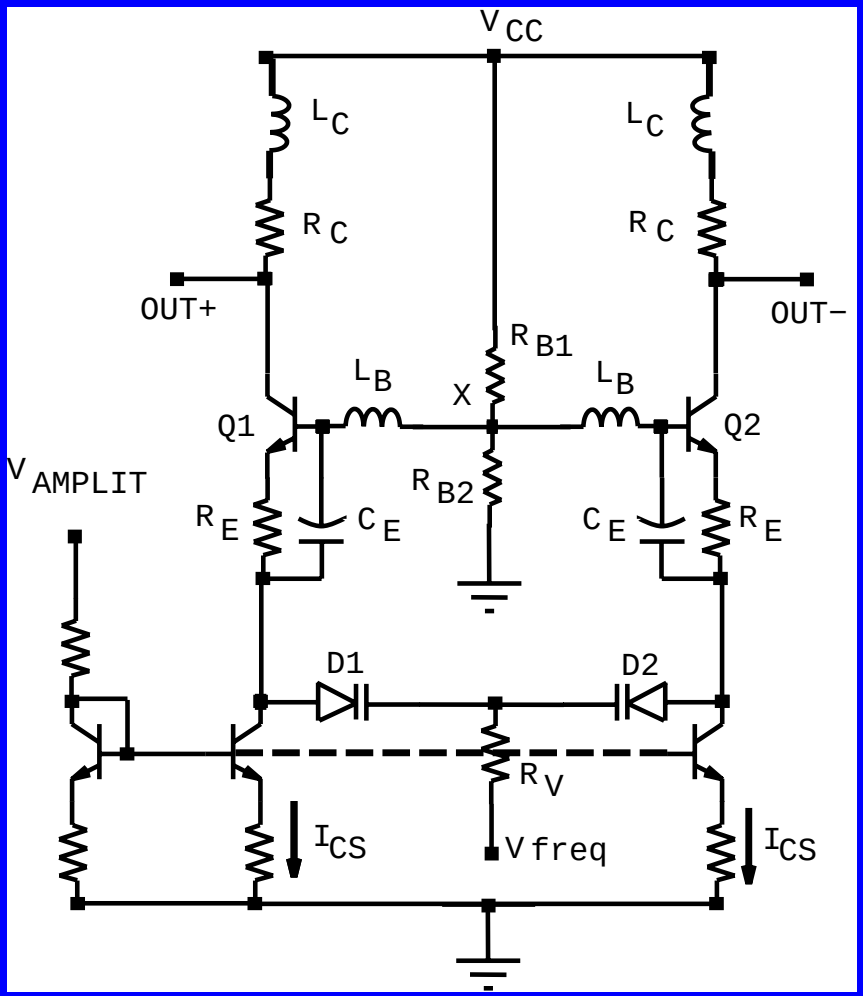


Building Blocks

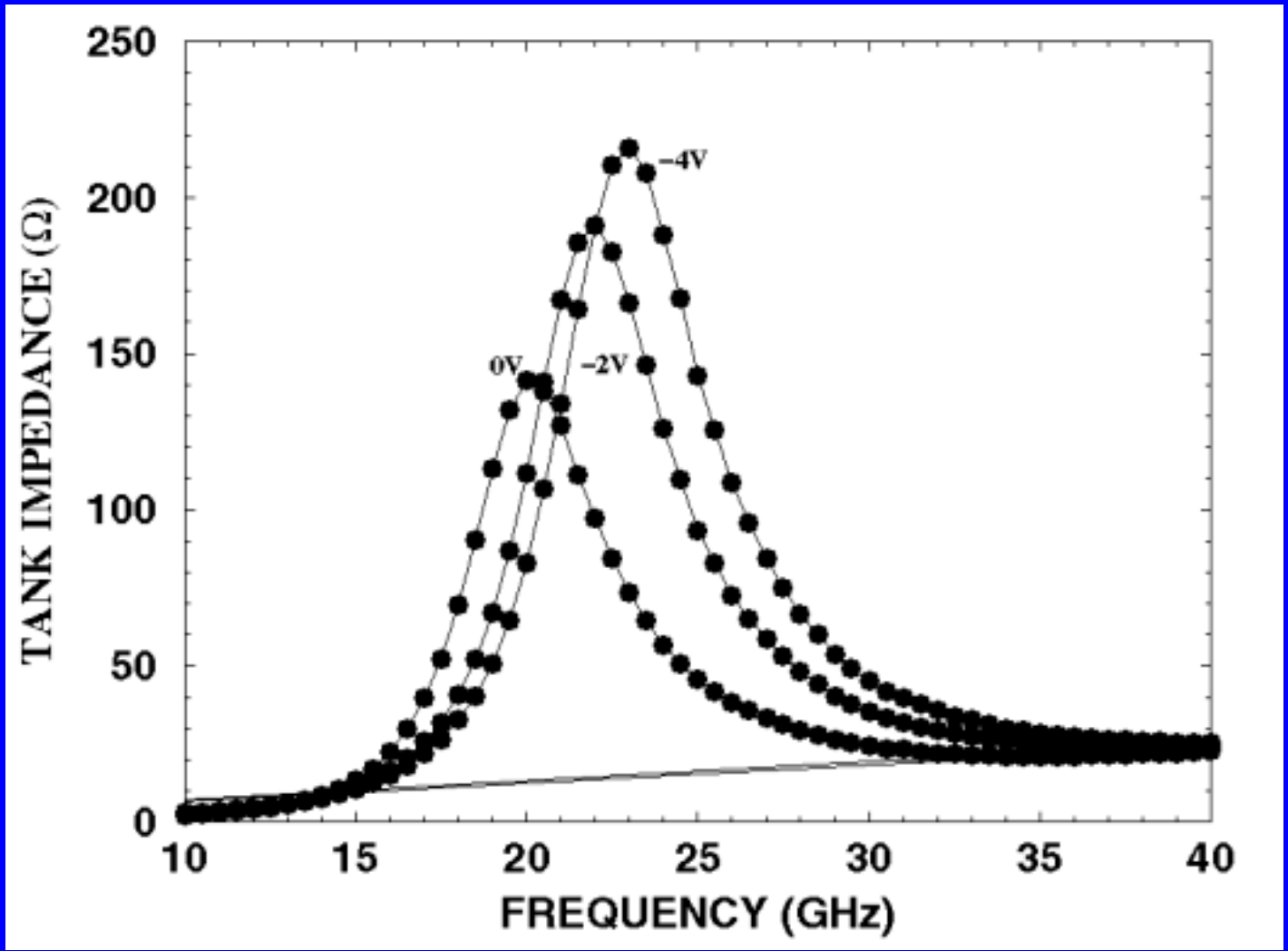
Si/SiGe 20/40GHz VCO

S.Voinigescu et al., MTT-Symposium 2000

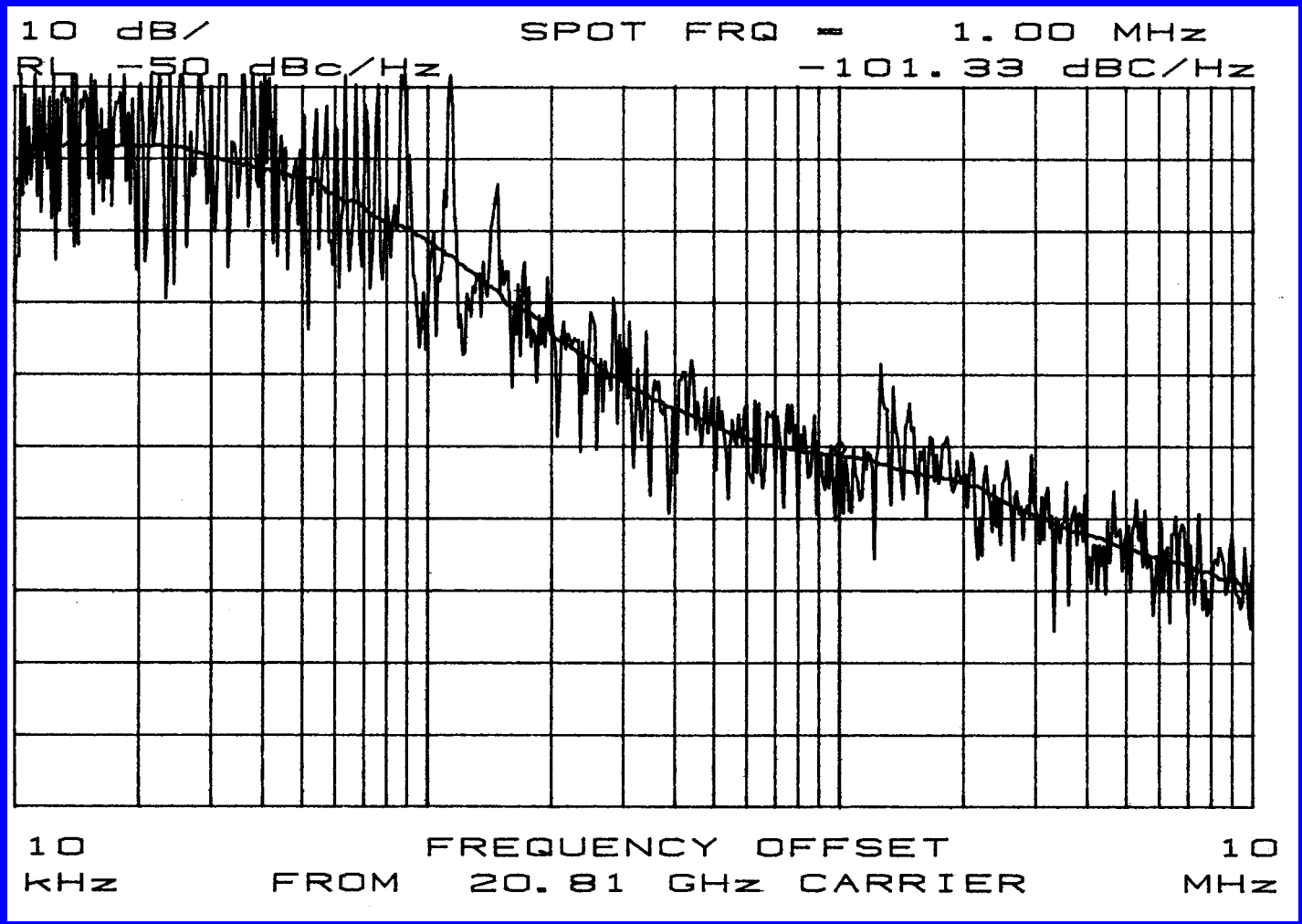
- **21.4GHz differential mode at OUT+ and OUT- nodes**
- **42.8GHz single-ended operation at X node.**
- **15% tuning range**
- **100dBc/Hz @ 1MHz**



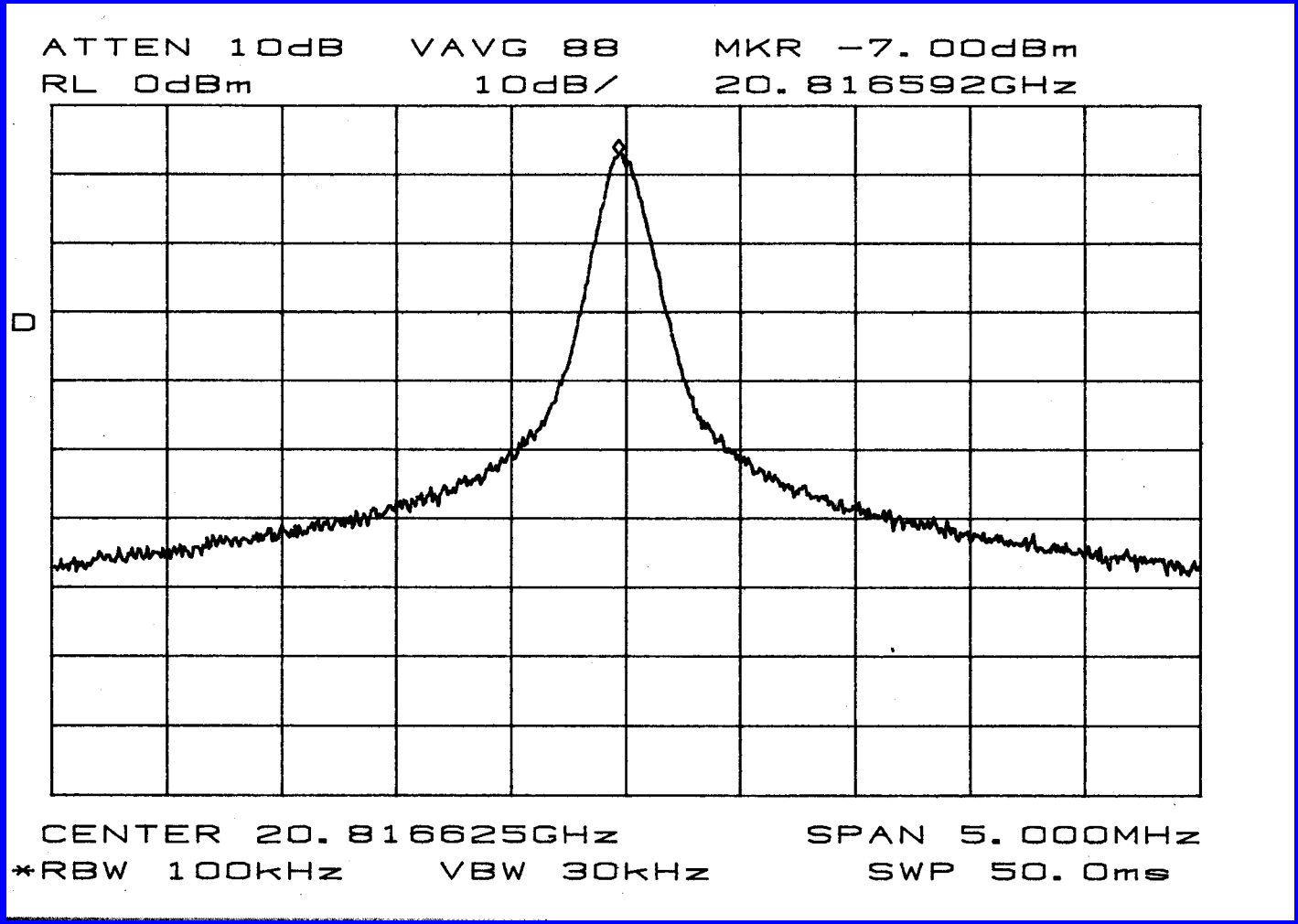
20GHz VCO Tank Tuning



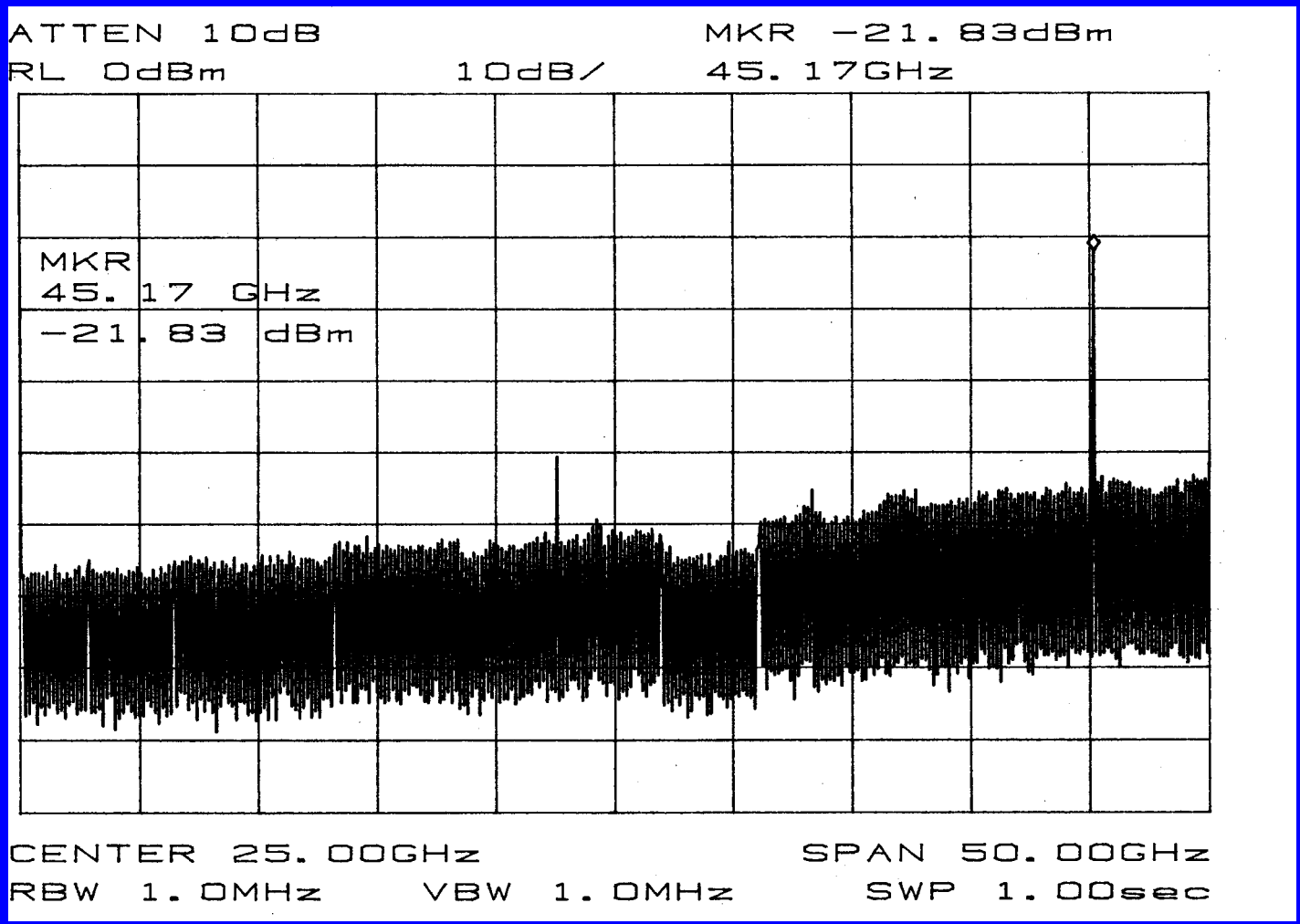
20GHz VCO Phase Noise



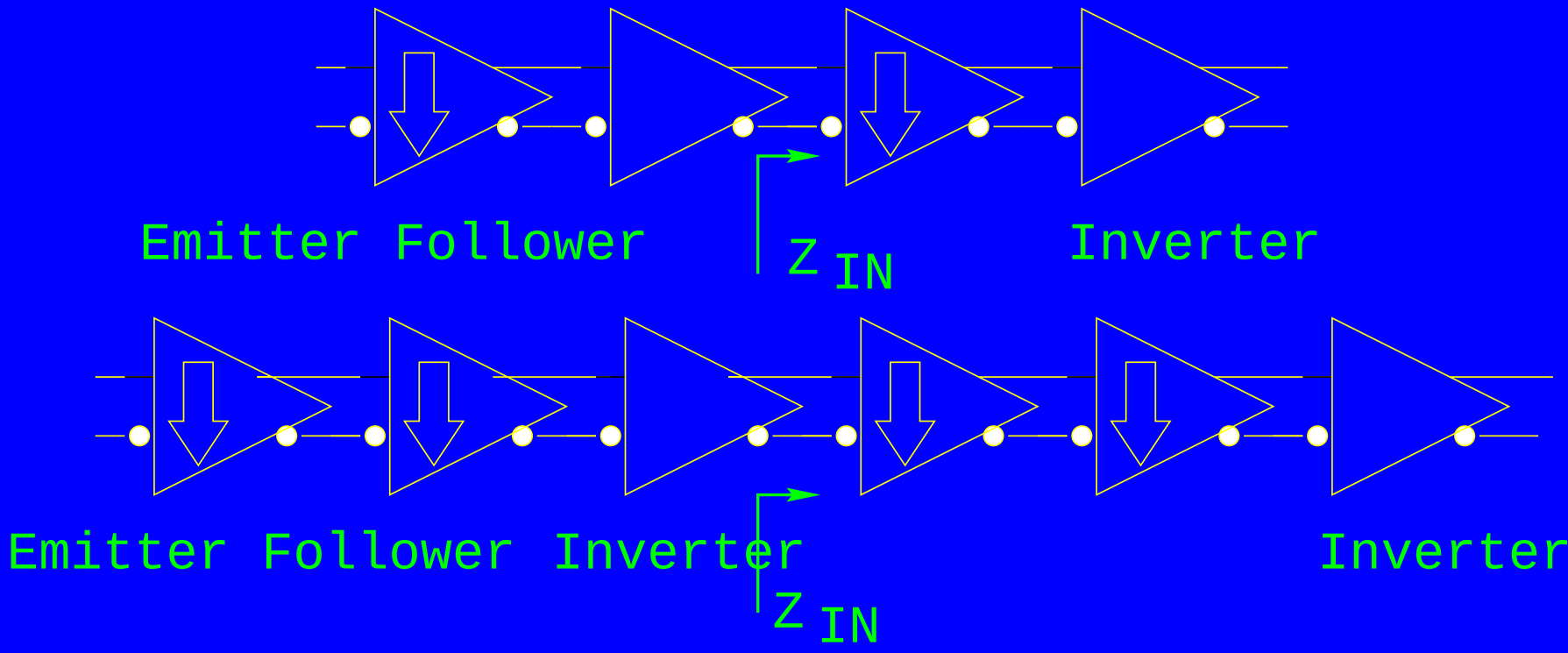
20GHz VCO Spectra



45GHz VCO Spectra



Digital Blocks: E^2CL vs. ECL



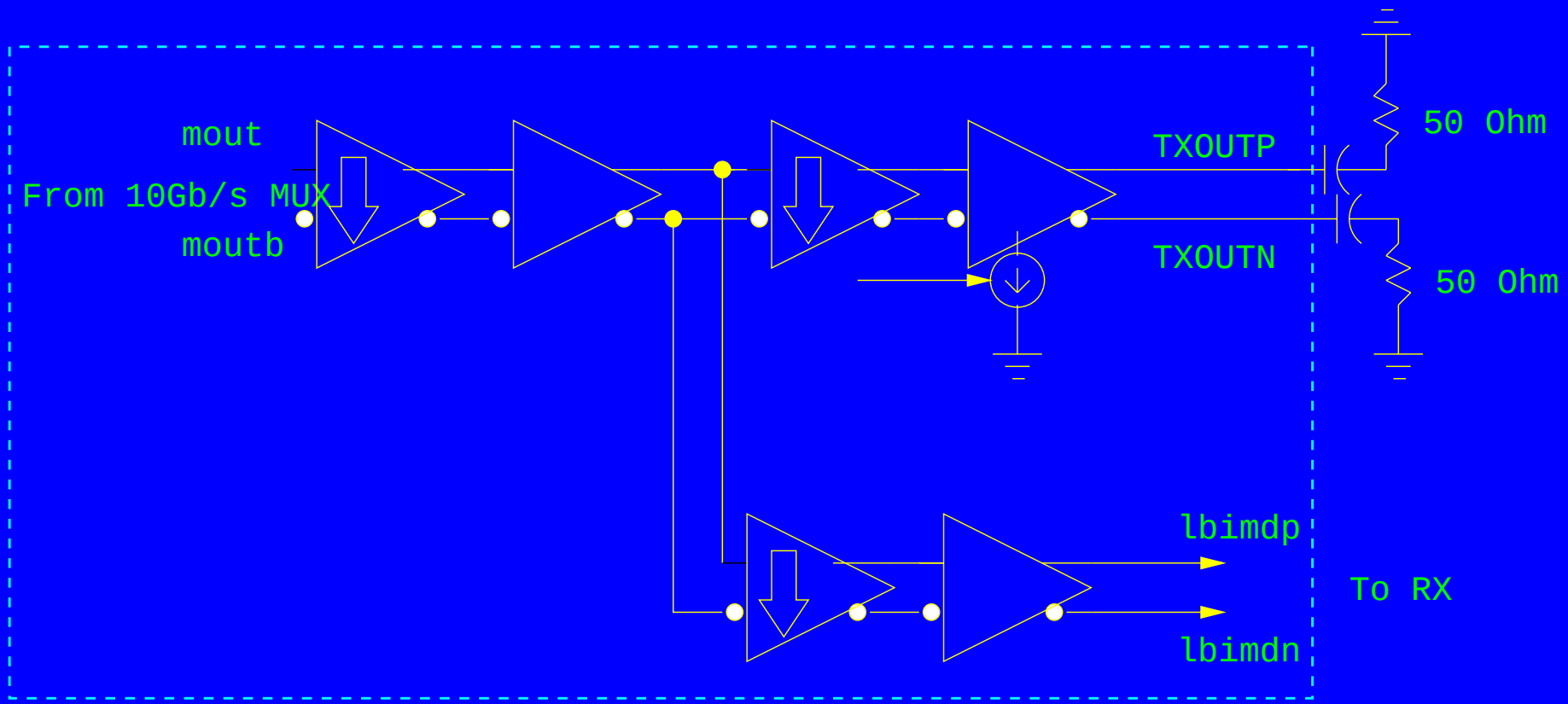
- ECL able to operate @ 3.3V in SiGe/InP
- E^2CL requires MOSFET current source @3.3V

Digital Blocks: MOS vs. Bipolar

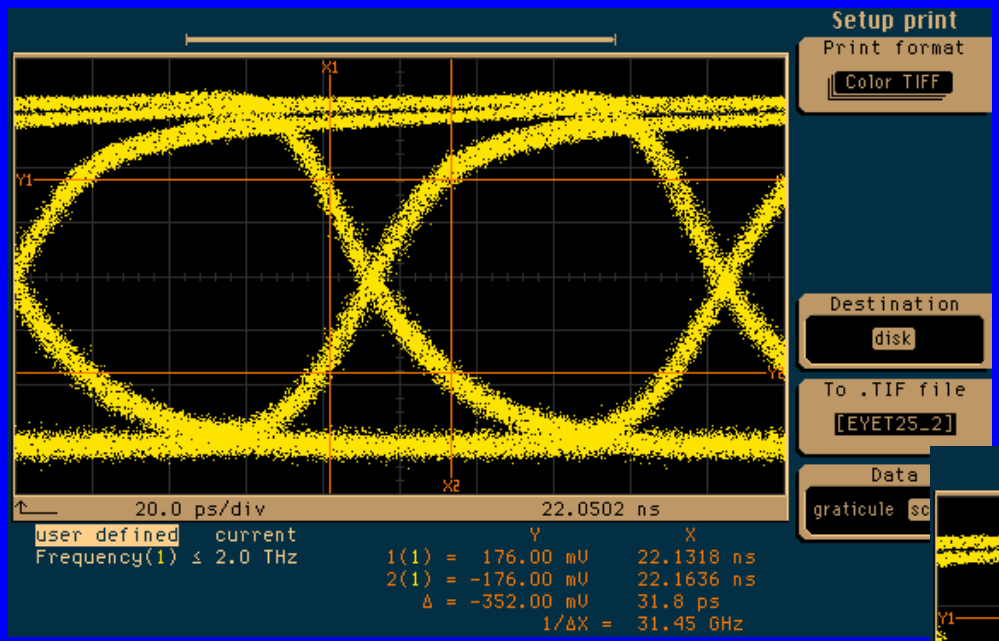
- For jitter reduction need fully differential logic
- CML/ECL-like CMOS Logic
- Less gain than bipolar => need more current
- Supply voltage: 1.2V vs. 3.3V compensates for current increase

Output Drivers

AC-COUPLED 10.3Gb/s OUTPUT DRIVER: 300mV-600mV/side

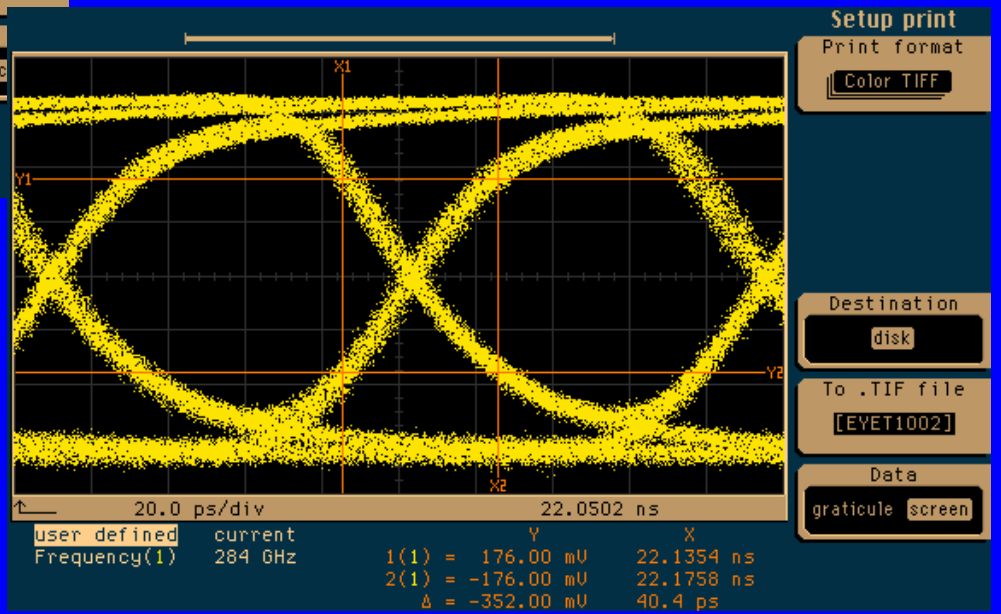


Driver with Variable Swing

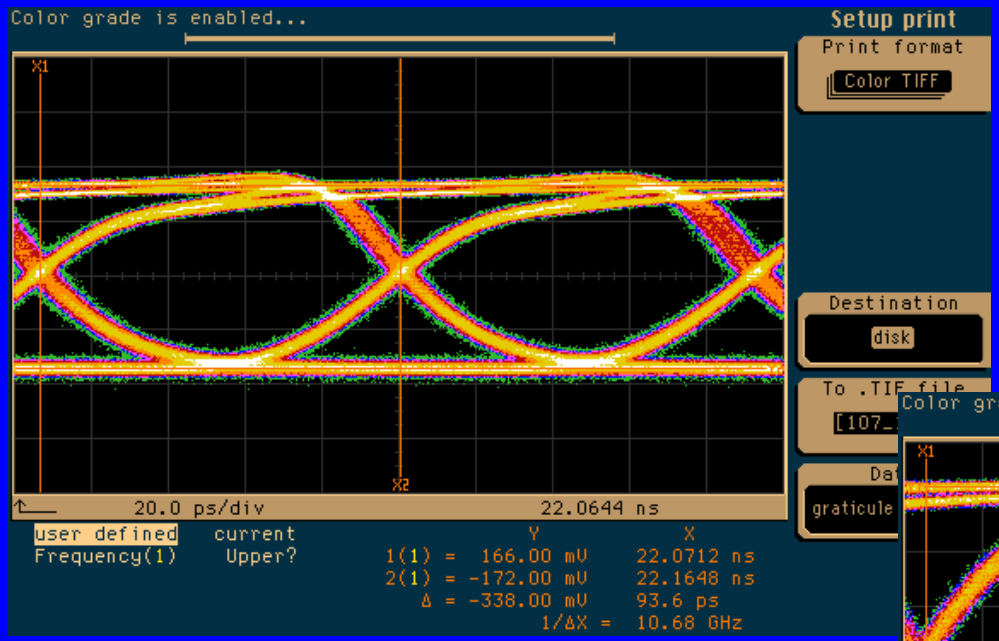


600mV p-p per side @ 25 °C

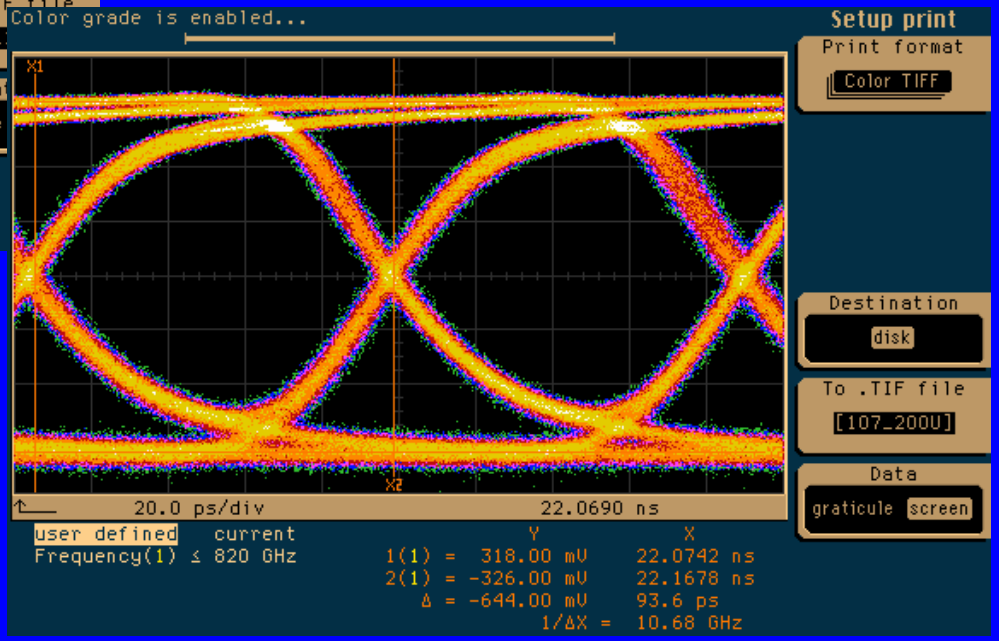
600mV p-p per side @ 100 °C



Driver with Variable Swing

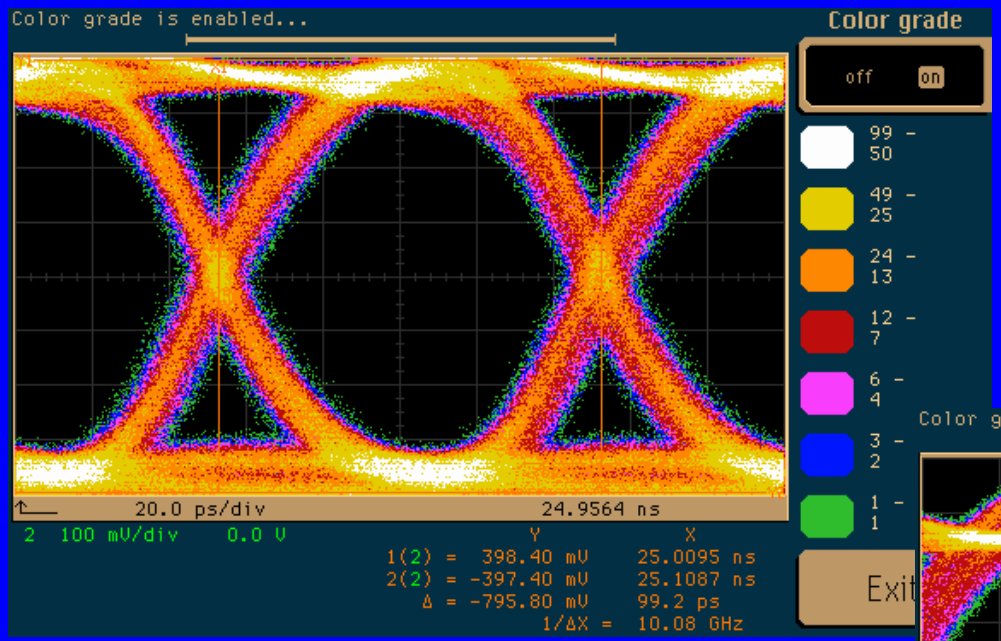


300mV p-p per side
@ 100 °C



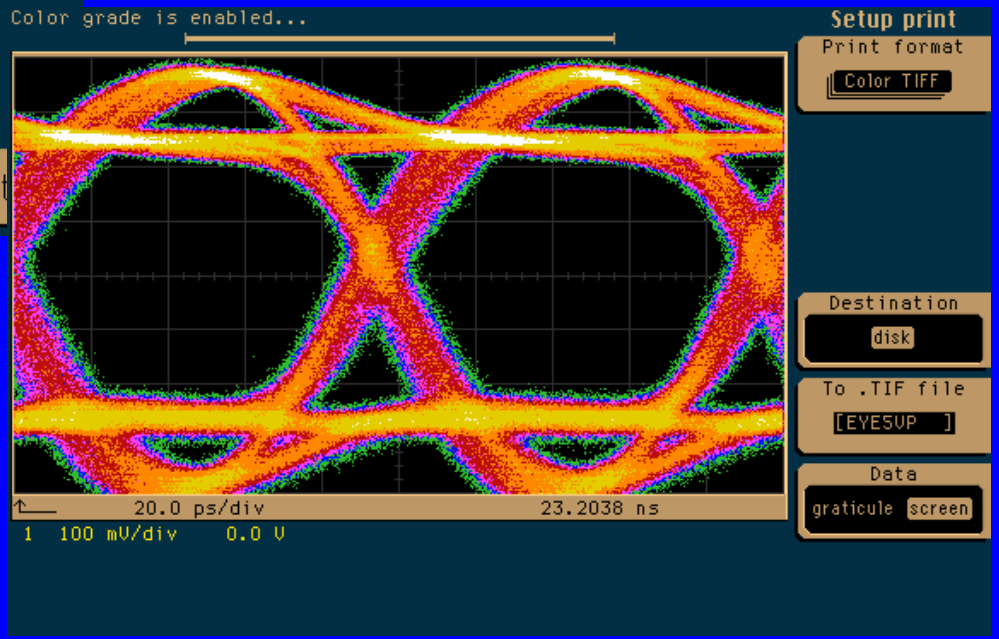
600mV p-p per side
@ 100 °C

Driver with Peaking Control

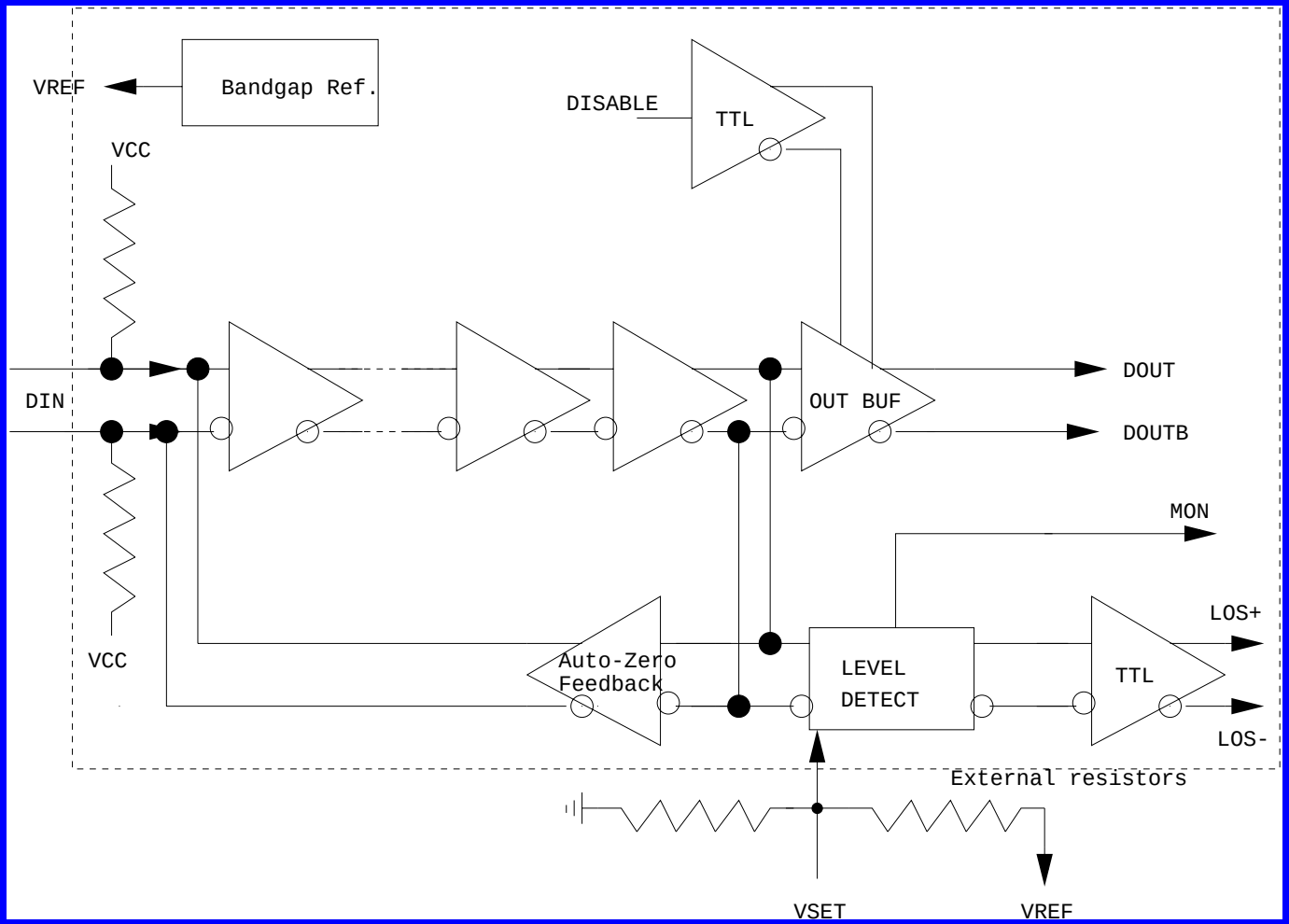


800mV p-p per side -no peaking

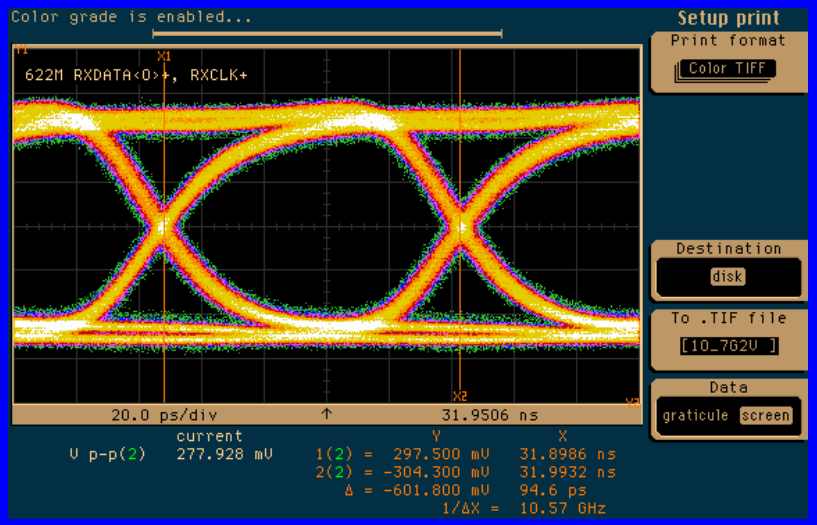
> 800mV p-p per side with peaking



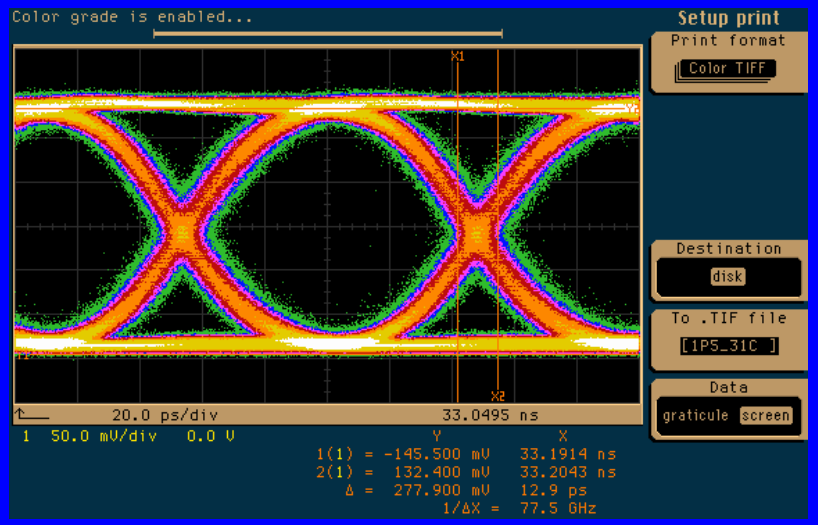
Limiting Amplifier

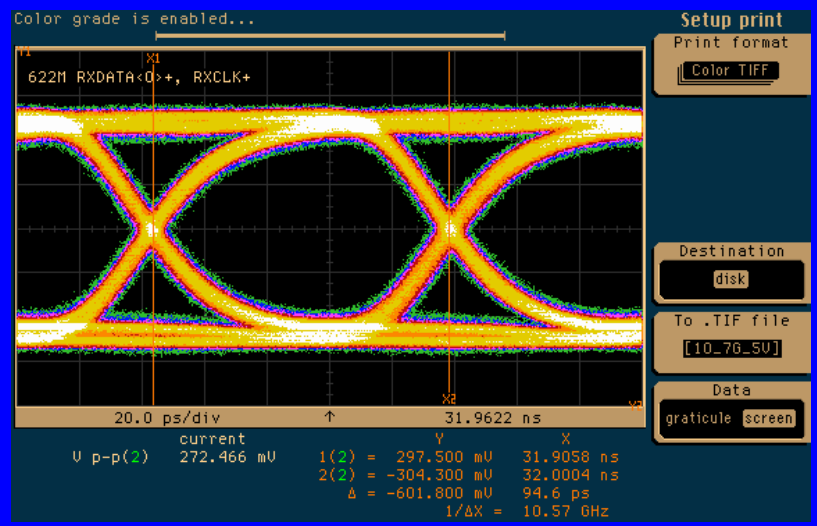


Limiting Amp10.7Gb/s, 2^{31} Eyes

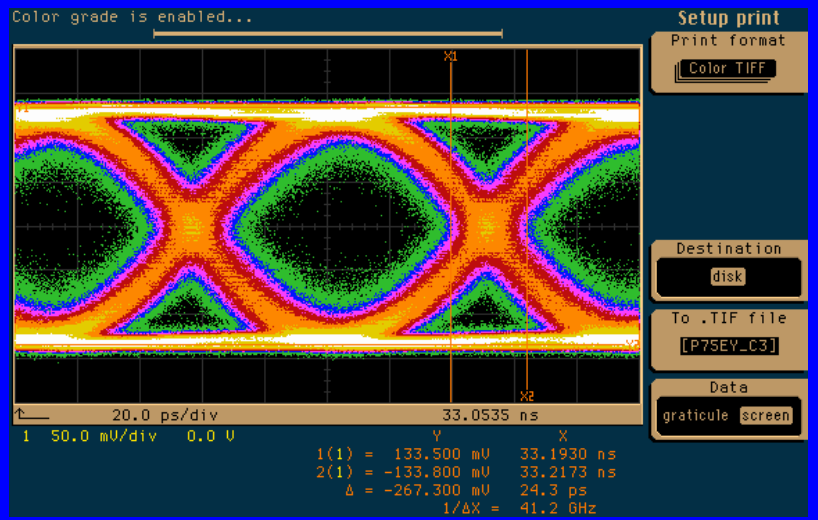


<2V input 15mV>



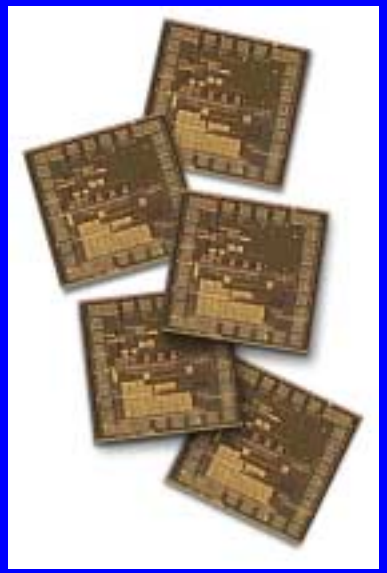


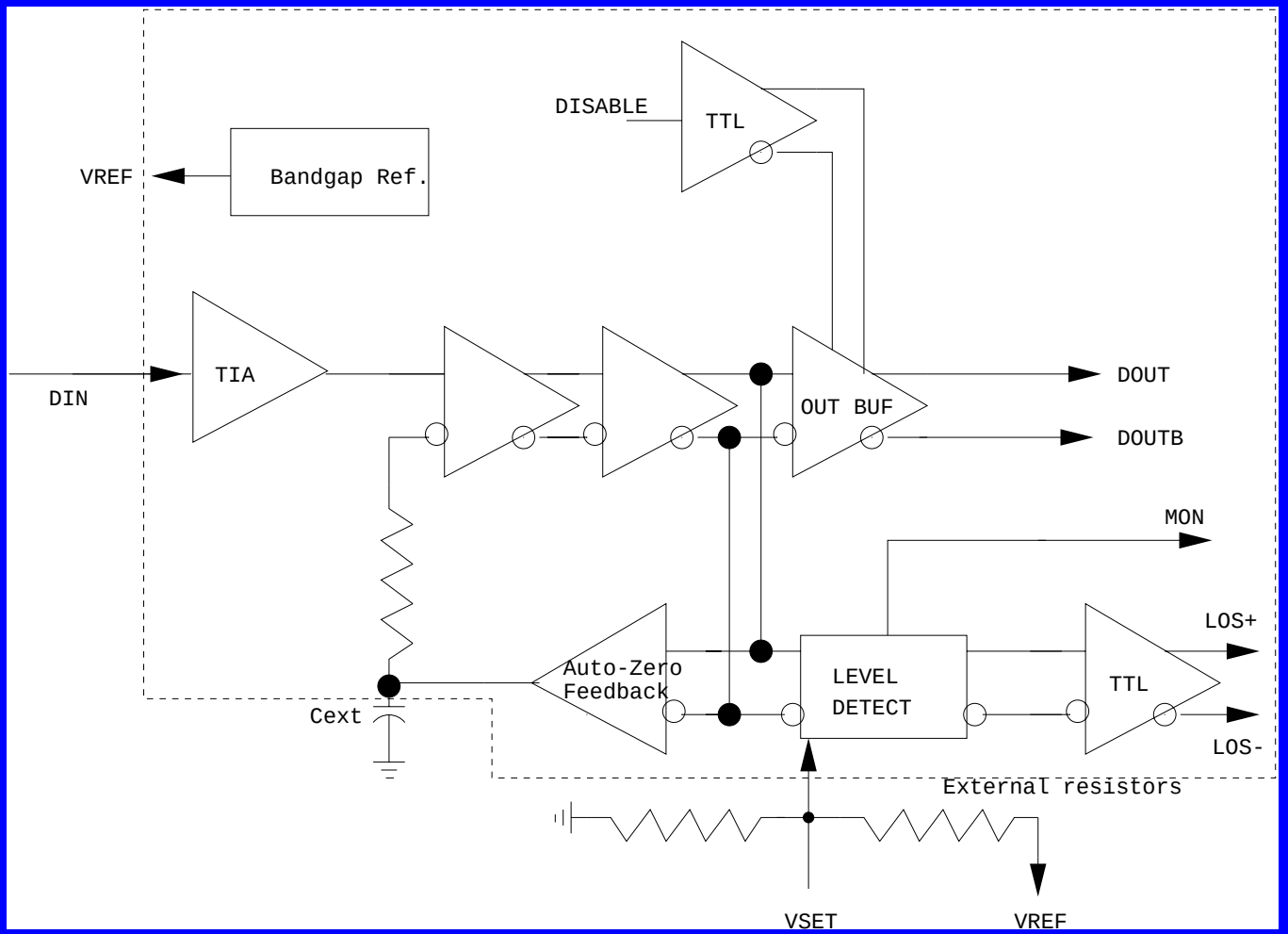
<0.5V 7mV >



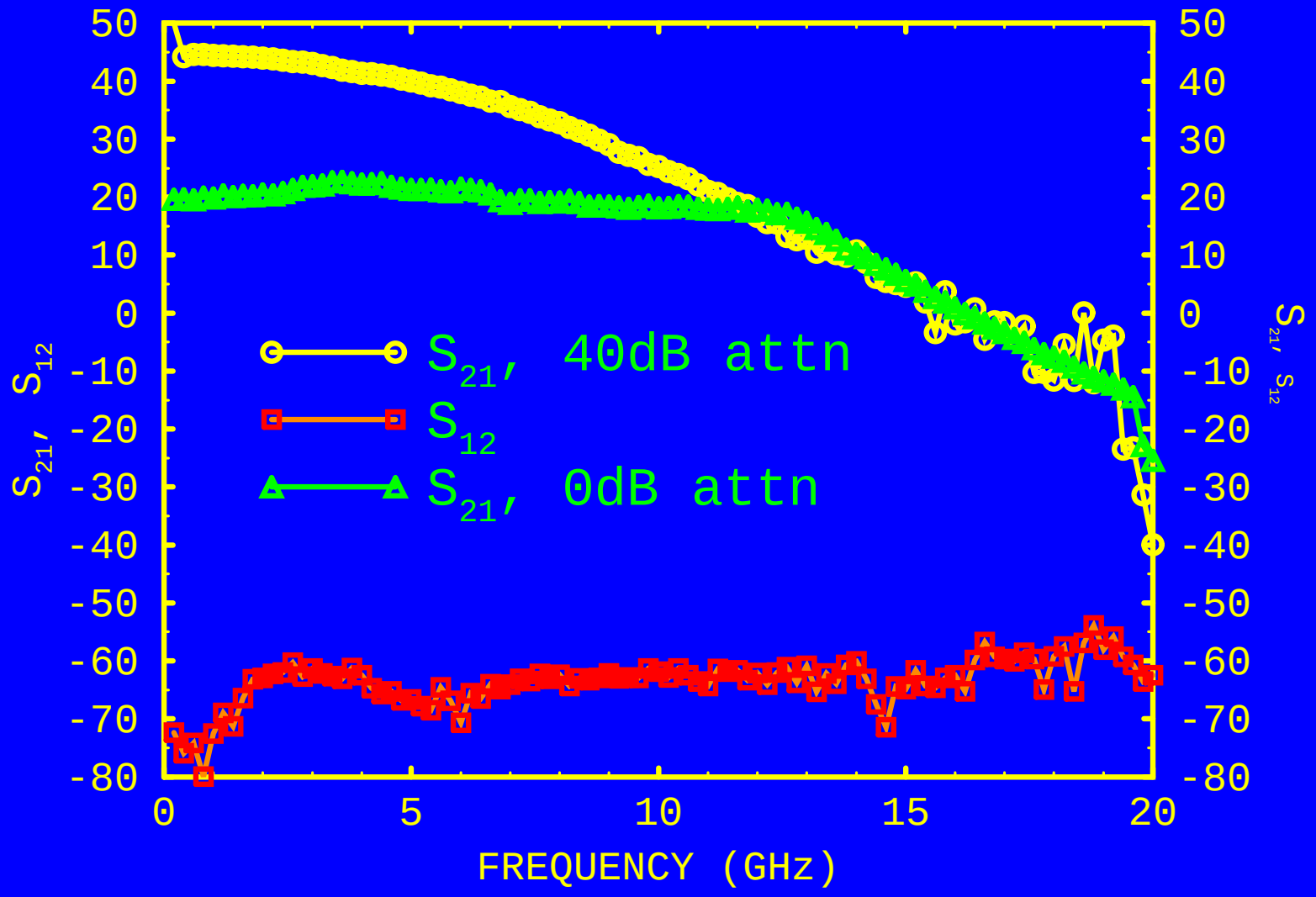
10Gb/s PHY Demo

Transimpedance-Limiting Amp

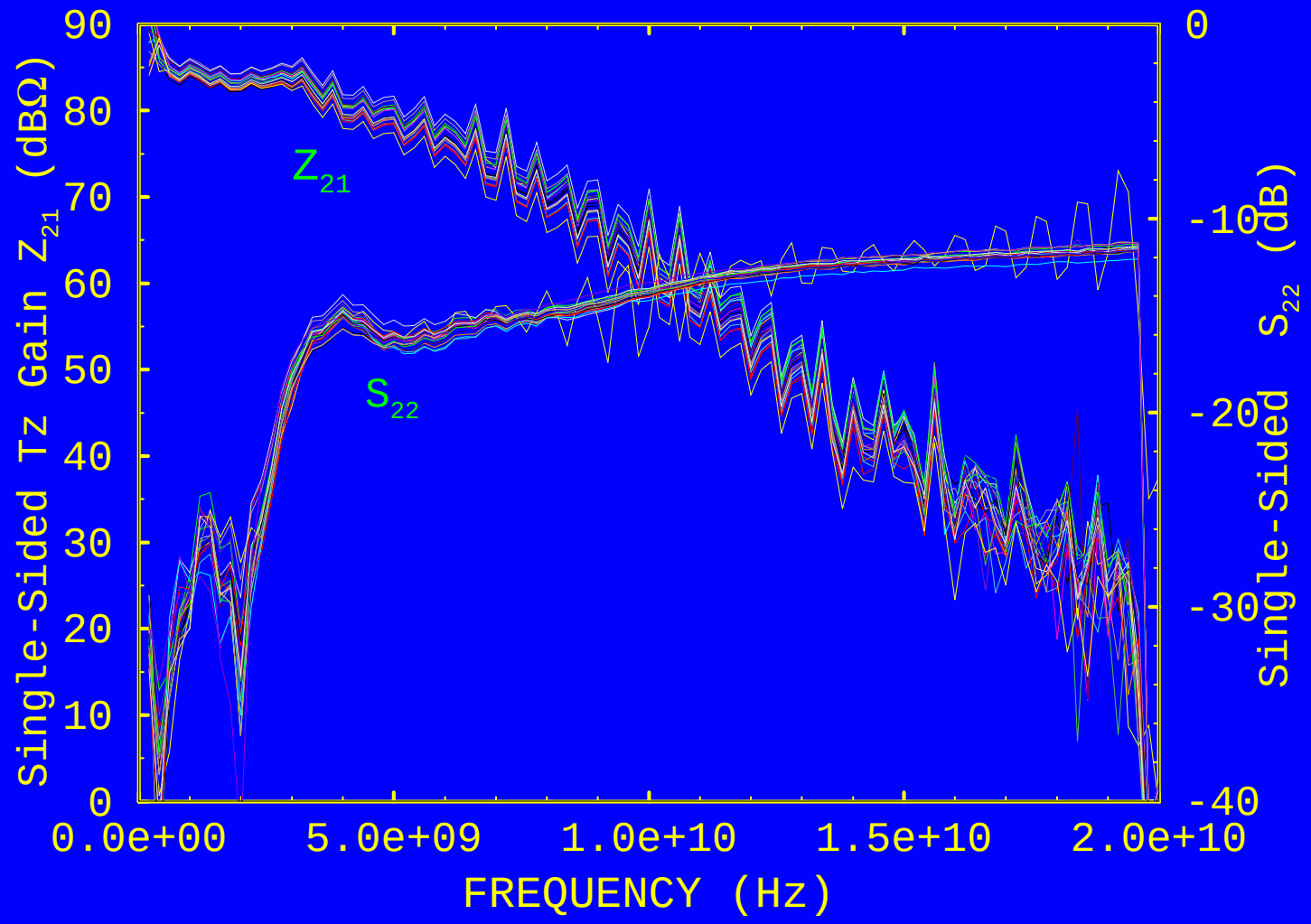




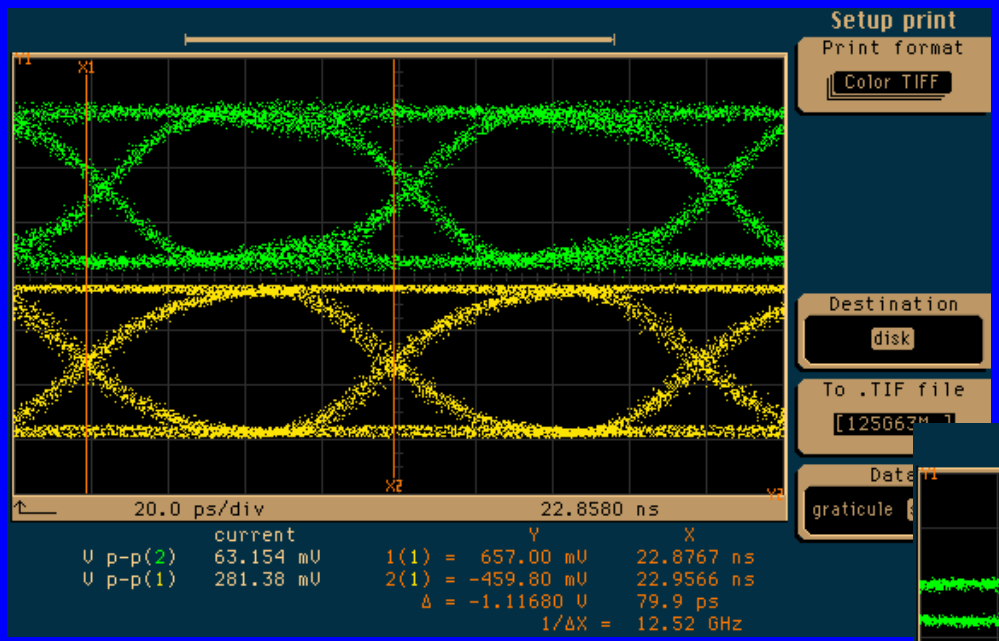
TIALA: Gain and Isolation



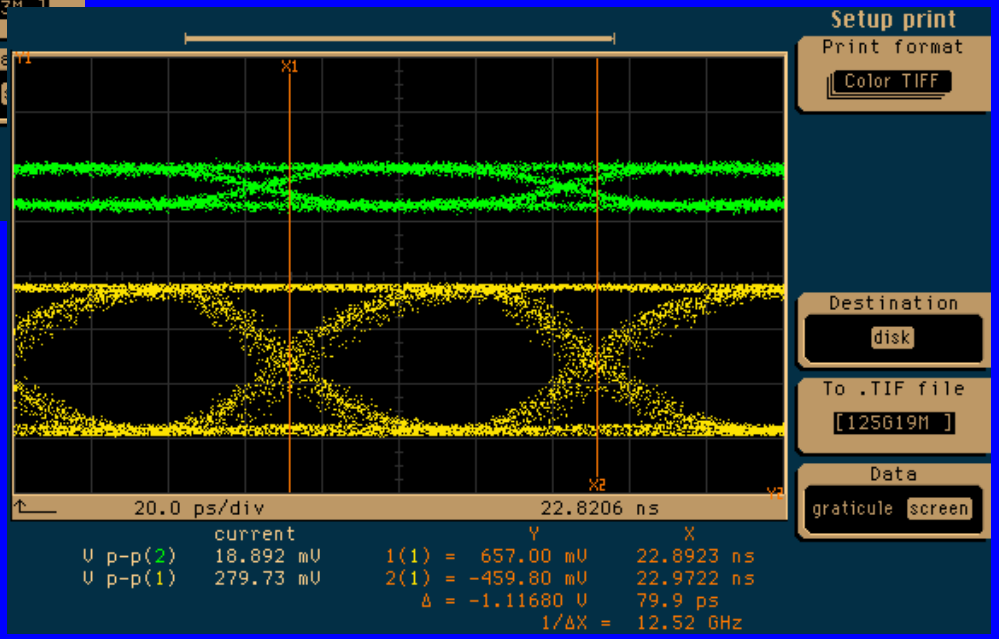
TIALA: Tz Gain & Output Match



TIALA: 12.5Gb/s Eye Diagrams



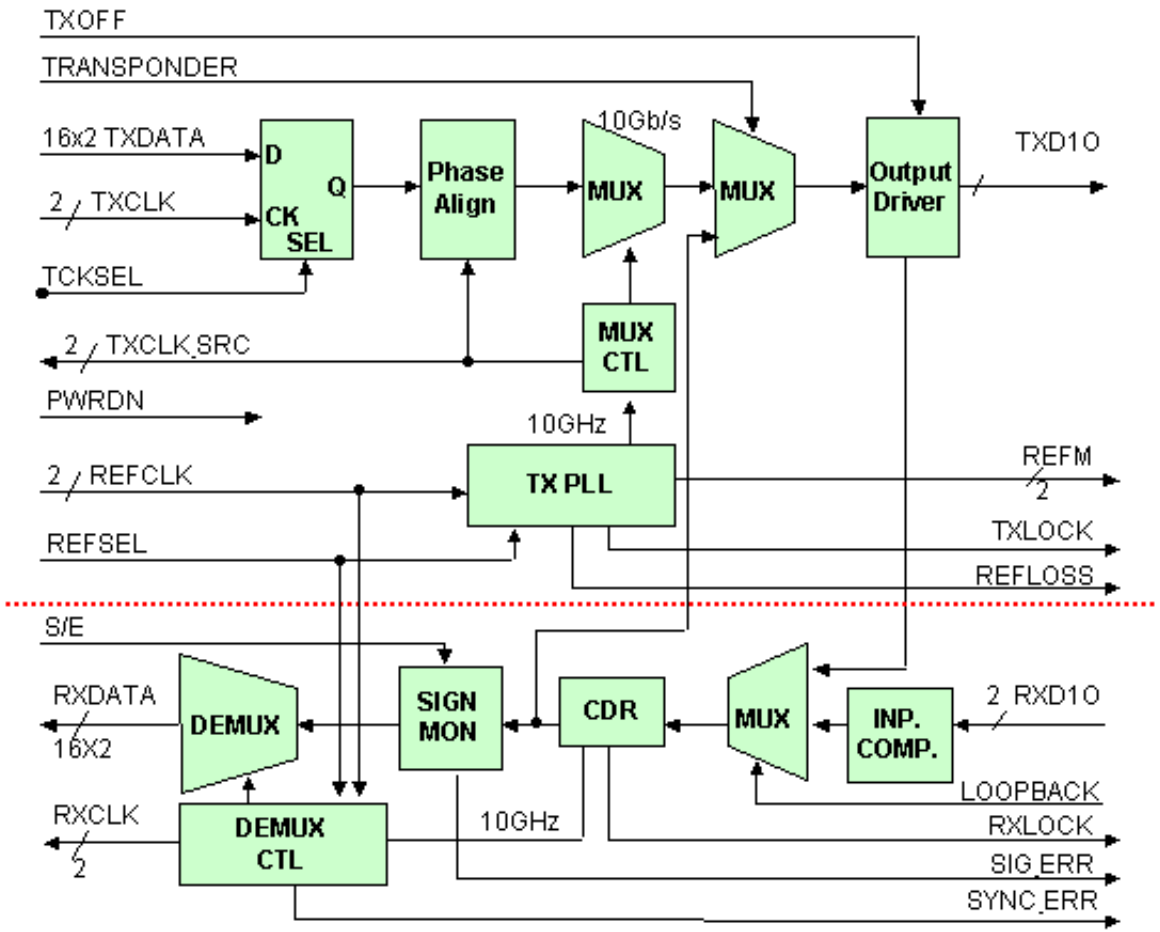
Large signal input

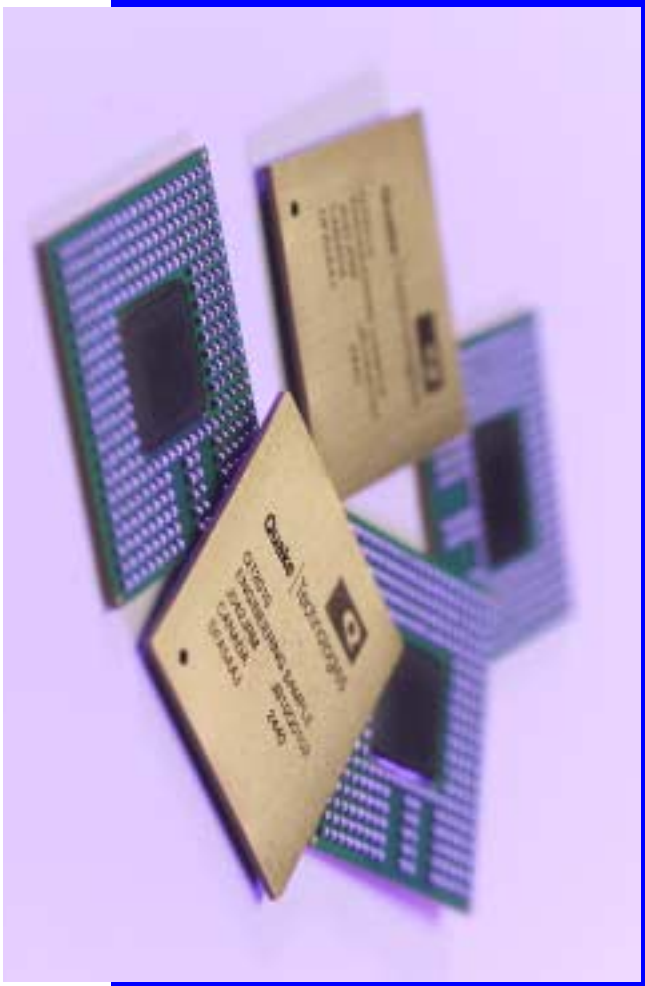


Small signal input

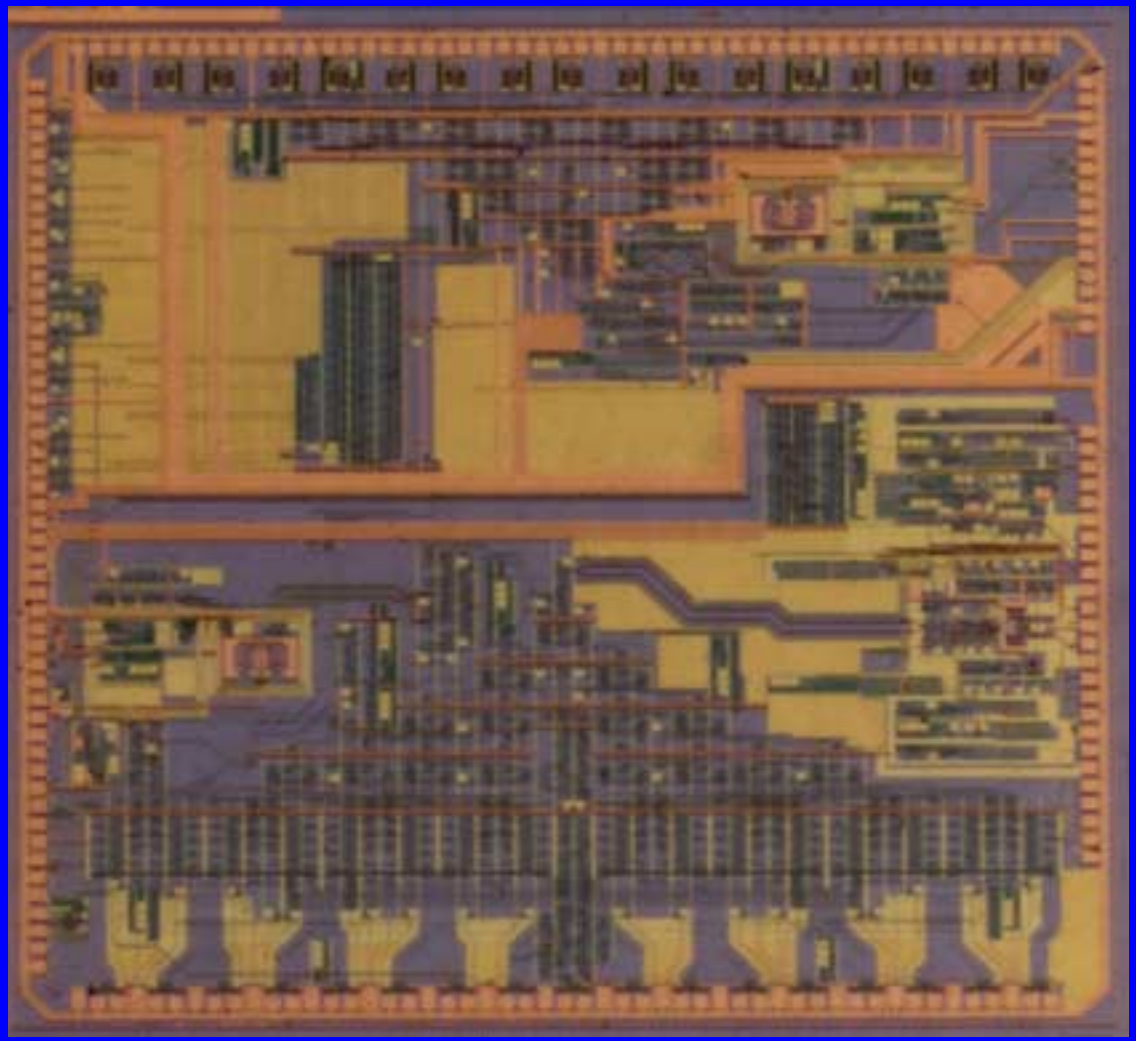
TIALA in 5 Km Fiber Loop

OIF-Compliant 10Gb/s SERDES



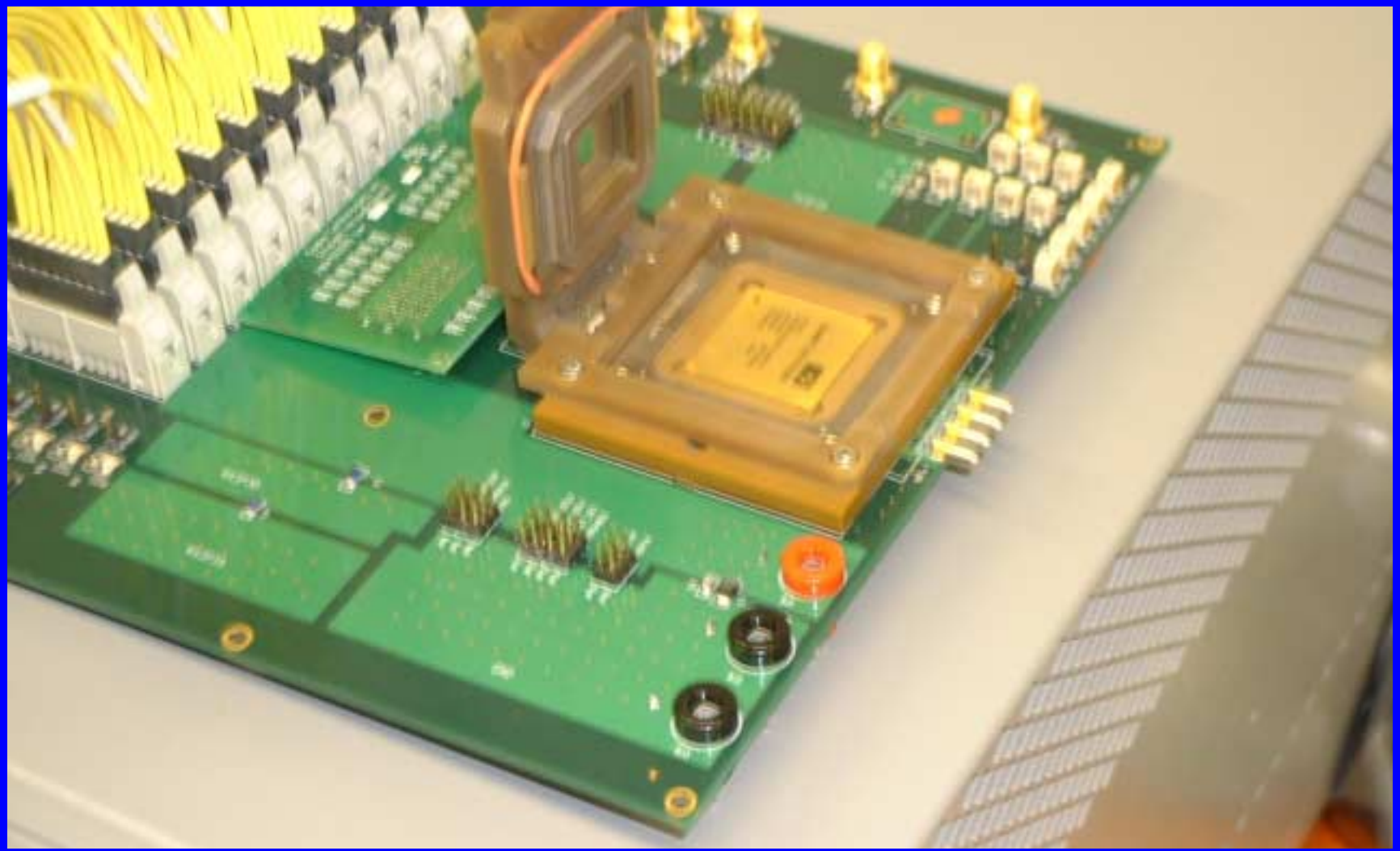


Chip Microphotograph

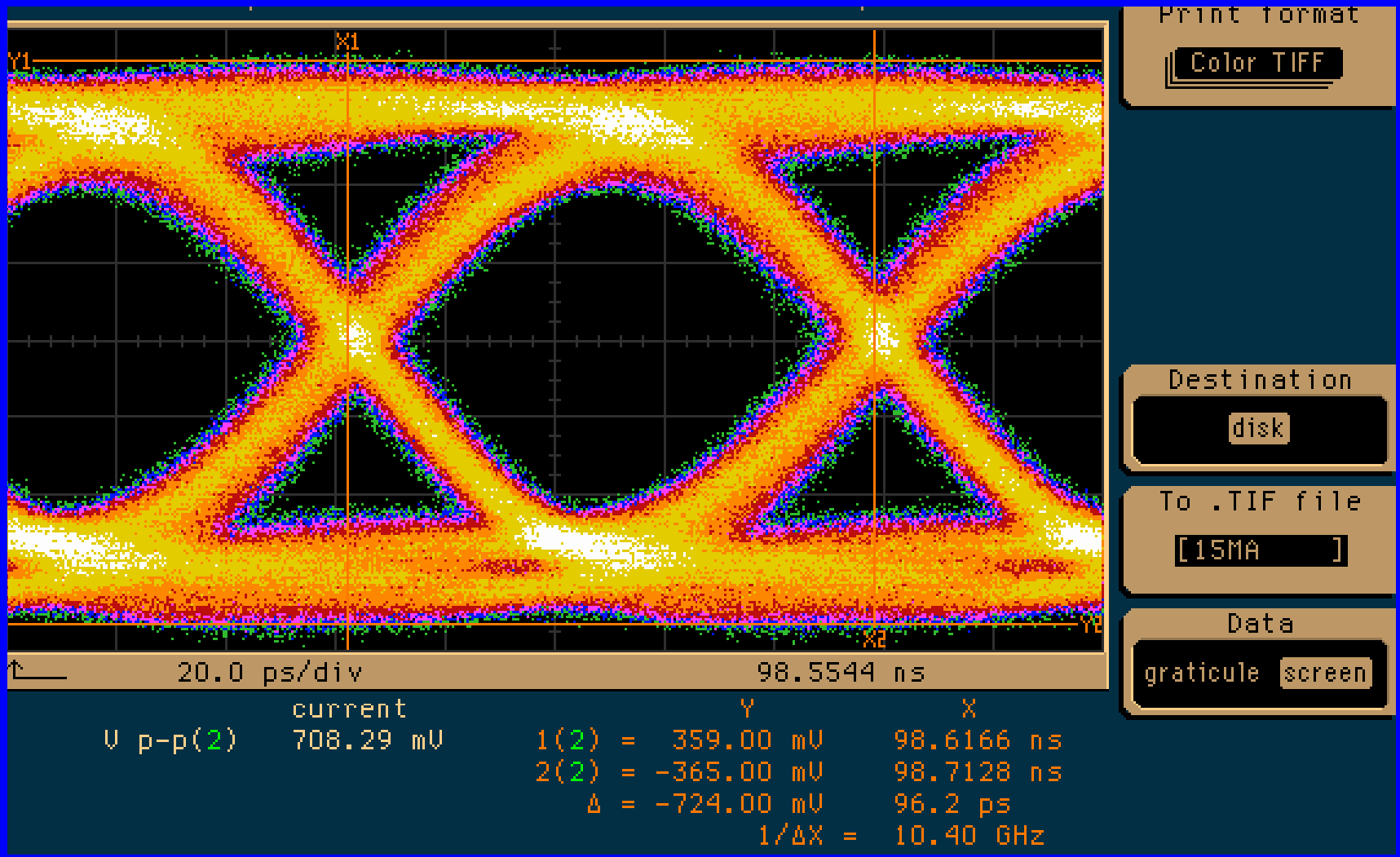


- 3.3V supply
- 2.1W
- CDR
- CGU
- 1:16 DEMUX
- 16:1 MUX
- variable output
- loopback

Evaluation Board



Eval Board Measurements



Summary

- SiGe BiCMOS and 0.12μm CMOS main contenders for 10Gb/s SERDES
- SiGe Bi(CMOS) & GaAs (MZ modulator driver) for 10Gb/s EOI functions
- Mixed InP/SiGe for 40Gb/s SERDES
- InP DHBT and GaAs p-HEMT for 40Gb/s drivers
- Demonstrated highly integrated (<2.5W, 3.3V) two-chip SERDES-TIALA solution.

Acknowledgements

Leif Larson, Aaron Shultz , Joseph Loo, Phil Luu, Tudor Savescu and Justin Chang for TIALA Fiber Loop setup and SERDES eval board design and demo.