A 1.5V 20/30 Gb/s CMOS Backplane Driver with Digital Pre-emphasis

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Abstract

A high-speed input comparator and output driver with adjustable pre-emphasis for applications in serial inter-chip communications over backplanes at 20 Gb/s is presented. The circuit was implemented in 130-nm CMOS and consumes 140 mW from a 1.5-V supply. It has over 30 dB dynamic range with a sensitivity of 20 mVp-p and a differential output swing of 700 mVp-p at 20 Gb/s. The output driver features a novel digital pre-emphasis circuit with independent pulse height and width control. Other features include 30%-70% eye-crossing control and adjustable output swing between 170 mVp-p and 350 mVp-p per side at data rates up to 30 Gb/s.

Introduction

Serial inter-chip communication is gaining acceptance over parallel architectures mostly because printed circuit board (PCB) routing and pad-limited silicon are excessively costly for commodity designs. To minimize the overall circuit area required for a serial transmitter/receiver pair, equalization can be performed at the transmitter instead of at the receiver. At the transmitter, pre-equalizers alter the wave-function to account for the low-pass response of the interconnect. Historically pre-emphasis has been achieved either using clocked flip-flops to first delay the data and then sum it with itself, or with analog differentiators that only allow for amplitude control of the pulse. The flip-flop implementation, while very robust, places severe strain on device technology since the flip-flop operates typically at twice the frequency of the driver istelf. A novel digital differentiator is presented in this paper that enables control of both amplitude and width of the pre-emphasis pulse.

40 Gb/s CMOS amplifiers [1], demultiplexers and multiplexers [2] have been recently reported. While demonstrating the high-speed potential of standard CMOS technology, these circuits suffer from limited dynamic range due to poor sensitivity and due to the modest output swing of about 100 mVp-p per side. This paper presents the first CMOS driver with duty-cycle, amplitude, and pre-emphasis control operating with over 30 dB dynamic range at data rates exceeding 20 Gbps.

Circuit Design

A. *Circuit Topology*

Fig.1 shows the block diagram of the backplane driver highlighting the four sections of the circuit. The pre-emphasis path is placed in parallel with the main signal path and the current from both output stages are summed across the 50 Ohm load resistors (not shown) to develop the differential output voltages. The parallel path consists of delay buffers, and the digital differentiator circuit. The output swing is adjusted from the tail current of the output buffer while the amount of pre-emphasis is controlled by the tail current of the last stage in the pre-emphasis path.

B. *Transistor sizing and biasing for high-speed*

The f_T and g_m of a 130-nm n-MOSFET vary linearly with V_{GS}-V_T for effective gate voltages less than 0.25 V and reach their peak at 0.4 V, corresponding to a drain current density of 0.25 to 0.3 mA/μm. This behaviour is illustrated in Fig. 2. MOS-CML gate voltage swings far exceeding 400 mVp-p will therefore lead to unnecessary power dissipation without any improvement in speed. Based on this observation, every circuit block consists of a MOS-CML inverter whose tail current is set to correspond to the peak f_T bias of the n-channel MOSFET of 0.25 mA/μm. This bias scheme ensures the maximum switching speed with a voltage swing of 450 mVp-p. Inductive peaking is employed in every stage to further improve the bandwidth.

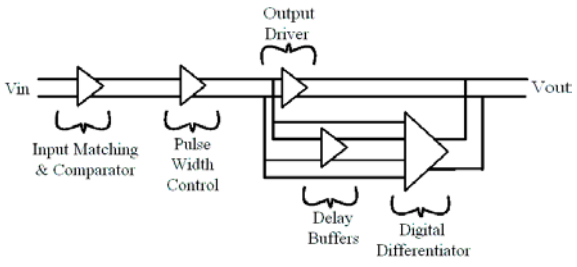

Fig. 1: Backplane driver topology

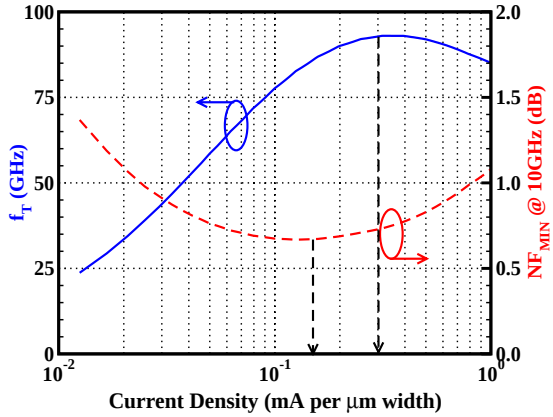

Fig. 2: f_T and NF_{MIN} versus current density for a 130-nm n-MOSFET with 2 μm unit finger width biased at V_{DS} = 1V.

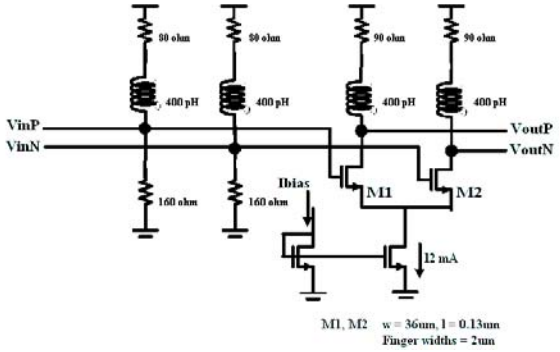

Fig. 3: Input matching network and comparator

C. *Input Matching and Low-noise Comparator*

Fig. 3 shows the input matching network and low-noise comparator. The input differential pair has higher-gain and larger tail current than the other stages in order to reduce the noise. A compromise was reached between achieving the best possible noise match, which calls for large transistor sizes and bias current, and broadband input impedance match. On-chip matching resistors, implemented as a resistive divider with series inductors, provide the gate bias of the input transistors.

D. *Eye-Crossing Control*

The pulse-width control circuit, illustrated in Fig. 4, consists of two inductively-loaded differential stages with a DC offset control pair connected at the output of the first stage. By applying a DC voltage between *Vpos* and *Vneg*, an offset voltage is developed on *VmidDIFF*, shifting the zero-crossing between the two outputs. Due to the finite rise and fall time of the waveform, after truncation by the limiting action of the second inverter, *Vout* exhibits a change in duty-cycle.

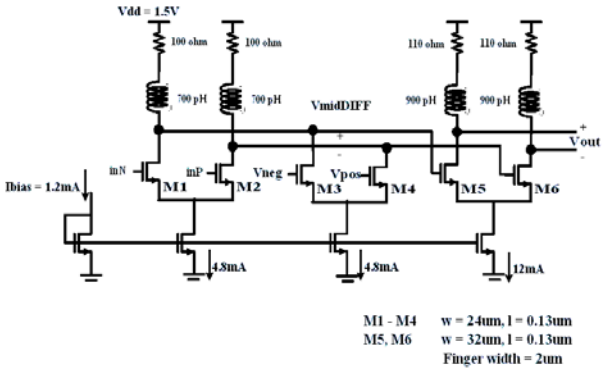

Fig. 4:Pulse-width control circuit and operation

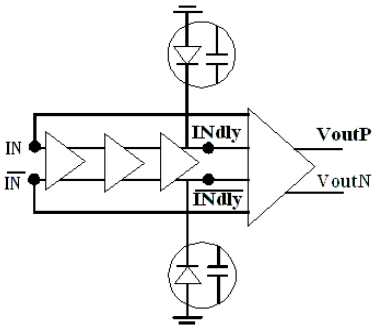

Fig. 5: Digital pre-emphasis block

E. *Digital Pre-emphasis*

The digital pre-emphasis circuit whose block diagram is shown in Fig. 5 features three delay cells, implemented as inverters, followed by a digital differentiator circuit. The third delay cell employs varactor diodes connected in parallel with resistive loads in order to control the delay and, therefore, the pre-emphasis spike width.

Fig. 6 illustartes the waveforms in the digital differentiator. The circuit has two differential inputs *IN*, $\overline{IN}$ and *INdly*, $\overline{INdly}$, and a differential output *Voutp*, *Voutn* which is summed with the currents from the main path across the on-chip 50 Ω load resistors.

The logical function is identical to that of a digital XOR gate, with the exception that the output of the digital differentiator operates as a tertiary (three-level) logic system. The pre-ephasis spike height is controlled by two constant current sources *Iswch* whose value is adjustable bewteen 0 and 10 mA. Finally, transistors M3 and M6 compensate the V_{DS} drop across transistors M1,M2 and M4,M5, respectively.

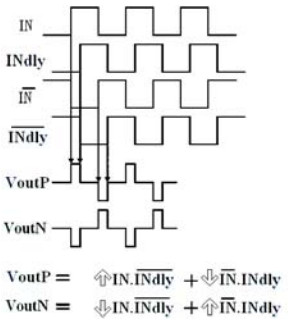

Fig. 6: Pre-emphasis waveforms and transfer function

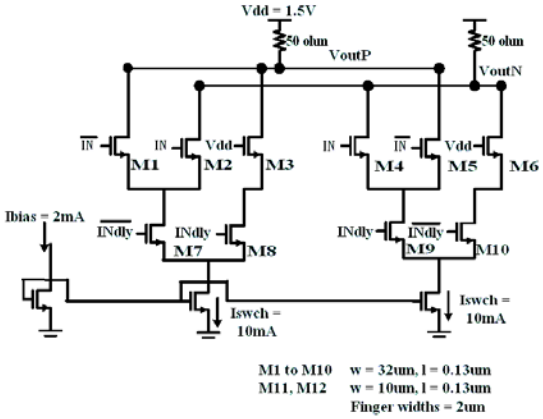

Fig. 7: NMOS Digital differentiator

Fabrication

The circuit was fabricated in STMicroelectronics' 130 nm standard CMOS process with typical n-MOSFET f_T and f_{max}. of 90 GHz and 100 GHz, respectively. The chip microphotograph is reproduced in Fig. 8. The design is pad-limited and the area of the design around the outside of the pads is 1.0mm x 0.5mm. Power and ground signals were placed along the central horizontal line. Transistors and poly-silicon resistors are located adjacent to the central line, followed by signal path routing, and with the load inductors on the outside. Each of the 18 inductors was implemented with 3-D stacked-spiral layouts and the area occupied by each inductor is less than 40µm x 40µm.

Experimental Results

The circuit was fully tested on wafer. The small signal S parameters and noise figure were measured in a single-ended configuration. The input and output return loss is better than -12 dB up to 50GHz, as shown in Fig. 9. The differential small signal gain was be 18dB, also confirmed in large by the eye diagram measurements of Fig. 10. The single-ended noise figure is 16 dB, 2-dB higher than simulation.

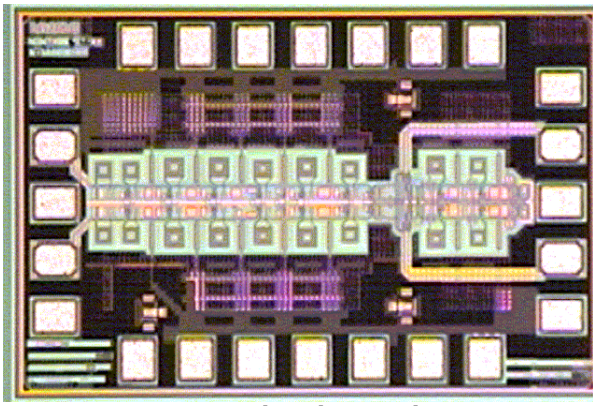

Fig. 8: Chip Photograph

Time domain measurements were performed with an Anritsu 40 Gb/s BERT specified between 25Gb/s and 43 Gb/s and a PRBS pattern of 2^{31} - 1. At 20 Gb/s the BERT operates out of range with significantly more jitter than at 25 Gb/s or 30 Gb/s. A sensitivity of 20 mVpp, as illustrated in Fig. 10, was measured at 20 Gb/s when the input was applied single-endedly and the unused input was terminated with a 50-Ω load. The sensitivity degraded to 60 mVp-p, and 150 mVpp, at 25 Gb/s and 30 Gb/s, respectively.

Typical 30 Gb/s and 25 Gb/s output eye diagrams are illustrated in Figs. 11 and 12, respectively. Fig. 13 demonstrate 40% to 60% eye-crossing control at 25Gb/s.

Fig. 14 shows output amplitude control at 20 Gb/s. The input signal in both diagrams is 200mVpp, applied to one side only, and the output is varied between 170mVpp and 340mVpp. The measured waveforms with pre-emphasis at 20Gb/s are reproduced in Fig. 15. The eye-diagram exhibits higher positive overshoot than undershoot. Table 1 summarizes the overall circuit characteristics.

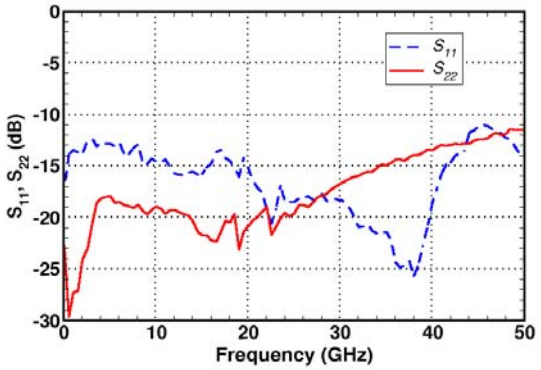

Fig. 9: Measured single-ended S_{22} and S_{11}

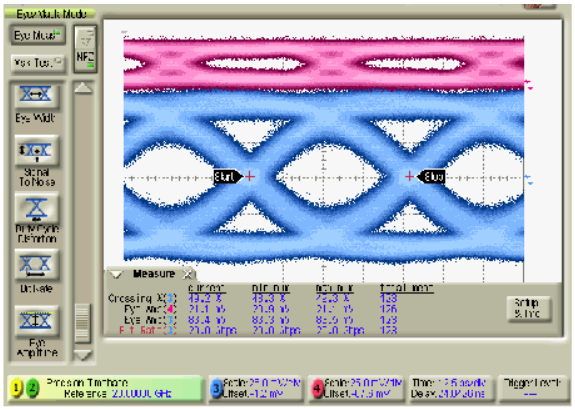

Fig. 10: 20Gb/s eye-diagrams 2^{31}-1 PRBS: single-ended input 21 mVpp, differential output 84mVpp per side

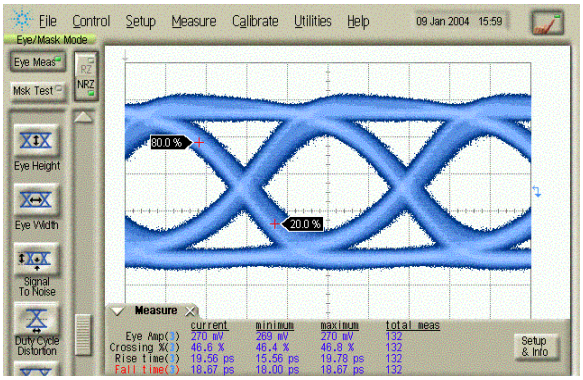

Fig. 11: 30 Gb/s output eye-diagram with 260 mVpp per side for a single-ended 200 mVpp, 2^{31}-1 input PRBS.

Conclusions

A 20 Gb/s backplane driver with more than 30 dB dynamic range was implemented in 130-nm CMOS technology. The circuit consumes 150 mW from a 1.5 V supply and features output swing, duty cycle and pre-emphasis control. The circuit is operational without pre-emphasis at data rates up to 30 Gb/s with 300 mVp-p swing per side.

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References

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[2] D. Kehrer, H.D. Wohlmuth, "40 Gb/s 2:1 Multiplexer and 1:2 Demultiplexer in 120 nm CMOS," *IEEE ISSCC Digest*, pp. 345-346, 2003

[3] D.S. McPherson et al., *JSSC*, Vol.9, pp.1485-1496, 2003.

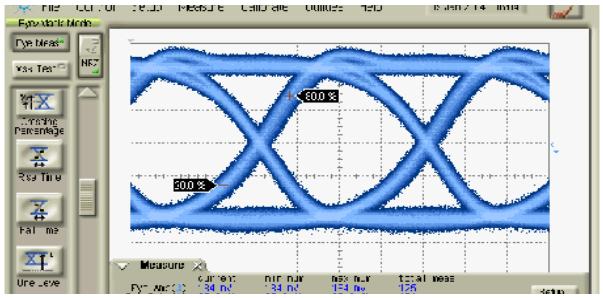

Fig. 12: 50% Output eye-crossing control at 25Gb/s

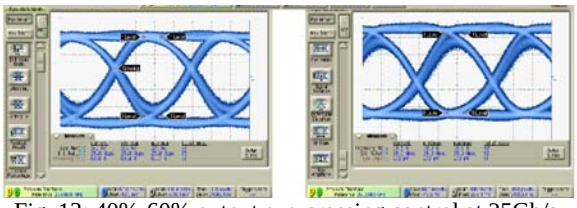

Fig. 13: 40%-60% output eye-crossing control at 25Gb/s

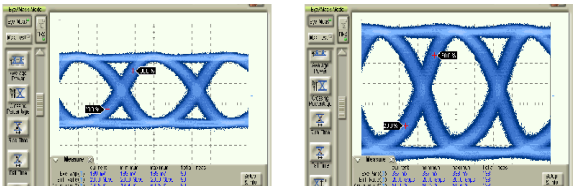

Fig. 14: Output amplitude control at 20 Gb/s: output of 170 mVpp and 340 mVpp per side, respectively.

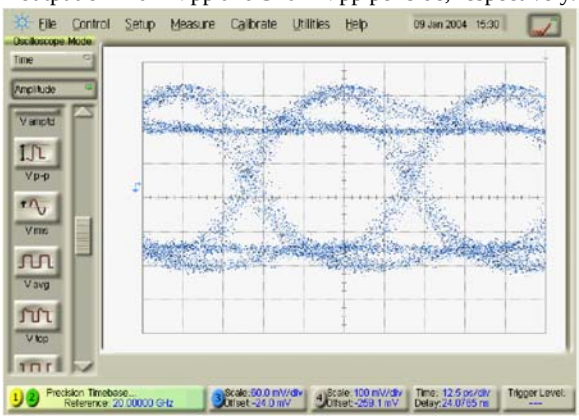

Fig. 15: 20Gb/s output eye diagram with 300 mVpp swing per side and pre-emphasis.

Table 1: Measured Circuit Parameters

Parameter	Measured value
supply	1.5 V
Power	150mW
Output Swing @ 20 Gbps	170-350mVpp
Pre-emphasis Control @20 Gbps	30%
Crossing Control @ 20 Gbps	30% to 70%
Eye sensitivity @ 20 Gbps	20(10)mVpp
Noise Figure	16 dB
S11/S22 up to 50 GHz	<-12 dB