A 1-Tap 40-Gbps Look-ahead Decision Feedback Equalizer in 0.18μm SiGe BiCMOS Technology

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***Abstract*— This paper describes a fully-differential 1-Tap decision feedback equalizer (DFE) in 0.18μm SiGe BiCMOS technology. The circuit is capable of equalizing NRZ data up to 40 Gbps. A look-ahead architecture is used with modifications to reduce complexity in the high speed clock distribution. An analog differential voltage controls the tap weights. The design is fabricated in 0.18μm SiGe BiCMOS technology with a 160-GHz f_t. It occupies an area of 1.5mmX1mm and operates from a 3.3V supply with 230mA current. It is the first feedback equalizer at 40 Gbps in silicon.**

I. Introduction

Dispersion compensation, particularly polarization-mode dispersion (PMD), can be accomplished through a variety of means, both optical and electric. Compelling arguments in [1] and [2] push towards an electrical solution involving a mixed-signal decision feedback equalizer (DFE). Previous work presented by [3] show the implementation of the feed forward portion of the DFE. This work focuses on the design of the feedback equalizer.

Recent publications [4], [5] have shown operation of DFEs up to 10-Gbps in both CMOS and SiGe BiCMOS technology. The fastest feedback equalizer to the authors' knowledge is in III-IV technology at 40-Gbps [6] which utilizes a modified feed forward architecture with 2 delay elements. This work presents the first 40-Gbps DFE in silicon. It uses a well-known, proven look-ahead architecture. In addition, the chip is fabricated in a BiCMOS technology which allows for integration of adaptation algorithms on chip.

The following sections highlight the circuit design of the feedback equalizer and implementation issues, followed by the measurement results and verification performed at 40 Gbps.

II. Circuit Design

The topology of the DFE is a look-ahead architecture originally proposed in [7]. This architecture is different from the conventional (direct) feedback equalizer since filter processing is removed from the feedback path to help alleviate tight timing constraints. Unlike the high-speed implementation discussed in [7], retiming of the selector inputs has been replaced with slicers to remove considerable complexity in the clock path, clock skew management and overall power. A block level view of the chip can be seen in Fig. 1.

A shunt feedback input buffer stage (topology commonly known as a transimpedance amplifier (TIA)) is used as a voltage preamplifier for low noise and large bandwidth

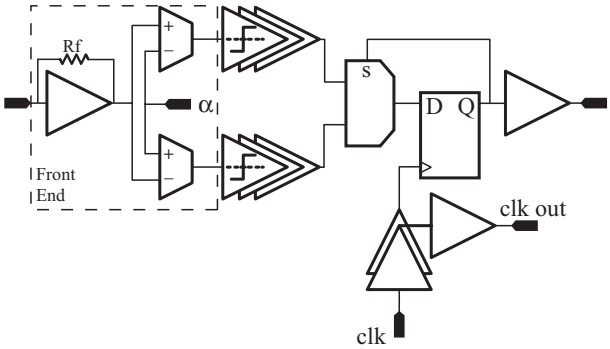


Fig. 1. Look-ahead DFE chip block level architecture

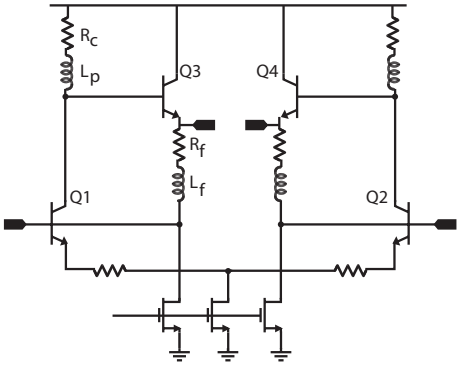


Fig. 2. Schematic of input shunt feedback (TIA) stage

(Fig. 2). Unlike conventional input amplifiers, it provides simultaneous input impedance and noise matching without limiting bandwidth [8]. The output of the shunt feedback buffer is fed into a slicing threshold adjustment block which varies the differential DC offset of the output via the α control voltage. This effectively changes the slicing threshold into the 3 cascaded ECL buffers that limit the signal. Each path acts as an equalizer to cancel post cursor intersymbol interference (ISI). The slicer output feeds into the Decision Selective Feedback (DSF), where the DSF selects one of the paths based on the previous decision of the flip flop. The output of the flip flop is driven off-chip via an output driver with variable swing. The clock path features 2 stages of E^2CL buffers, and is also made available off-chip for possible testing purposes.

The threshold adjustment circuit (Fig. 3) applies a differen-

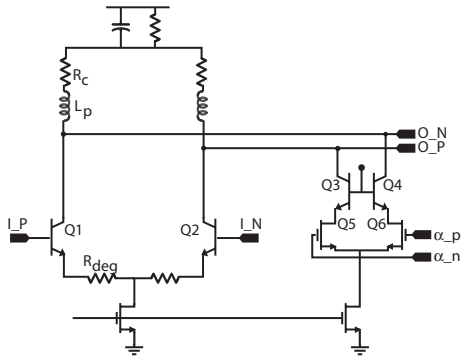


Fig. 3. Schematic of slicing threshold adjustment circuit for ISI cancellation

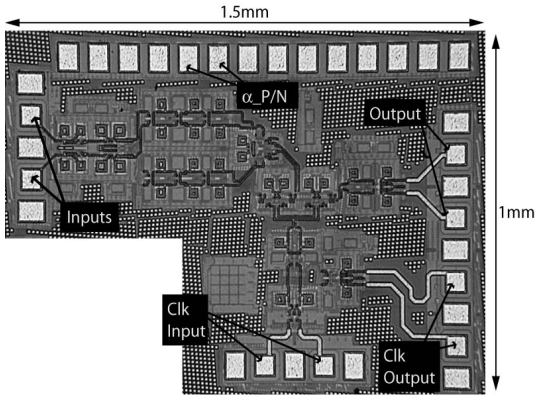


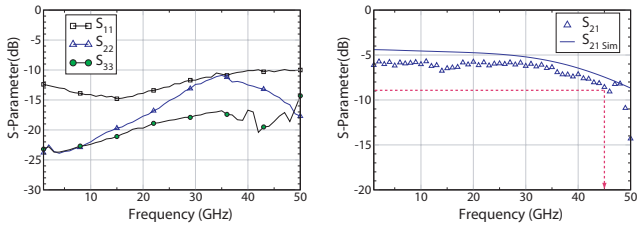
Fig. 4. DFE fabricated in Jazz Semiconductors' SBC18hx 0.18μm SiGe BiCMOS technology with a 160-GHz f_t operating from a 3.3V supply with 230mA current.

tial control voltage to the MOSFET differential pair to vary the output DC voltage. The MOSFETs are buffered from the high speed path with bipolar transistors chosen because of their lower collector bulk capacitance. They also provide larger tuning linearity due to the higher output resistance and a constant V_{DS} on $Q_{5/6}$ for even large changes in the DC voltages at the output.

III. Fabrication and Results

The full chip (Fig. 4) is fabricated in Jazz Semiconductors' SBC18HX 0.18μm SiGe BiCMOS technology with a 160-GHz f_t. The layout corresponds to the chip architecture in Fig. 1. It occupies an area of 1.5mmx1mm and operates from a 3.3 V supply with 230 mA current. A breakout of the broadband front end, including the TIA and slicing threshold adjustment circuit indicated in Fig. 1, was also fabricated to characterize the linear portion of the circuit.

The single-ended S-parameter measurements, with the other differential input/output terminated with 50 Ω, were performed using a Wiltron 360B VNA. Measurements show the single-ended return loss (Fig. 5(a)) of all the high speed ports for the DFE to be better than -10 dB up to 40 GHz. Single-ended S-parameter measurements of the front end breakout, through the TIA and one of the threshold adjustment circuits with the other outputs terminated, demonstrate the 3dB bandwidth of



(a) (b)

Fig. 5. S-parameter measurements of (a) DFE return loss for the input (S_{11}), output (S_{22}) and clock input (S_{33}), and (b) measurements and simulation of S_{21} for front end breakout

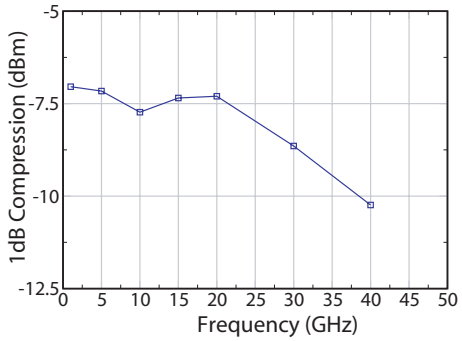


Fig. 6. Measured P_{1dB} over frequency

45-GHz up to the slicers. Since the measurements are single-ended, the actual gain is 6 dB higher than that presented in Fig. 5(b).

The 1dB compression point (P_{1dB}) was measured for the TIA and threshold circuit breakout to determine the maximum linear input power swing that can be applied. The measurement results up to 40 GHz can be seen in Fig. 6. A P_{1dB} of approximately -7 dBm is measured which corresponds to a single-ended input of approximately 135 mV_{pp}. The measured DC offset voltage at the outputs of the threshold circuit versus the DC control signal, α, is produced in Fig. 7. It demonstrates ISI cancellation for all linear input amplitudes.

In the absence of a 40-Gbps bit error tester (BERT), two large signal equalization tests were completed to verify functionality. The first measurement involved a bit error test

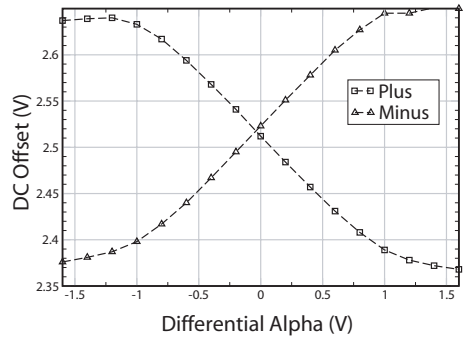
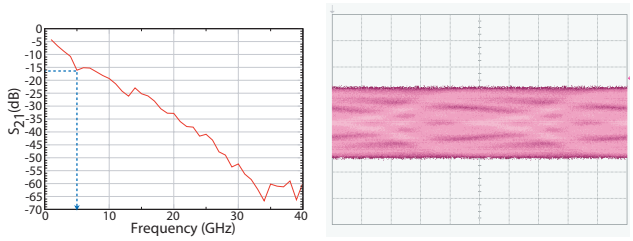


Fig. 7. Measured output offset voltage versus the differential DC control voltage for ISI cancellation



(a) (b)

Fig. 8. 20-ft SMA cable (a) frequency response and (b) 10-Gbps $2^{31}-1$ PRBS input eye diagram

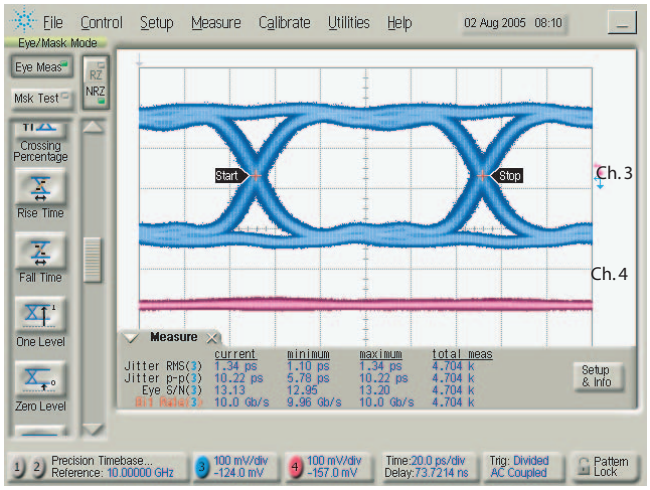


Fig. 9. Measured single-ended output eye diagram at 10-Gbps through a 20-ft SMA cable

performed through a 20-ft SMA cable at 10 Gbps. The second measurement involved equalization through a 9-ft SMA cable at 40 Gbps with pattern waveform capture and hand error checking using the Agilent 8600C oscilloscope.

The 10-Gbps bit error test (BERT) runs off a single clock source, where one OTB3P1A Centellax 10-Gbps board is configured as a $2^{31}-1$ PRBS generator and the other is connected as a PRBS error checker. The PRBS data is fed through a dispersive channel into the equalizer. One of the equalizer outputs is displayed on the Agilent oscilloscope and the other is fed into the error checker. The error trigger on the checker is also fed into the other remote head of the Agilent scope. A transition on the error trigger (ch. 4) indicates a bit error.

The frequency response of the channel used for the BERT test is shown in Fig 8(a), along with a single-ended input eye diagram at 10 Gbps in Fig. 8(b). The resulting single-ended output eye diagram is presented in Fig. 9. It has an SNR of 13.12 and swing of 300 mV_{pp}. The channel 4 trigger shows error free operation for 4000+ measurements.

The test setup for 40-Gbps measurements is described in Fig. 10. Two Centellax OTB3P1A boards produce 10-Gbps PRBS data which are fed into a multiplexer to generate a broadband 40-Gbps data stream which is 4 times the bit length of the PRBS pattern of the boards (i.e. a 2^7-1 PRBS

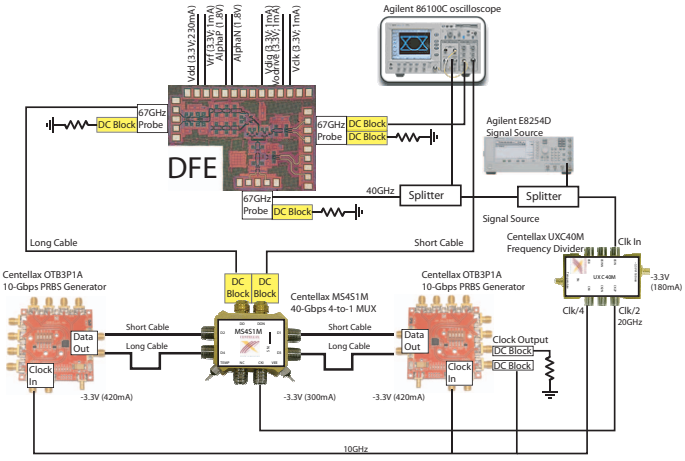
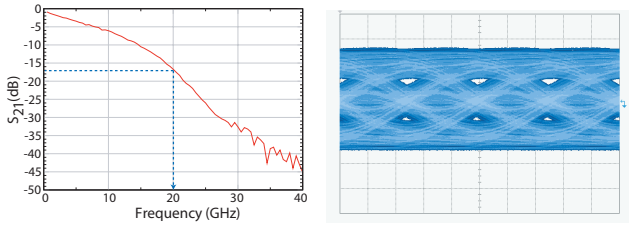


Fig. 10. Setup for large-signal 40-Gbps measurements



(a) (b)

Fig. 11. 9-ft SMA cable (a) frequency response and (b) 40-Gbps input eye diagram

configuration results in a 508-bit repeating sequence). The scope displays the equalized single-ended output of the DFE as well as the ideal data pattern from the mux. Error checking was performed on the bit sequence using the pattern lock feature in the Agilent scope.

The frequency response of the channel used for the 40-Gbps measurement is shown in Fig 11(a), along with a single-ended input eye diagram at 40 Gbps in Fig. 11(b). The single-ended output in Fig. 12 has an RMS jitter is 750fs, peak-to-peak jitter of 5.11ps, SNR of 9.1, and a swing of 340 mV_{pp}. The corresponding bathtub curve in Fig. 14 indicates a timing margin of 0.75UI, with a total jitter of 6.13ps. A segment of the output bit sequence when the boards are configured for a 2^7-1 PRBS pattern (output of 508-bit length) is presented in Fig. 15, from top to bottom for ideal, unequalized, and equalized outputs. Errors in the unequalized output are indicated with arrows above the sequence.

IV. Conclusion

The design and experimental characterization of 1-tap DFE operating at 40-Gbps was described. The circuit architecture is based on a look-ahead topology without retiming at the inputs into the selector. A TIA input stage is used because it provides low noise and large bandwidth. The threshold adjustment circuit allows for a wide linear tuning range while providing high speed operation. The performance was verified with a BERT at 10 Gbps through a 20-ft SMA cable and at

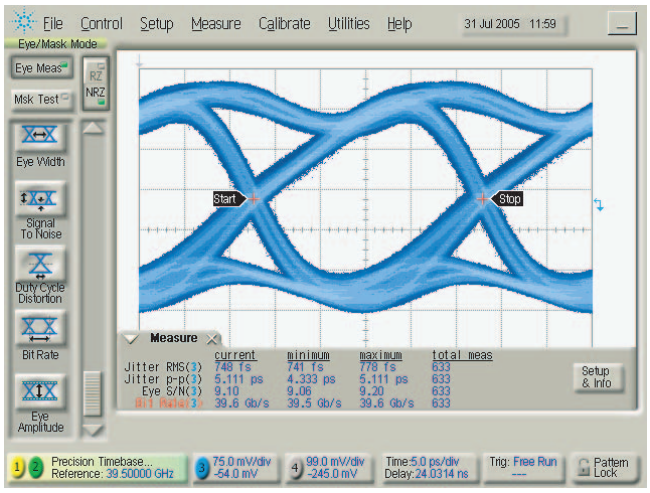


Fig. 12. Single-ended equalized output eye through 9-ft SMA cable at 39.5Gbps, board pattern of $2^7 - 1$

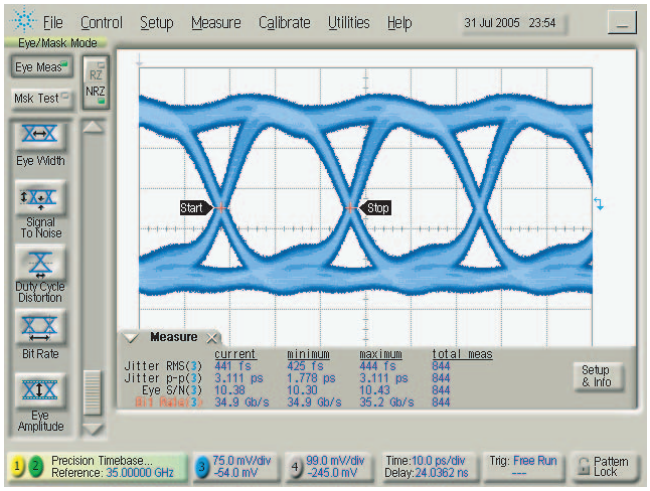


Fig. 13. Single-ended equalized output eye through 9-ft SMA cable at 35Gbps, board pattern of $2^{31} - 1$

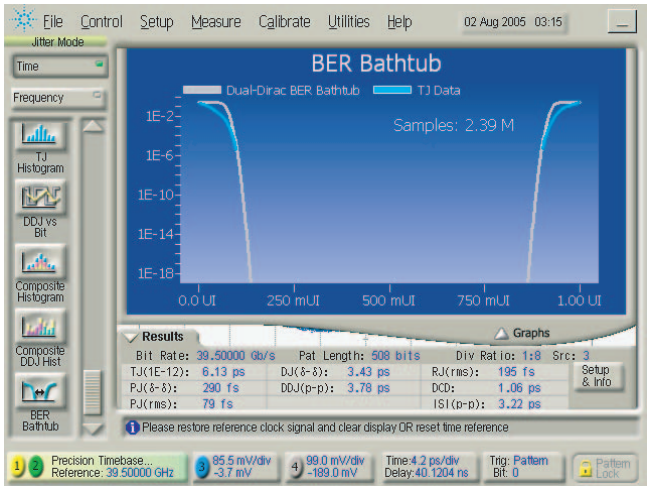


Fig. 14. Single-ended bathtub curve for single-ended output eye through 9-ft SMA cable at 39.5Gbps

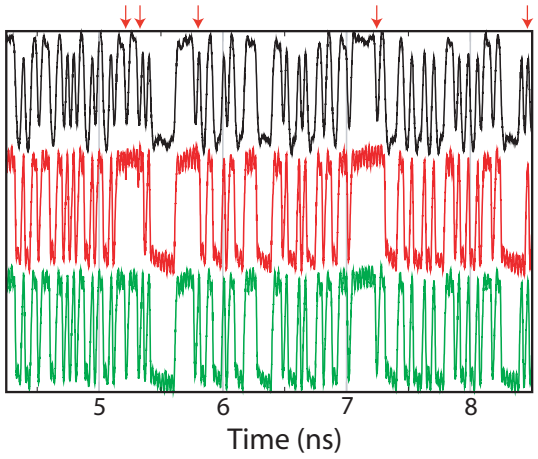


Fig. 15. Segment of 508-bit sequence ($2^7 - 1$ PRBS on each board) for an ideal (top), unequalized (middle) and equalized (bottom) output. Errors indicated by arrows above bit sequence.

40 Gbps over a 9-ft SMA with visual error checking. The DFE significantly reduces the ISI within the channel. To the authors' knowledge, this is the first DFE in silicon at 40-Gbps. In combination with a feed forward equalizer, this paper demonstrates that an equalizer suitable for electrical PMD compensation is realizable in silicon.

V. Acknowledgments

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