

A 60 mW per Lane, $4 \times 23\text{-Gb/s } 2^7 - 1$ PRBS Generator

E. Laskin and S. P. Voinigescu

Edward S. Rogers Sr. Department of Electrical and Computer Engineering
University of Toronto, Toronto, Ontario, Canada
Email: laskin@eecg.utoronto.ca

Abstract – An ultra-low-power, 4-channel $2^7 - 1$ PRBS generator with 60 mW per channel was designed, fabricated and measured to work up to 23 Gb/s. The circuit is based on a 2.5-mW BiCMOS CML latch topology, which, to the best of our knowledge, represents the lowest power for a latch operating above 10-Gb/s. The chip also includes an integrated PRBS checker and error counter.

Keywords – PRBS generator, BiCMOS cascode, BiCMOS CML

I. INTRODUCTION

Pseudo Random Bit Sequence (PRBS) generators and checkers are widely used for testing the correct functionality of high speed digital circuits when no other sources are available. They can also be integrated on the same chip as the device under test for built-in self test (BIST) purposes. For these applications, it is important that the generator be able to produce as long a sequence as possible, but also be low power. Previously, our group has designed a record 80-Gb/s PRBS generator with a $2^{31} - 1$ sequence length [1]. However, due to the long sequence length, it was too large and power hungry to be used as an IP block. Currently, we are exploring ways to reduce the power consumption of PRBS generators, while maintaining the speed. This paper reports an ultra-low-power $2^7 - 1$ PRBS generator with 4, appropriately delayed, parallel output streams at 23-Gb/s each, which can be further multiplexed to an aggregate PRBS output at 92 Gb/s with minimal circuitry. The 4-channel PRBS generator consumes 235 mW from 2.5 V, which results in only 60 mW per output lane. The entire chip, which also integrates an error checker and a 5-bit error counter, consumes 940 mW.

The low power performance of the circuit is facilitated at the transistor level by the design of a low-power SiGe BiCMOS CML latch. At the system level, power is optimized by using a parallel, as opposed to series, PRBS generator topology [2], which avoids additional phase shifting circuitry and is suitable for generating signals that can be multiplexed directly.

II. CHIP ARCHITECTURE

A top-level block diagram of the chip is shown in Fig. 1. It contains a $2^7 - 1$ PRBS generator circuit that produces 8 parallel signals at 12 Gb/s; a MUX that combines the 8 signals into 4 parallel output lanes at 24 Gb/s, one of which is provided off-chip for testing; a PRBS checker; an error counter circuit with 5 output bits; a switch to manually introduce errors into the sequence; and, finally, a tree of

buffers that distributes the 12-GHz clock signal to all components. Fig. 1 also illustrates how this chip can be part of a 2.5-V 80-Gb/s transmitter system with the addition of only a 4-to-1 multiplexer and an 80-Gb/s output buffer, already in development [3].

PRBS Generator Design

A PRB-sequence with a length of $2^7 - 1$ is generated according to $x^7 \oplus x^6 = 1$ or $x^1 \oplus x^2 = x^8$, where x^D represents a delay of D clock cycles. This can easily be implemented with a linear feedback shift register in which the outputs of the sixth and seventh flip-flops are added together and provided as input to the first flip-flop of the register. This configuration of the generator outputs the PRBS bits in series, i.e. bits 1-7 are available in the first clock cycle, bits 2-8 in the second clock cycle, bits 3-9 in the third, etc. In most cases it is advantageous to generate the PRBS at a lower speed and then to multiplex it to the required data rate. However, to preserve the randomness of the sequence, each pair of bits that are multiplexed must be 180° (or equivalently $1/2$ sequence length) apart. This implies that, in order to multiplex 8 streams into 4, 8 equally spaced phases of the sequence must be available at each clock cycle. For example, bits 0, 16, 32, 48, 64, 80, 96, 112 are needed in one clock cycle, bits 1, 17, 33, 49, 65, 81, 97, 113 in the next clock cycle, and so on. A sequence with any required delay can be generated by adding a number of other delayed sequences by the algorithm described in [4]. Since only 8 different delays are available in a $2^7 - 1$ generator by tapping from the flip-flops, phase shifting circuitry (which includes XOR gates and possibly retiming) would be needed to generate the 8 appropriate phases for multiplexing. The phase shifting circuitry

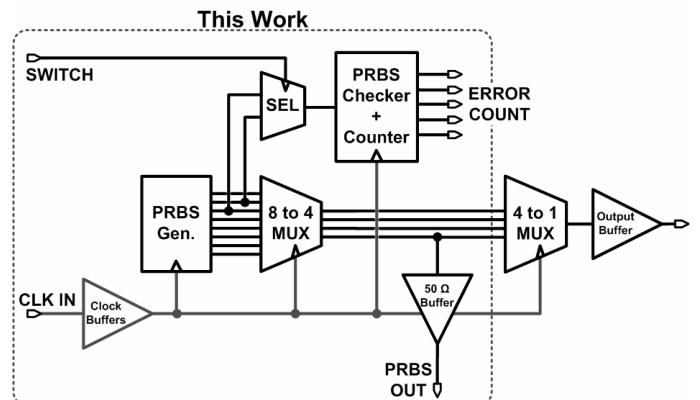


Figure 1: Top-Level Chip Schematic

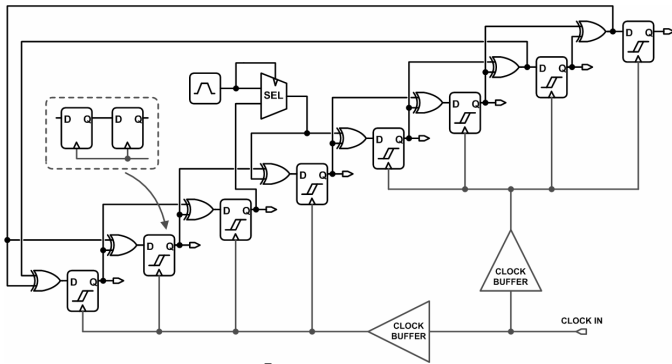


Figure 2: Parallel $2^7 - 1$ PRBS Generator Schematic

contributes to the power consumption by adding logic blocks and by increasing the fan-out in the shift register flip-flops.

An alternate, “parallel” architecture exists for PRBS generators [2]. It, too, operates according to the $x^1 \oplus x^2 = x^8 = x^0$ equation, but each of the delayed signals x^1 and x^2 is obtained from the same equation: $x^1 = x^2 + x^3$. The parallel PRBS generator schematic, which was implemented in the chip, is shown in Fig. 2. For a $2^7 - 1$ generator, the parallel architecture requires 8 flip-flops and 8 XOR gates, compared to 7 flip-flops and 1 XOR gate in the series architecture. But the main advantage of the parallel PRBS generator is that it directly generates all 8 appropriately delayed sequences for multiplexing without requiring any additional phase shifting logic. To generate 8 phase-shifted sequences from a series PRBS generator, at least 13 2-input XOR gates and possibly some retiming is required. Therefore, overall, power is saved compared to the series architecture. Fig. 2 also shows the generator clock tree and the reset signal which initiates the sequence. The 8 PRB-sequences are generated at 12 Gb/s and then multiplexed to 24 Gb/s by the 8-to-4 multiplexer shown in Fig. 3. The PRBS generator and the 8-to-4 multiplexer occupy an area of only $393 \mu\text{m} \times 178 \mu\text{m}$.

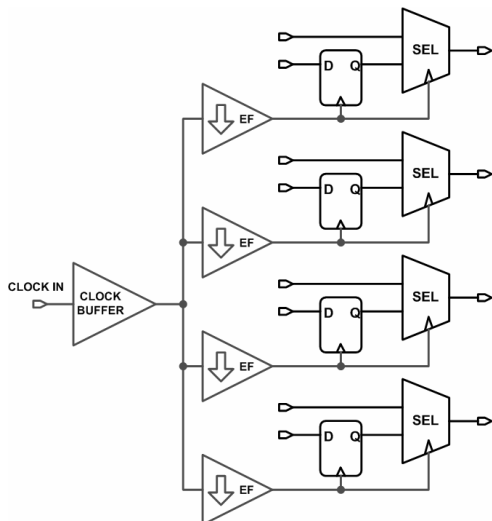


Figure 3: 8-to-4 MUX Schematic

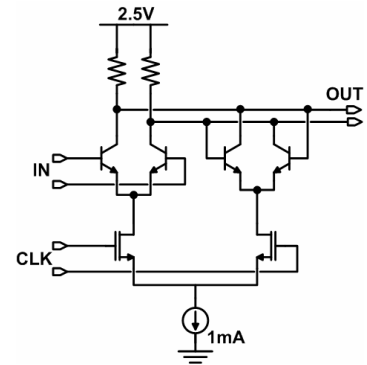


Figure 4: CML Latch Schematic

III. LOGIC TOPOLOGY

At the transistor level, the key feature of all the PRBS generator and checker blocks is the low power BiCMOS CML topology shown in Fig. 4. It differs from the BiCMOS ECL logic family presented in [1, 5] in two ways. Firstly, emitter follower stages are eliminated in the latching pair. Secondly, the tail current in all the CML BiCMOS cascode stages is reduced to 1 mA, which corresponds to 1.5 times the peak f_T current of a minimum size SiGe HBT. Biasing of the SiGe HBTs at 1.5 times the peak f_T current density is optimal for highest switching speed. For maximum speed, all n-MOSFETs are minimum length with $W = I_T / (0.3 \text{ mA} / \mu\text{m})$ [3]. The logic cells are designed such that one latch consumes only 2.5 mW and a fan-out-of-two flip-flop consumes 12.5 mW from a 2.5-V supply. Additionally, clock path emitter followers are shared between the two latches of the flip-flop (Fig. 5) and between the latch and selector of each 2-to-1 multiplexer (Fig. 3). The latch and flip-flop work at 12 Gb/s, with excellent agreement between measurement and simulation with parasitic resistance and capacitance extraction. To minimize area, no inductors are used anywhere in the chip.

To the best of our knowledge, this is the lowest power latch operating above 10 Gb/s in any technology. Other recently reported sub-3.3V bipolar logic families [6, 7] consume significantly more power because they require doubling the tail current for a given logic function. Note that, since MOSFETs are used on the clock path, the tail current source can be eliminated to further reduce supply voltage and power as in [8]. While 130-nm or 90-nm MOS CML latches operate from 1.5-V or lower supplies, they require more than 2 times higher tail currents and inductive peaking to operate above 10 Gb/s, thus offsetting the advantage provided by the lower supply voltage [8].

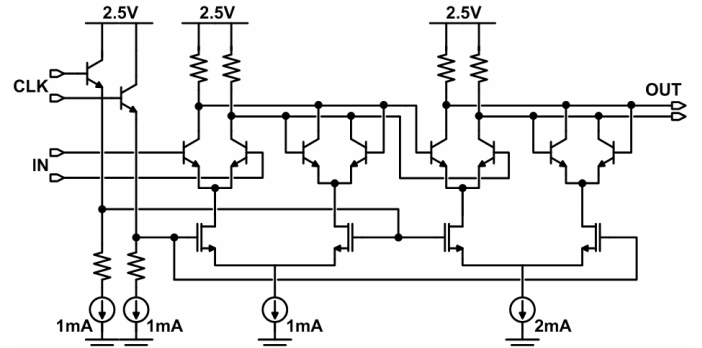


Figure 5: D flip-flop Schematic

Future Logic Scaling

We have investigated several techniques for further reducing the power consumption of logic gates while maintaining the same data rate in the same technology. As shown in Fig. 6a, current source transistors can be eliminated to make the latch operate from 1.8 V with a total current of 1 mA, consuming only 1.8 mW. In this case, the total current is controlled by the size of the bottom NMOS devices which are biased at 1/2 peak f_T current density of 0.15 mA/ μm . Simulations with parasitic resistance and capacitance extracted from layout, indicate that no loss in speed is incurred in this latch compared to the one shown in Fig. 4.

We have also explored how CML logic speed improves by scaling to the next technology node while consuming the same power. Simulation of the latch schematic shown in Fig. 6b with 90-nm MOSFETs and 230-GHz f_T HBTs [9], and with the same layout parasitics as before (pessimistic), indicates that it can be operated at 30 Gb/s with 1 mA total current from 1.8-V supply. This is a factor of 2 improvement in speed with respect to the same latch implementation in the present 0.13- μm SiGe BiCMOS technology.

IV. MEASUREMENT RESULTS

The chip was fabricated in a 0.13- μm SiGe BiCMOS technology with transistor f_T of 160 GHz. It occupies an area of 1 mm \times 0.8 mm, limited by the pad frame.

Testing of the PRBS generator was conducted on wafer at different input clock frequencies. One of the differential outputs of the generator was connected to an Agilent E4448A PSA series spectrum analyzer and the other output was connected to an Agilent 86100C DCAJ, which is capable of identifying, locking, and characterizing the jitter of digital sequences as long as $2^{15} - 1$ at data rates beyond 40 Gb/s. The $2^7 - 1$ pseudo-random sequence was verified by looking at the sequence bits in the time domain and by checking the spacing of tones in the output spectrum. The spacing between tones is equal to the bit-rate divided by the sequence length. The spectrum also has nulls at multiples of the input clock frequency, indicating NRZ logic. Figs. 8-13 demonstrate the correct operation of the PRBS generator at 12 Gb/s, where the RMS jitter is 1.4 ps and the spectral tones are spaced 94.5 MHz apart. Figs. 14-19 show correct operation at 23 Gb/s with RMS jitter of 1.3 ps. The 20% to 80% rise/fall times are 18 ps and the spectral tones are spaced 180.9 MHz apart. Figs. 20-22 show the output eye and the spectrum at 24 Gb/s which has correct spacing of 189.2 MHz. However, the scope could not lock to the sequence. Clearly, all logic blocks work up to

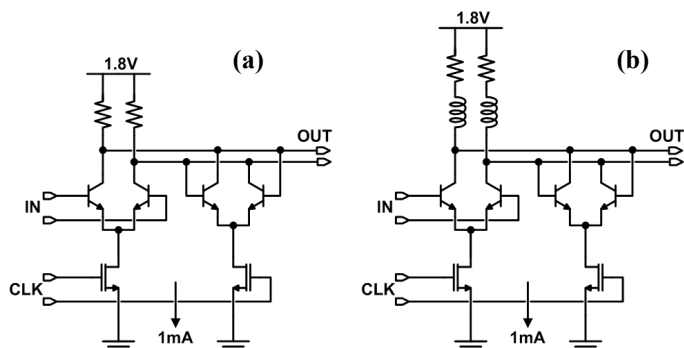


Figure 6: Low Voltage Latch Schematics

24 Gb/s but their delay increases relative to a clock cycle time limiting the error-free operation speed to 23 Gb/s. Operation of the PRBS generator was verified to be correct down to 100 Mb/s.

V. CONCLUSION

A $2^7 - 1$ PRBS generator chip, with integrated error checker and counter was designed, fabricated and characterized. The design was optimized for low power consumption at the architecture and circuit level. A 2.5-V, 1-mA latch is used on the 12-Gb/s path. To the best of our knowledge this is the lowest power latch operating above 10 Gb/s.

ACKNOWLEDGMENT

The authors thank Bernard Sautreuil and Rudy Beerkens for their support and STMicroelectronics for fabrication. We also thank Micronet and CMC for CAD tools and support, and NSERC for financial support.

REFERENCES

- [1] T. Dickson, *et al.*, "A 72Gb/s $2^{31}-1$ PRBS Generator in SiGe BiCMOS Technology," in *2005 IEEE ISSCC Digest of Technical Papers*, pp. 342-343.
- [2] S. Kim, *et al.*, "45-Gb/s SiGe BiCMOS PRBS Generator and PRBS Checker," in *CICC 2003*, pp. 313-316.
- [3] S. P. Voinescu, *et al.*, "Algorithmic Design Methodologies and Design Porting of Wireline Transceiver IC Building Blocks between Technology Nodes," in *CICC 2005*, accepted.
- [4] A. N. Van Luyn, "Shift-Register Connections for Delayed Versions of m-Sequences," *Electronics Letters*, vol.14, no. 22, pp. 713-715, Oct. 1978.
- [5] T. Dickson, *et al.*, "A 2.5-V 45-Gb/s decision circuit using SiGe BiCMOS logic," in *IEEE J. Solid-State Circuits*, vol. 40, no. 4, pp. 994-1003, Apr. 2005.
- [6] Y. Amamiya, *et al.*, "1.5-V Low Supply Voltage 43-Gb/s Delayed Flip-Flop Circuit," in *2003 IEEE GaAs Digest*, pp. 169-172.
- [7] D. Kucharski, K. Kornegay, "A 40Gb/s 2.5V 2^7-1 PRBS Generator in SiGe Using a Low-Voltage Logic Family," in *2005 IEEE ISSCC Digest of Technical Papers*, pp. 340-341.
- [8] K. Kanda, *et al.*, "40Gb/s 4:1 MUX/1:4 DEMUX in 90nm Standard CMOS," in *2005 IEEE ISSCC Digest of Technical Papers*, pp. 152-153.
- [9] P. Chevalier, *et al.*, "230 GHz self-aligned SiGeC HBT for 90 nm BiCMOS technology," in *Proceedings of IEEE BCTM 2004*, pp 225-228.

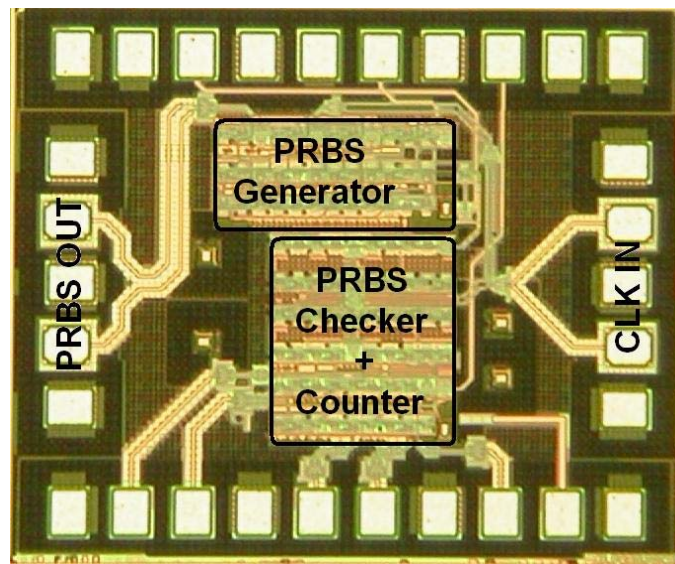


Figure 7: Die Photo

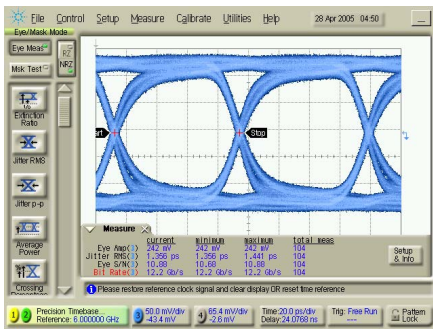


Figure 8: 12 Gb/s Eye

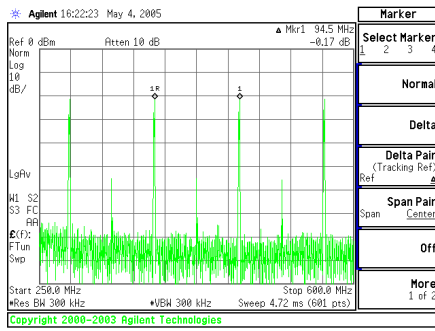


Figure 13: 12 Gb/s Spectrum

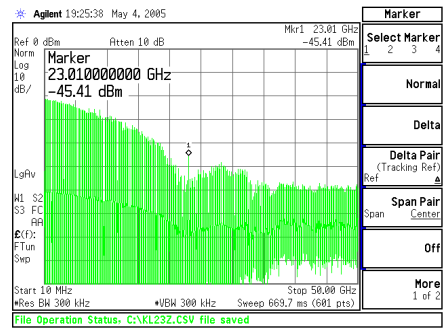


Figure 18: 23 Gb/s Spectrum

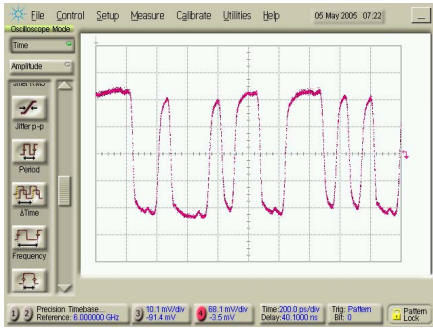


Figure 9: 12 Gb/s Waveform

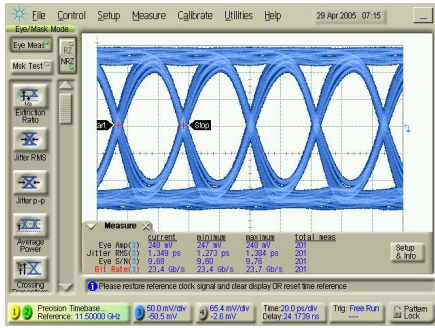


Figure 14: 23 Gb/s Eye

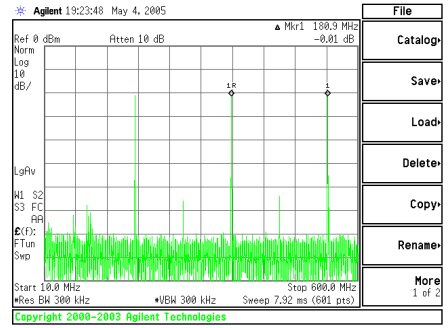


Figure 19: 23 Gb/s Spectrum

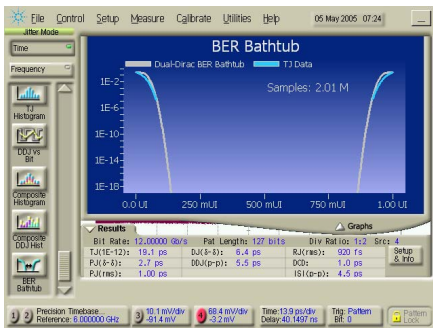


Figure 10: 12 Gb/s BER Bathtub

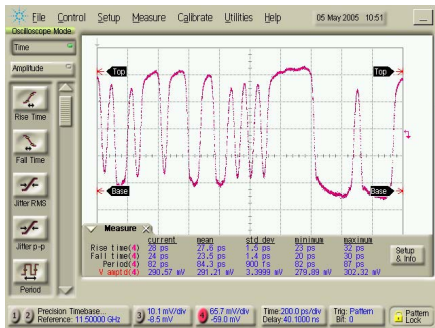


Figure 15: 23 Gb/s Waveform

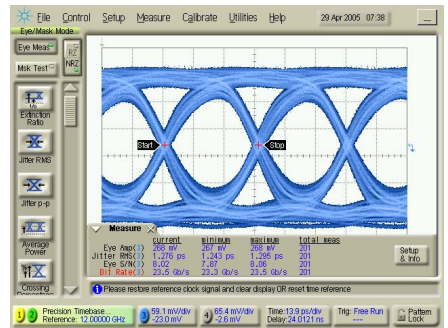


Figure 20: 24 Gb/s Eye

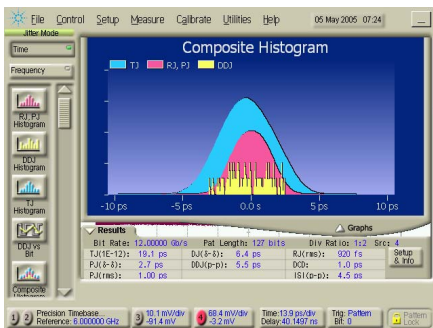


Figure 11: 12 Gb/s Jitter

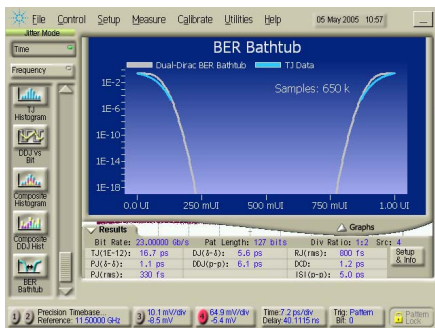


Figure 16: 23 Gb/s BER Bathtub

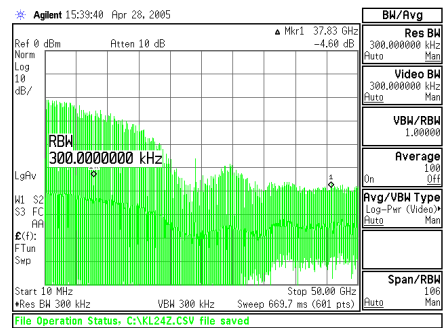


Figure 21: 24 Gb/s Spectrum

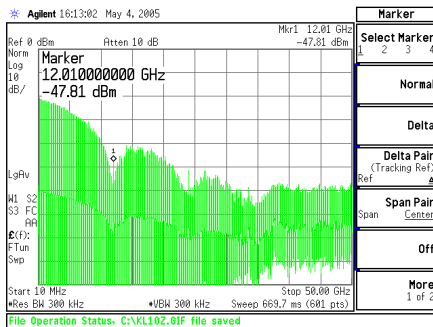


Figure 12: 12 Gb/s Spectrum

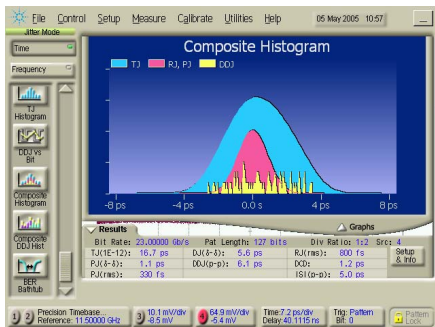


Figure 17: 23 Gb/s Jitter

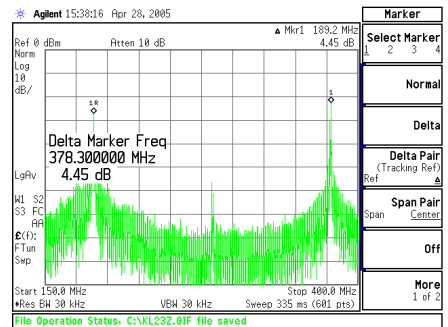


Figure 22: 24 Gb/s Spectrum