

# Design Methodology and Applications of SiGe BiCMOS Cascode Opamps with up to 37-GHz Unity Gain Bandwidth

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**Abstract**—A new technique to design highly stable operational amplifiers with maximum unity gain bandwidth,  $UGB$ , is developed. It relies on biasing MOSFETs at the peak  $f_{MAX}$  current density. Several opamps, based on MOS-HBT SiGe BiCMOS cascodes, were designed and fabricated with  $UGB$  as high as 37 GHz. This record bandwidth is achieved with active p-MOSFET loads. A 1.3-GHz bandpass filter was implemented using two fully differential opamps with common-mode-feedback.

**Keywords** - operational amplifier, unity-gain bandwidth, cascode, SiGe BiCMOS, peak  $f_{MAX}$  current density, bandpass filter, common-mode feedback

## I. INTRODUCTION

Traditional MOSFET opamp design relies on biasing the transistors at a relatively low effective gate voltage of 0.1 to 0.2V. Apart from resulting in circuits with a relatively modest bandwidth, in sub-180nm technologies, this approach makes the opamp performance sensitive to threshold voltage and bias current variation. We report on a family of operational amplifiers (opamps) with record-breaking unity-gain bandwidth implemented in a 130-nm SiGe BiCMOS technology [1]. The fully differential opamps, featuring common-mode feedback, are based on a MOSFET-SiGe HBT cascode stage that proved to be optimal in high-speed CML/ECL [2] and millimeter-wave [3] applications. We now demonstrate that, when appropriately sized and biased, this topology (Fig. 1) results in highly linear, wideband amplifiers which require virtually no compensation to ensure good stability even at frequencies exceeding 20 GHz.

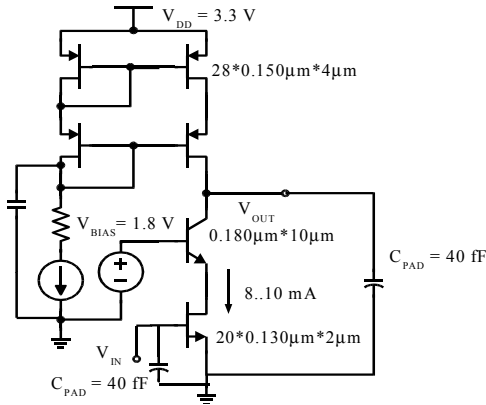


Figure 1. Opamp half-circuit schematic.

## II. CIRCUIT DESIGN

It is well-known that the cascode stage with a MOSFET input and npn BJT output is ideal for realizing opamps with good stability [4]. Its main advantage over MOS-MOS or HBT-MOS cascodes stems from the complete elimination of the Miller effect, leading to an always stable, single-pole transfer function. The pole associated with the drain of the n-MOSFET and the emitter of the HBT is pushed to very high frequencies, at approximately  $f_{T,HBT}$ . The latter easily exceeds 150 GHz in a state-of-the-art SiGe BiCMOS process and can therefore be ignored. For the circuit illustrated in Fig.1, the low frequency gain, dominant pole, and  $UGB$  can be described as

$$A_V = -g_{m,nMOS} R_{out} \quad UGB = \frac{g_{m,nMOS}}{2\pi C_{out}} \quad (1)$$

$$f_{p1} = \frac{1}{2\pi R_{out} C_{out}} \quad (2)$$

where

$$R_{out} \approx g_{m,pMOS} r_{o,pMOS}^2 \quad (3)$$

$$C_{out} = C_{bc} + C_{cs} + C_{db,pMOS} + C_{gd,pMOS} + C_L \quad (4)$$

In deriving (3) we have ignored the output resistance of the nMOS-HBT cascode. Due to the much larger  $g_m$  and  $r_o$  of the HBT, it exceeds that of the pMOS cascode by more than an order of magnitude.

The second pole of the circuit is located at the gate of the n-MOSFET. It, too, can be pushed far beyond  $f_{p1}$  by employing a multi-finger transistor geometry (to reduce the gate resistance  $R_g$ ) and a driver stage with low output resistance (such as an emitter or source follower) to act as a low- $R_s$  signal source.

$$f_{p2} = \frac{1}{2\pi(R_g + R_s)(C_{gs} + C_{gd})} \quad (5)$$

For the phase margin to be larger than  $45^\circ$ ,  $f_{p2}$  must exceed  $UGB$ . It is important to note that, in the limit of negligible load capacitance (i.e.  $C_L=0$ ),  $f_{p2}$  becomes a technology constant. Furthermore,  $C_{out}/W$  is, to first order, invariant across technology nodes and foundries since it is dominated by the

$C_{db}$  and  $C_{gd}$  of the p-MOSFET, approximately 1 fF/ $\mu\text{m}$  and 0.3 fF/ $\mu\text{m}$ , respectively.

Beyond the choice of topology, the key to achieving record  $UGB$  is to bias the MOSFET at a large effective gate voltage where the  $I$ - $V$  characteristics become linear rather than obey the classical square law [6]. More precisely, the MOSFET is biased at 0.2mA/ $\mu\text{m}$ , corresponding to the peak  $f_{MAX}$  current density. Even though this regime is unconventional for opamp design because it results in somewhat reduced low-frequency gain, it leads to three favorable outcomes: (i) maximized  $UGB$ , (ii) maximized linearity, and (iii)  $UGB$  becomes insensitive to threshold voltage and bias current variation. This choice of bias point relies on the experimental observation that, in deep submicron MOSFETs, the optimum noise figure current density (0.15mA/ $\mu\text{m}$ ), the peak  $f_{MAX}$  current density (0.2mA/ $\mu\text{m}$ ) [5], and the peak  $f_T$  current density (0.3mA/ $\mu\text{m}$ ) [5] remain largely invariant between foundries and technology nodes [6]. For the first time, we apply this observation to the algorithmic design of operational amplifiers using SiGe BiCMOS cascodes. To maximize the  $UGB$  of the opamp, all p- and n-MOSFETs and SiGe HBTs in the differential cascode stage are biased at their peak  $f_{MAX}$  current density, while the DC gain remains above 34 dB.

The schematic of a fully differential opamp using the nMOS-SiGeHBT cascode with active p-MOSFET cascode load is shown in Fig. 2. Emitter followers  $Q_5$  and  $Q_6$  provide low output impedance and appropriate DC voltage levels to drive an identical stage. The common-mode feedback path, consisting of the degeneration resistors of  $Q_5$  and  $Q_6$  and of  $Q_{11}$  and  $Q_{12}$ , operates as follows. If the common-mode DC voltage at  $V_{ON}$  and  $V_{OP}$  rises, the current through  $Q_{11}$  increases, it is next mirrored by  $Q_{12}$  leading to a reduction in the common-mode voltage at the collectors of  $Q_3$  and  $Q_4$  and, finally, at  $V_{ON}$  and  $V_{OP}$ .

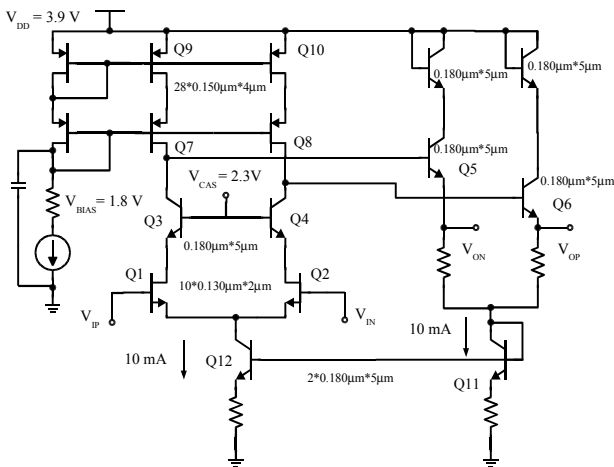


Figure 2. Differential opamp schematic.

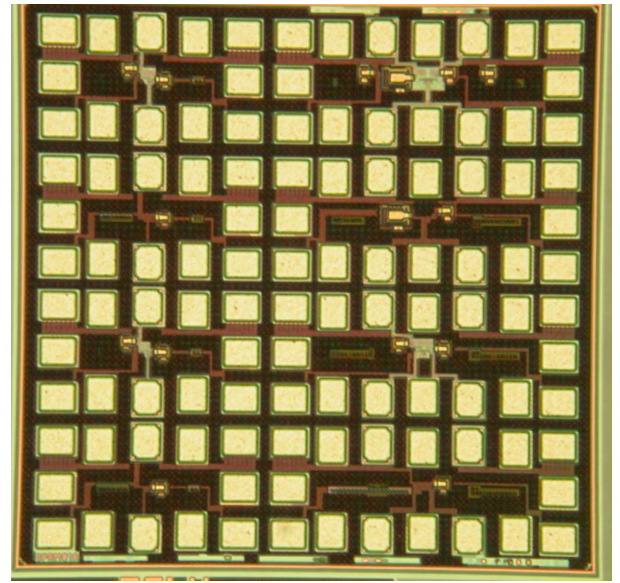


Figure 3. Die photograph of the opamp test structures.

### III. EXPERIMENTAL RESULTS

A number of test structures were designed and fabricated as shown in the chip microphotograph reproduced in Fig. 3. This includes (i) cascode half-circuits with 5-mA and 10-mA bias current, with and without 1-pF load capacitance, (ii) cascode differential amplifiers with current-mirror output, and (iii) fully differential amplifiers with common-mode feedback. S parameter measurements were carried out on wafer up to 65 GHz using a Wiltron 360B Network Analyzer and GGB probes.

The measured DC and S parameter data presented in Figs. 4 and 5 for two opamp half-circuits confirm that the pad capacitance of 40 fF is sufficient to provide more than 30 degrees phase margin for a BiCMOS cascode stage with 34 dB gain and  $UGB=37$  GHz. The bandwidth of the 10-mA circuit is almost twice as large as that of the 5-mA circuit since the load capacitance is comparable in both cases.

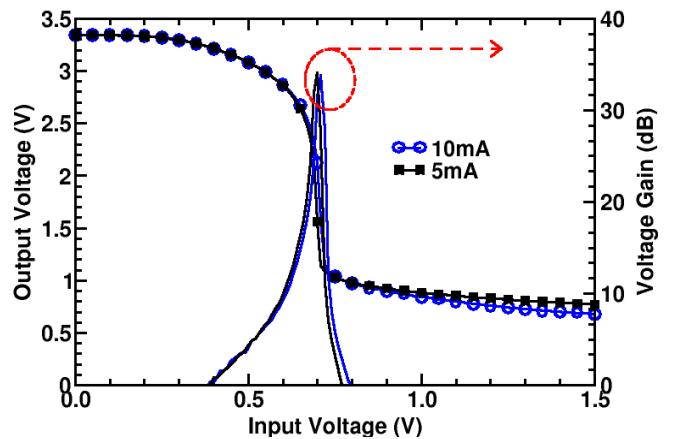


Figure 4. DC gain of 5-mA and 10-mA opamp half-circuit test structures.

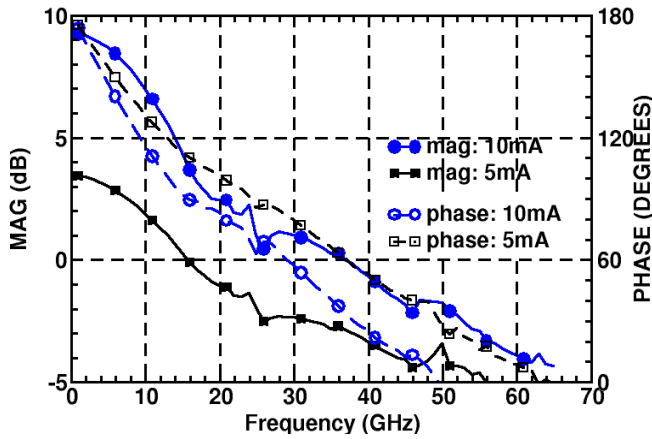


Figure 5. Measured gain and phase for opamp half-circuits scaled for 10-mA and 5-mA bias current, respectively, and directly driving the 40-fF pad capacitance and 50- $\Omega$  load.

Fig. 6 compiles the measured  $UGB$  data as a function of MOSFET current density for two half circuits. They demonstrate that MOSFETs should be biased at peak  $f_{MAX}$  for large opamp bandwidth, and closer to peak  $f_T$  current densities as the load capacitance increases proportionally with respect to transconductance. The  $UGB$  of both circuits varies by less than 15% when the bias current density changes from 0.15mA/ $\mu\text{m}$  to 0.35mA/ $\mu\text{m}$ , making the design extremely robust to process variability affecting  $V_T$  and the bias current.

The DC gain of the fully differential opamp from Fig.2 is reproduced in Fig.7 for different bias current densities. As expected, the DC gain decreases with increasing current density. At the same time, the input linear voltage range is improved when the current density approaches 0.3 mA/ $\mu\text{m}$ , as predicted in [6] based on the measured  $f_{MAX}$ - $I_D$  characteristics of n-MOSFETs. The input offset voltage is typically lower than 2.5 mV. The magnitude and phase of the single-ended  $S_{21}$  are plotted in Fig.8. The single-ended  $UGB$  is 11 GHz while the differential one (obtained by adding 6 dB to the measured gain) is 18 GHz, in excellent agreement with that of the 5-mA half-circuit.

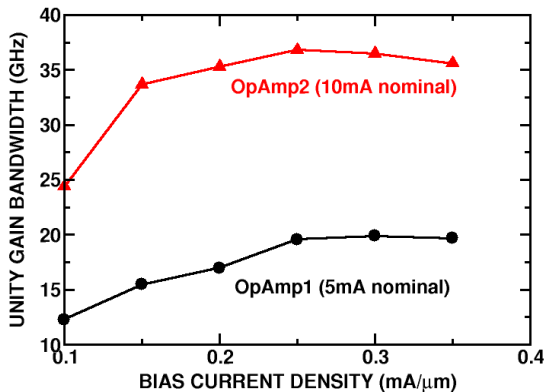


Figure 6. Measured  $UGB$  as a function of current density.

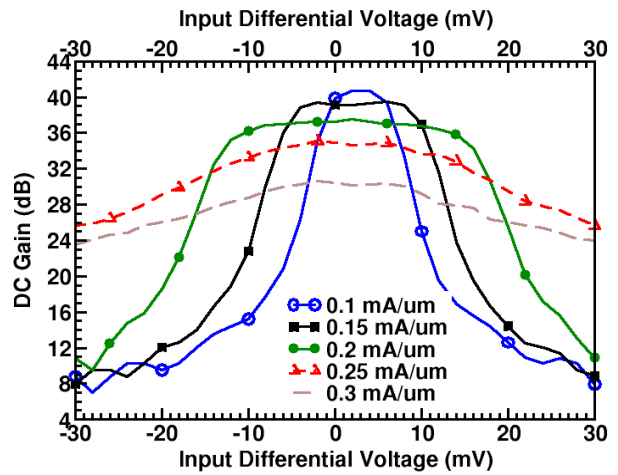


Figure 7. Measured DC gain as a function of MOSFET current density and input differential voltage.

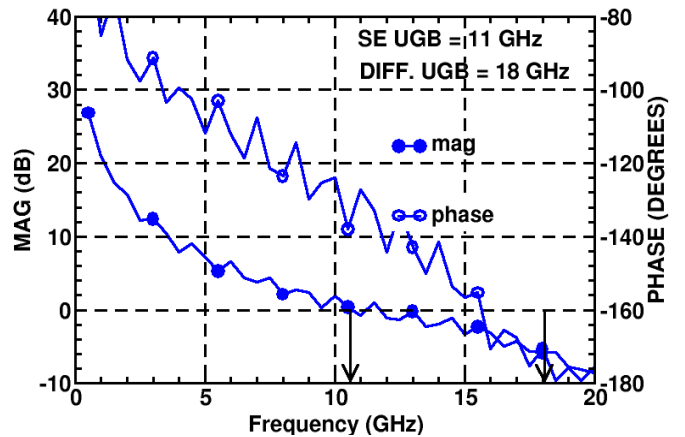


Figure 8. Measured single-ended gain  $S_{21}$  and phase of the differential opamp with 10-mA tail current (5 mA per side) whose schematic is shown in Fig. 4

A 2-stage opamp bandpass filter with a biquad architecture (Fig. 9) was scaled from a textbook design [7] to 1.2 GHz to serve as a demonstration vehicle for the applicability of these opamps in the GHz-range. The die photograph is reproduced in Fig.10. At 0.2mmx0.3mm, including pads, it occupies significantly less area than L-C based filters operating at this frequency. The measured  $S_{21}$  (Fig. 11) peaks at over 20 dB while  $P_{1dB}$  and  $OP_{1dB}$  are -25 dBm, and -2.5 dBm, respectively, as in Fig. 12.

#### IV. CONCLUSION

The design and experimental characterization of SiGe BiCMOS operational amplifiers with unity gain bandwidths as high as 37 GHz has been described. This record-breaking performance is achieved by (i) employing a MOS-HBT cascode stage to maximize the phase margin and (ii) by biasing both the MOSFET and the SiGe HBT at their peak  $f_{MAX}$  current densities to maximize the unity gain bandwidth of the amplifier. For the first time it is proven both theoretically and experimentally that there is direct correlation between the peak

$f_{MAX}$  current density of the MOSFET and the unity gain bandwidth of the opamp. In addition, in deep submicron technologies, the choice of large bias current densities improves the linearity and robustness of the circuit to process variation. Finally, since the peak  $f_{MAX}$  and peak  $f_T$  current densities of MOSFETs are largely invariant between technology nodes and foundries [6], the circuit can be ported to other (Bi)CMOS nodes with minimal redesign effort.

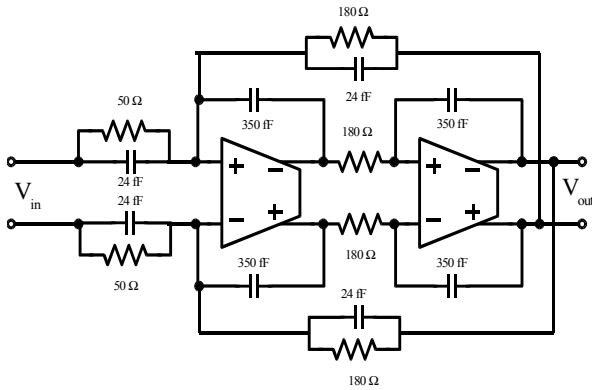


Figure 9. Biquad bandpass filter schematics

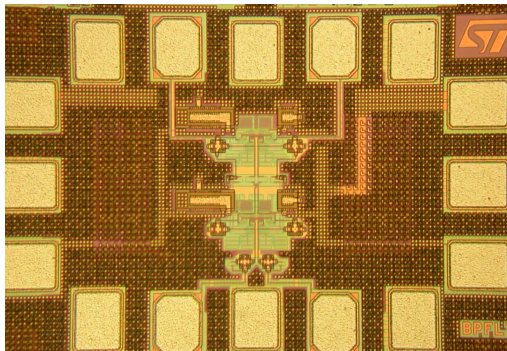


Figure 10. Opamp biquad filter die photograph. For reference, the HF pads are  $50\mu\text{m} \times 70\mu\text{m}$ .

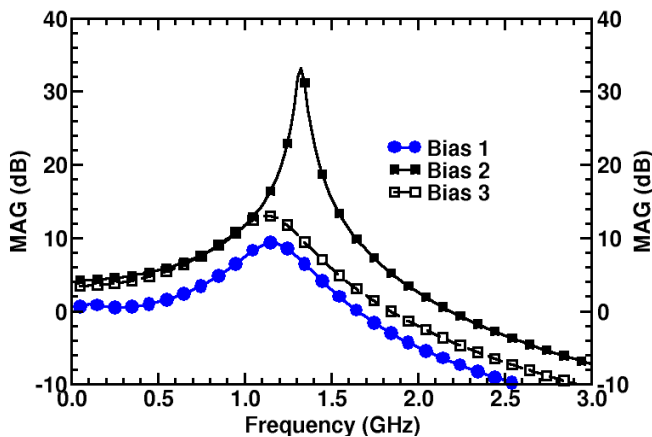


Figure 11. Measured biquad filter transfer characteristics for different bias conditions.

## ACKNOWLEDGMENTS

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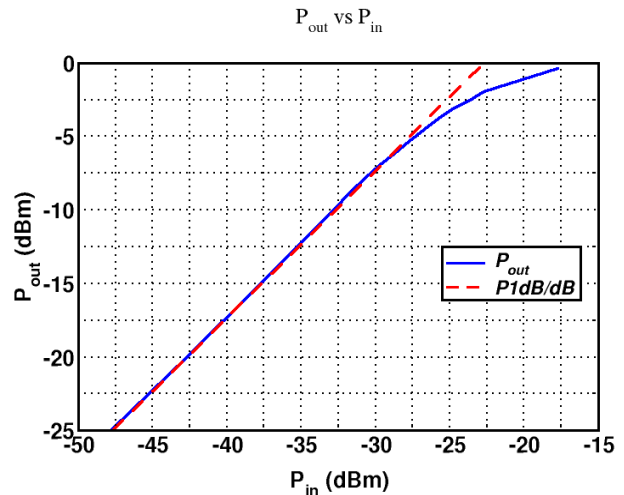


Figure 12. Measured  $P_{1dB}$  of the biquad filter.