A 40-GSamples/Sec Track & Hold Amplifier in 0.18μm SiGe BiCMOS Technology

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Abstract— This paper presents a 40-Gsamples/Sec Track & Hold Amplifier (THA). The chip is manufactured in 0.18μm SiGe BiCMOS and operates from a 3.6-V supply. The total power consumption is 540mW with a chip area of 1.1mm². Time domain measurements illustrate 40-GHz sampling with 5, 8 and 10 GHz sinusoidal input signals. S-parameter measurements show a 3-dB bandwidth of 43 GHz in track mode. The P1dB and IIP3 are -10.5 dB and 2.5 dB, respectively, at 12 GHz. The measured THD for a 19 GHz input signal is -27 dB at the input compression point and the SFDR is -30 dB for a 19 GHz input signal. When accounting for the 10 dB noise figure, the resolution of the THA is estimated to exceed 4 bits for signals with 40 Gb/s data rates.
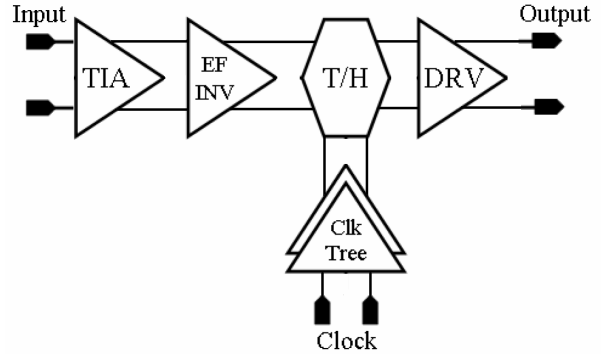
Figure 1: Simplified block diagram of the 40-Samples/Sec THA.

I. INTRODUCTION

In the past, optical fiber was considered to be an infinite medium. However, the rapid scaling of data rates of optical networks, at a factor of two every nine months, has exposed two important fiber impairments: polarization mode dispersion in single mode fibers and differential mode dispersion in multi mode fibers. Thus, to ensure error free communication at high bit rates (i.e. > 10 Gb/s), some method of data equalization is required.

It can be argued that analog equalization is more practical at high data rates than digital equalization. However, assuming high-speed Analog to Digital Converters (ADCs) can be realized, digital equalization is more robust, scalable and offers more flexibility. The design of a Track and Hold Amplifier (THA) above 10 GSamples/Sec is the first bottleneck in realization of high speed digital equalizers. This work presents a 40-GSamples/Sec THA, which to the best of our knowledge, is the fastest THA in silicon. Other lower speed THAs have been reported in [1], [2].

II. TRACK & HOLD AMPLIFIER DESIGN

Figure 1 shows a simplified block diagram of the track and hold amplifier presented in this paper. The input stage is a broadband transimpedance amplifier matched to 50Ω. An emitter follower/inverter stage precedes the track and hold block which is followed by a linear output driver designed to drive off-chip 50Ω loads. A high bandwidth clock distribution network delivers the 40-GHz clock to the THA.

A. Transimpedance Amplifier (TIA)

Since the TIA is used as an input stage, its noise figure, linearity and bandwidth determines the overall system performance. Traditionally, designers have used emitter followers and heavily degenerated inverters as input stages [2]. While this approach can provide sufficient bandwidth and linearity, using 50Ω resistive loads for matching or heavy resistive degeneration offers poor noise figure. A TIA provides simultaneous noise and signal matching without the need for a 50Ω matching resistor. Noise matching is achieved by sizing the input transistors and biasing them at minimum noise figure current density, J_{OPT}. Simulation shows the TIA has a single-ended noise figure of 10 dB at 20 GHz. An emitter-follower inverter stage with similar gain, bandwidth and linearity in this technology has a simulated noise figure of 14 dB at 20 GHz. The negative feedback of the TIA offers good linearity and high bandwidth without the need for degeneration. Signal matching is achieved by selecting the feedback resistor, R_F, and the loop gain, T, to satisfy the following equation:

$$Z_{in} = \frac{R_F}{1+T} = 50\Omega$$

The bandwidth of this stage is further enhanced by using inductive peaking, both in the feedback path and at the output [3].
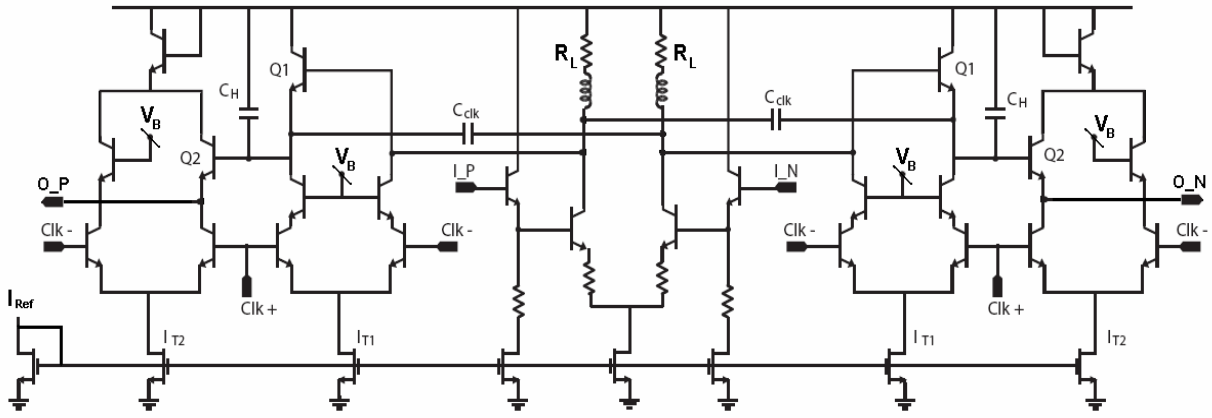
Figure 2: Circuit diagram of the emitter follower/inverter followed by the track & hold block.
I_P and I_N signals are provided by the TIA output.

B. Emitter Follower/Inverter and Track & Hold stages

The output of the TIA is fed to an emitter follower/inverter stage which in turn drives the track & hold block. Figure 2 shows the schematic of these two blocks. In track mode, Q1 and Q2 act as emitter followers and the output follows the input signal. In hold mode, the tail current I_{T1} flows through the inverter's load, R_L. The value of R_L is chosen such that the voltage drop ($I_{T1}R_L = 0.5V$) turns off transistor Q1 and provides good isolation between input and output.

The hold capacitance C_H includes the parasitic capacitances at that node and a 150fF MIM capacitor. At the clock rate of 40 GHz, significant clock feed through is added to the output signal. The capacitance C_{clk} reduces the effect of clock feedthrough in hold-mode which appears at the output of the track and hold amplifier [4]. The value of C_{clk} is chosen for a 66% reduction in hold-mode feedthrough. This results in a good balance between clock feedthrough reduction and bandwidth.

C. Clock Distribution Network (Clock Tree)

The clock path converts a single-ended clock input to a differential signal with 300mV$_{P-P}$ swing and drives four latches in phase. Its bandwidth must exceed 40 GHz. The clock distribution consists of a tree of emitter-follower inverters with a fan-out of 2. The four differential outputs of the clock tree drive the T/H circuit through double emitter-follower stages.

D. Output Driver

The output driver is designed to have an input dynamic range of 500mV$_{P-P}$ per side, provided by resistive degeneration, (20Ω), and a tail current of 24mA. The output return loss is further enhanced by inductive peaking.

III. LAYOUT AND FABRICATION

Careful attention was paid to layout symmetry. Each block consists of identical half circuits to ensure matching and low skew signal propagation, both in the signal and in the clock path.

The chip was fabricated in Jazz Semiconductor's 0.18μm SiGe BiCMOS technology with a 160-GHz f_T. The chip area is 1.1 mm^2 and the die photo is shown in Figure 3.

IV. MEASUREMENT RESULTS

The circuit operates from a 3.6-V supply and draws 150 mA. The T/H block and the clock distribution network consume 24 mA and 75 mA, respectively, while the remaining current is drawn by the input and output blocks. All measurements were conducted on-wafer.

The S-Parameter measurements were obtained with a Wiltron 360B Vector Network Analyzer and are shown in Figure 4. The input return loss is better than -15 dB up to 20 GHz and the output matching is better than -15 dB up to 40 GHz. S$_{21}$ shows a bandwidth of 43 GHz for the THA chip when the circuit is configured in track mode.
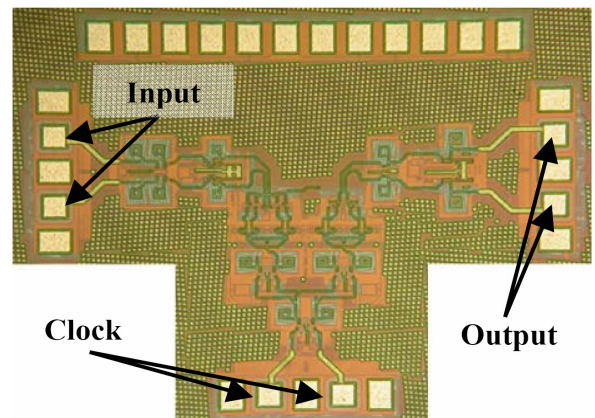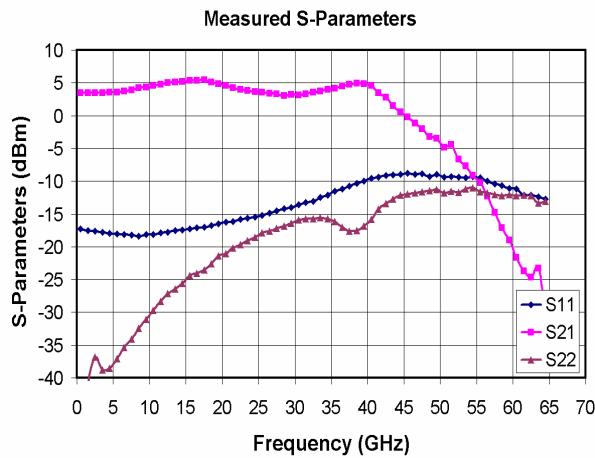

Figure 3: THA Die Photo

Figure 4: Measured Single-ended THA input return loss (S_{11}), output return loss (S_{22}) and transmission (S_{21}).

Time domain measurements were conducted using an Agilent 86100C DCA-J oscilloscope and an Agilent E8257D signal source. The two outputs of the THA were displayed on channel 3 and 4 respectively and the differential output was calculated using the scope's built in functions. A constant delay is added to one of the channels to compensate for the difference in delays between cables. The input power used is -12dBm with -16dBm of clock input power. Figure 6 shows the differential output of an 8- GHz signal sampled at 40 GHz while Figures 5 & 7 show both the single ended and differential outputs of 5-GHz and 10-GHz signals sampled at 40 GHz. The maximum single-ended clock feedthrough is 50mV, which is significantly reduced in the differential measurements.

The spectral content of the output signal was captured using an Agilent E4448A PSA spectrum analyzer. The input compression point of the circuit was measured for frequencies ranging from 2 GHz to 20 GHz, with 2-GHz steps, and is illustrated in Figure 8.
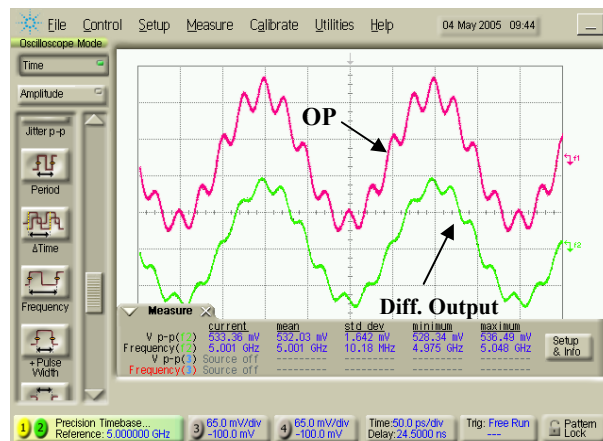

Figure 5: Differential (150mV/Div scale) & single-ended outputs of a 5-GHz sinusoid sampled at 40 GHz.
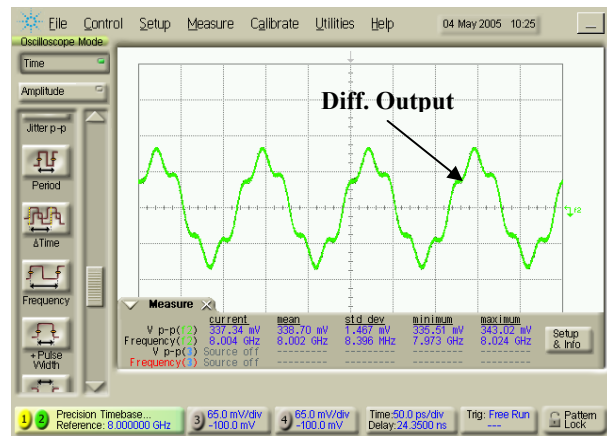

Figure 6: Differential output of an 8-GHz sinusoid sampled at 40 GHz, shown on a 100mV/Div scale.
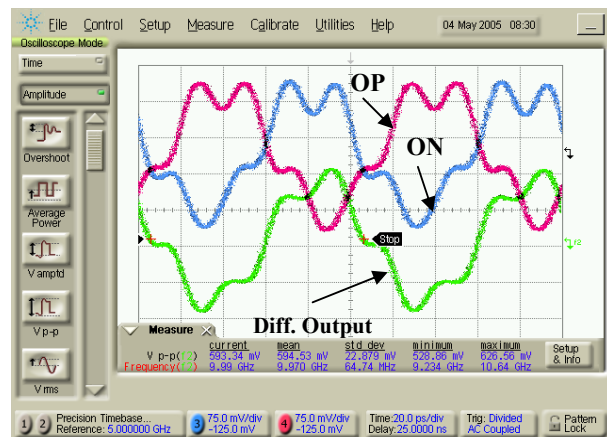

Figures 7: Differential (150mV/Div scale) & single ended outputs of a 10-GHz sinusoid sampled at 40 GHz.
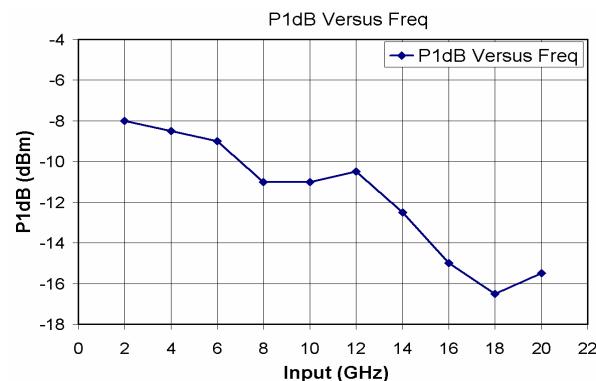

Figure 8: Measured P1dB versus input frequency

Figures 9 and 10 show the spectrum for two tone tests at 11 GHz and 19 GHz, respectively, for input signals of -14 dBm and -24 dBm. Figure 11 shows the measured IIP_3 as a function of frequency. The input-referred noise power spectral density of the THA obtained from simulation is $6nV/\sqrt{Hz}$ at 40 GHz. With a noise bandwidth of 40 GHz and SNR of 7 dB, this translates to a minimum detectable signal of -42 dBm and an SFDR of 30 dB for a 19 GHz input signal and 33 dB for a 10 GHz input signal.
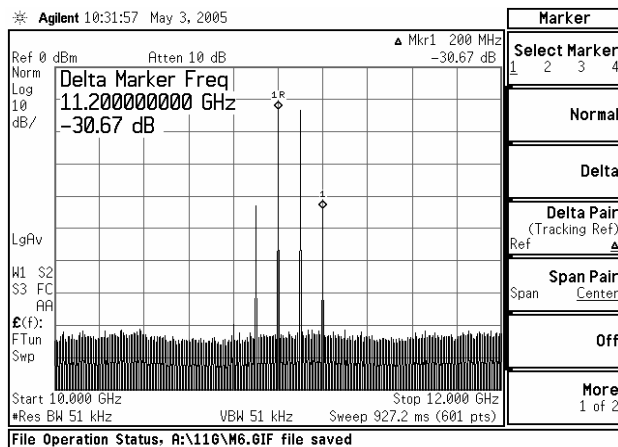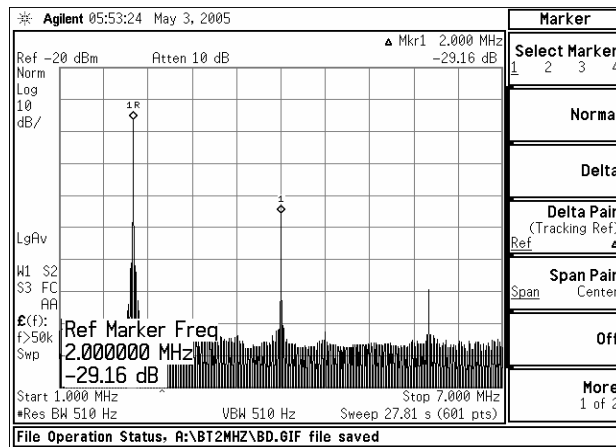
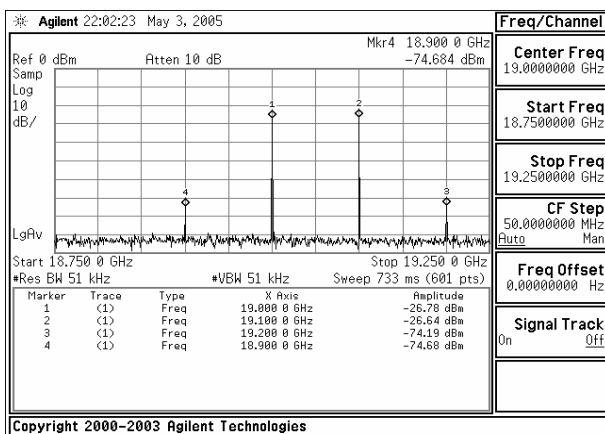**Figure 9:** Spectrum of IIP3 measurement at 11 GHz

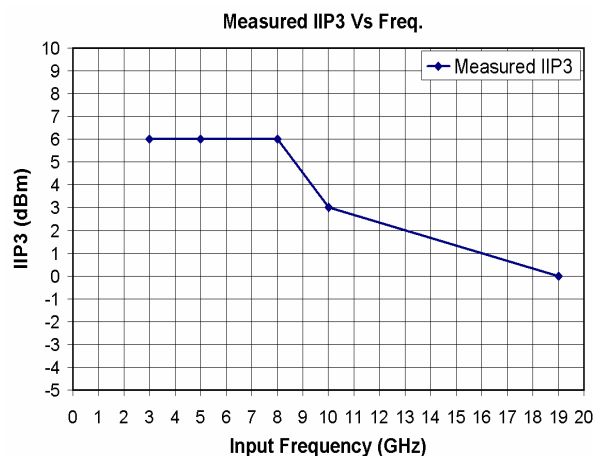**Figure 10:** Spectrum of IIP3 measurement at 19 GHz

Figure 11: Measured IIP3 versus input frequency

The measured THD for a 19 GHz input signal is -27 dB, and for a 10 GHz input signal is -29 dB, both measured at the input compression point. The spectral characteristics of the beat frequency test with $f_{in} = f_s + \Delta f$, $f_s = 40$ GHz, and $\Delta f = 2$ MHz is shown in Figure 12 with THD better than -26 dB measured at -20 dBm of input power.

Figure 12: Beat frequency test: input signal at 40.002-GHz sampled at 40 GHz

V. CONCLUSION

A 40-GSample/Sec THA was design and fabricated. The input and output matching are better than -15dB up to 20 GHz and up to 40 GHz respectively and the 3-dB bandwidth is 43 GHz in track mode. Input compression point of -10.5dBm at 12 GHz and IIP_3 of 2.5dBm at 12 GHz have also been measured. Time domain measurements verify sampling behaviour of the circuit with 5, 8 and 10-GHz input signals. The circuit shows an SFDR of 30 dB and 33 dB for input signal frequencies of 19 GHz and 10 GHz respectively and has a THD of better than -26 dB with a beat frequency test with input signal at 40.002 GHz. Based on the measurement results, the THA has a linearity of better than 4-bits and therefore can be used as a front end of an ADC with 4-bits of resolution.

VI. ACKNOWLEDGMENTS

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