An Inductor-Based 52-GHz 0.18 µm SiGe HBT Cascode LNA with 22 dB Gain

Michael Gordon,
Sorin P. Voinigescu

University of Toronto
Toronto, Ontario, Canada

ESSCIRC 2004, Leuven, Belgium

Outline

- Motivation
- LNA Topology Comparison
- Inductor-Based LNA Design
- Fabrication
- Measurement Results
- Conclusion
- Future Work

Work Motivation

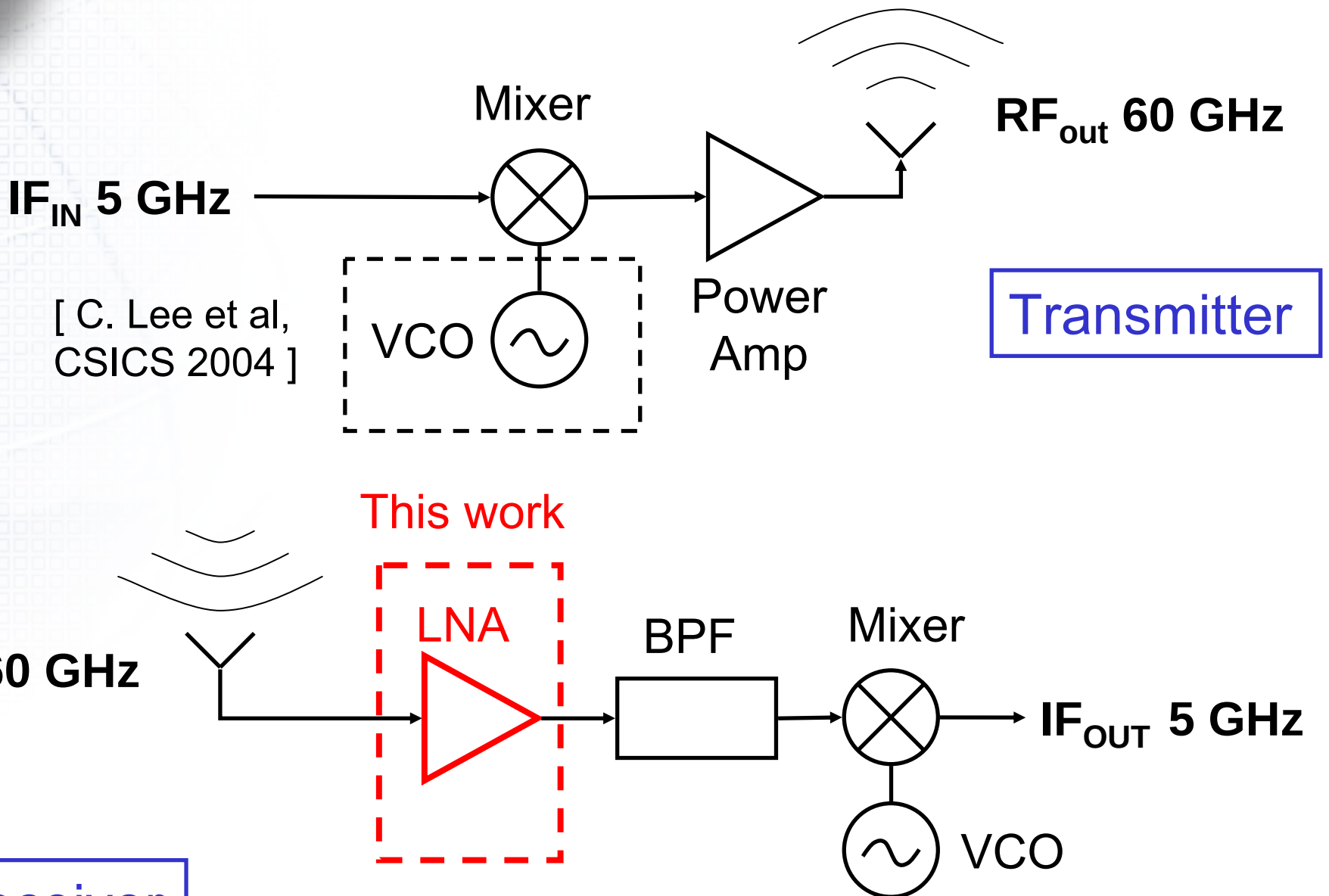
- 60-GHz WLAN (57-64 GHz)
- GigaBit Ethernet in 70-GHz and 80-GHz band
- 77-GHz Automotive RADAR

- mm-wave design advantages over 5-10 GHz RF
  - Simpler and robust super-heterodyne radio architecture (A lot of bandwidth available)
  - Smaller passives and die area (lower cost)
  - Smaller antenna with higher gain

Research Goals

- Study the feasibility of Si-based transceiver blocks for mm-wave applications
- Develop a mm-wave LNA design methodology
- Assess modeling limitations of active and passive components at mm-wave frequencies
  - Inductors
  - SiGe HBTs

Transceiver Overview



Choice of Technology

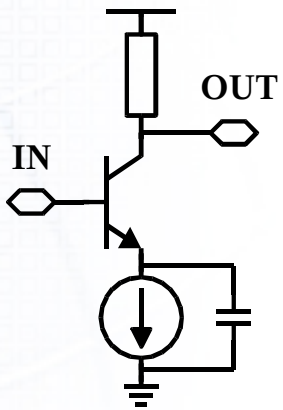
	f_T, f_{MAX}	Integration	Noise Figure	Breakdown voltage	Mask Cost
InP HBT	160	low	high	high	low
InP HEMT	170	low	low	low-medium	moderate
0.18µm SiGe	150	high	high	medium	low
90nm CMOS	140	high	low	low	high

[S.P. Voinigescu et al, SiRF 2004]

- CMOS NF < SiGe NF (in simulation)
- SiGe transistor NF_{min} of 5 dB stresses LNA design

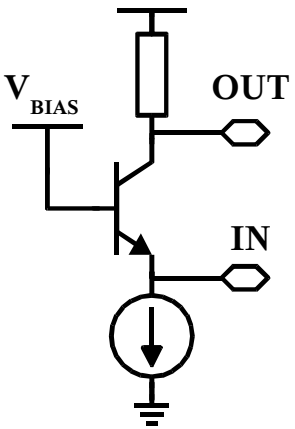
Basic LNA Topologies

Common-Emitter



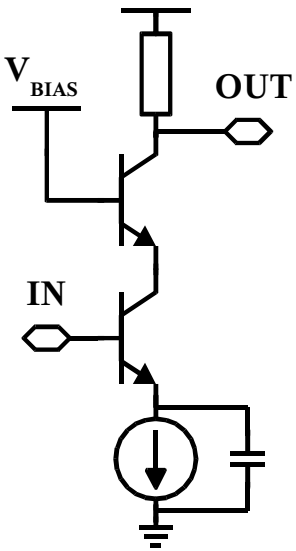
- Concurrent noise / input match

Common-Base



- Simple input match

Cascode



- Concurrent noise / input match
- Increased Gain
- High Isolation
- Increased Noise

First iteration tape-out at mm-wave frequency:

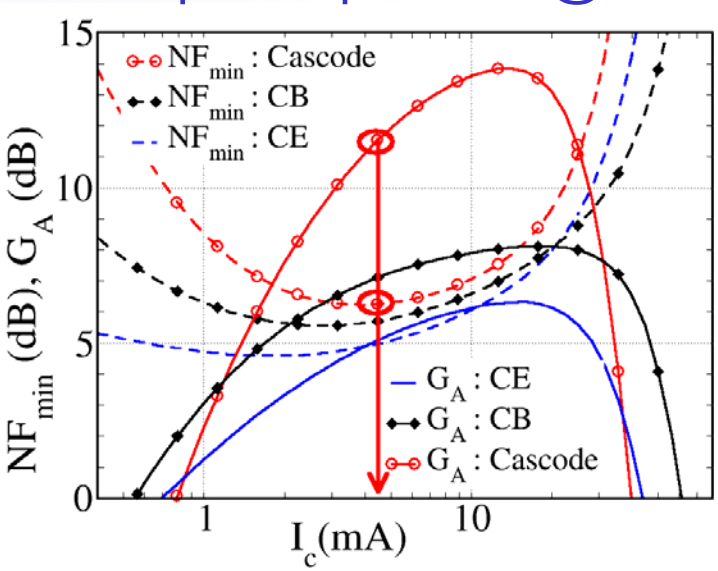
Topology must be insensitive to transistor model inaccuracies and process variations

LNA Topology Comparison

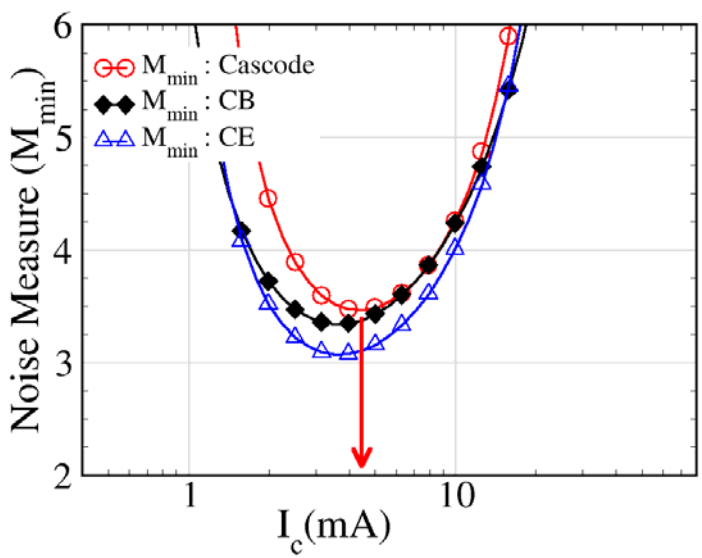
- Low gain at mm-wave frequencies (**need multi-stage**)
  - Use Noise Measure for comparison
- CE: lowest M_{min}, but lowest G_A
- Parasitics and emitter degeneration reduce gain
- **Cascode is the safe choice with high G_A and robustness**

$$M_{\min} = \frac{F - 1}{1 - \frac{1}{G_A}}$$

NF_{min}, G_A simulation
2 x 6.4μm/0.2μm HBT @ 52 GHz



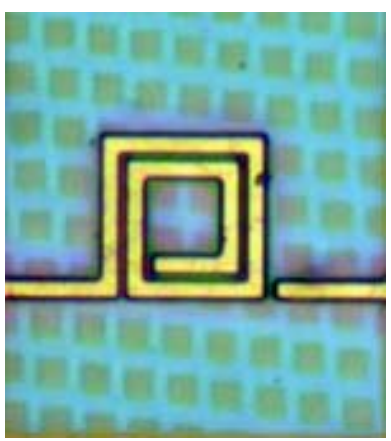
Calculated M_{min}



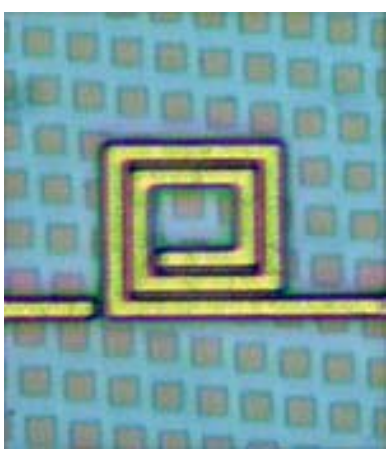
Inductor-Based LNA Design

- 60 GHz LNA in [S. Reynolds et al, ISSCC 2004] uses transmission-lines for matching and loading
- Inductors can replace transmission-lines
  - Smaller – **significant die area reduction**
  - L-C networks for input and output matching
- Need to be able to **design** inductors for mm-wave frequencies and **model** them accurately

29 μm



330 pH
Stacked Inductor



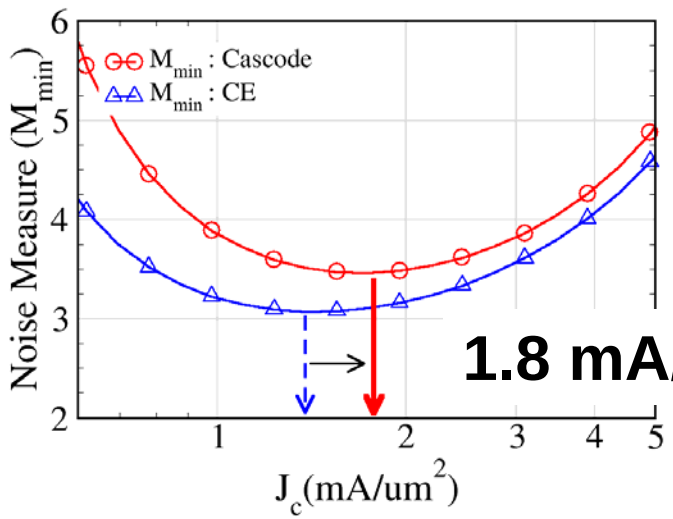
32 μm

440 pH
Stacked Inductor

Cascode Design Methodology

- Extension to an LNA Design Methodology presented in [S. Voinigescu et al, JSSC Sep '97] for 2-6 GHz

1. Starting with the cascode, bias it at its M_{min} current density (J_{OPT})



2. At J_{OPT}, size Q1-Q2 emitter lengths to match the real part of the optimum noise impedance (R_{sop}) to Z_o

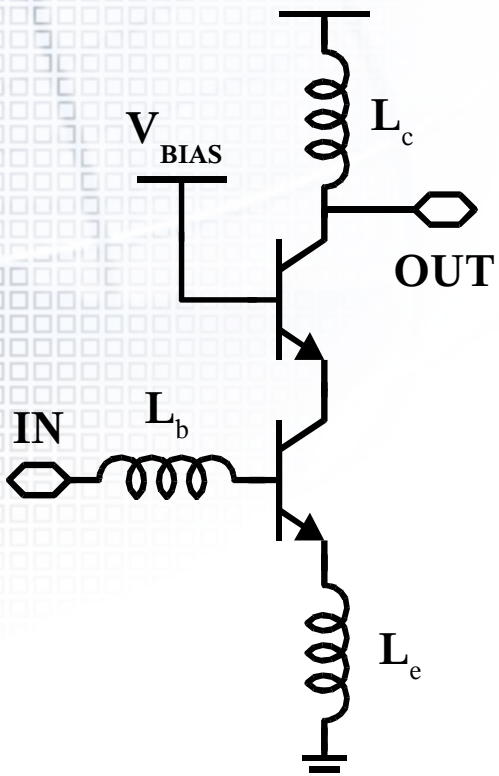
$$R_{sop} \sim l_e^{-1}$$

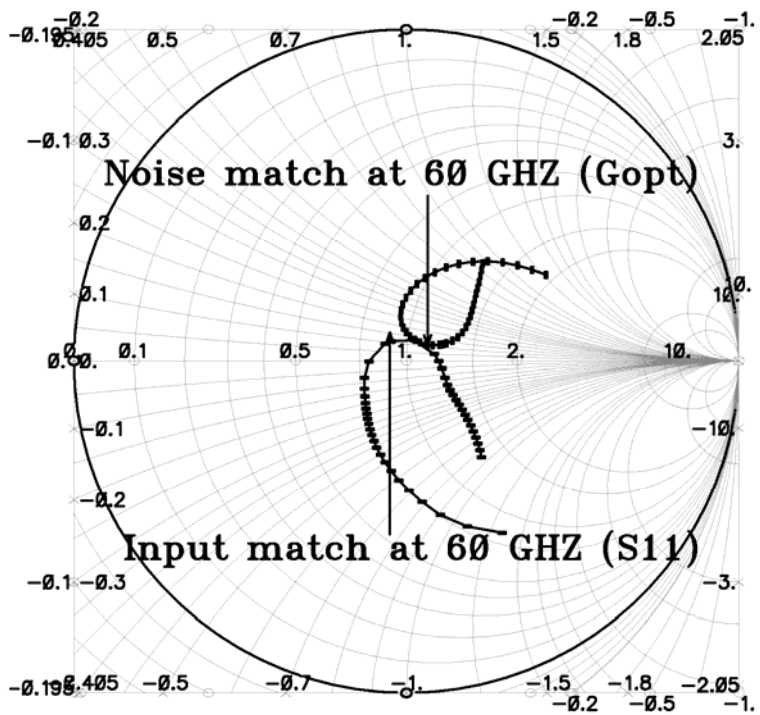
Cascode Design Methodology cont.

3. Add L_E and L_B to match Z_{IN} to Z_o

4. Add L_C to resonate the tank at the desired frequency

$$\mathrm{Re}\{Z_{IN}\} = \frac{L_e(2\pi f_T)}{\left(\frac{C_\pi + 2C_\mu}{C_\pi + C_\mu}\right)}$$





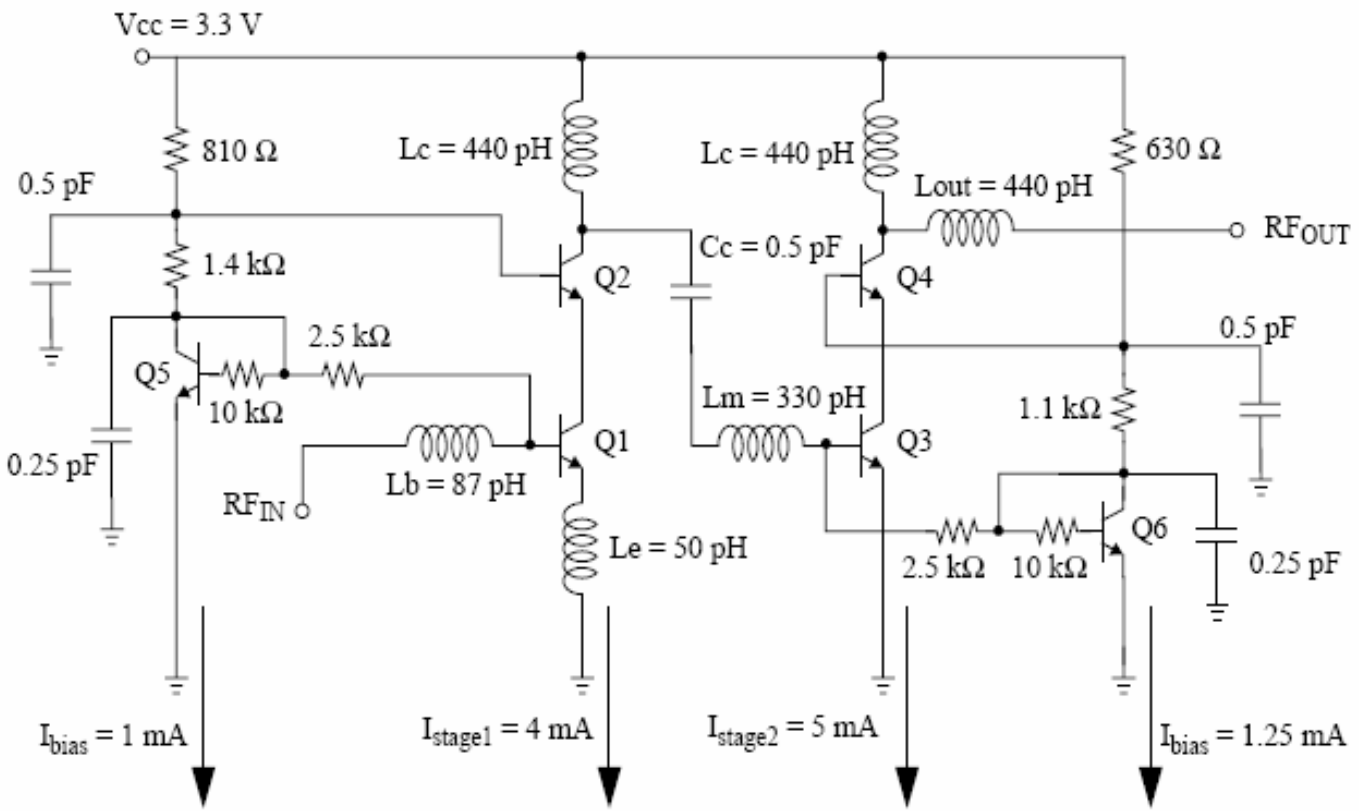
Concurrent input impedance and optimum noise impedance match

LNA Schematic

- Use two stages for higher gain
- Inter-stage matching inductor to improve power transfer
- Low-pass noise filtering of bias network

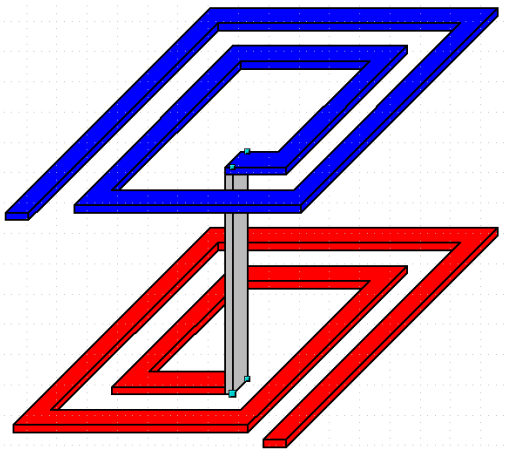
Q1-Q4:
2 x 6.4µm / 0.2µm

Bias Q5-Q6:
2 x 1.7µm / 0.2µm

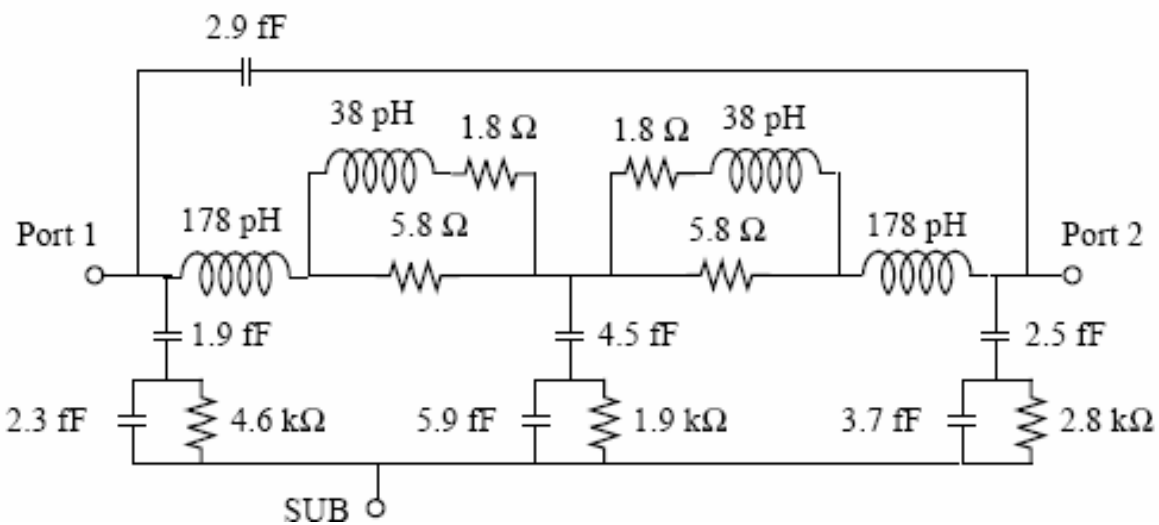


mm-wave Inductor Modeling

- mm-wave inductor design technique [T. Dickson et al, IMS 2004]
  - Use 3D stacked inductors
- Modeled using the ASITIC software tool
- Extracted compact 2-π inductor models used in circuit design



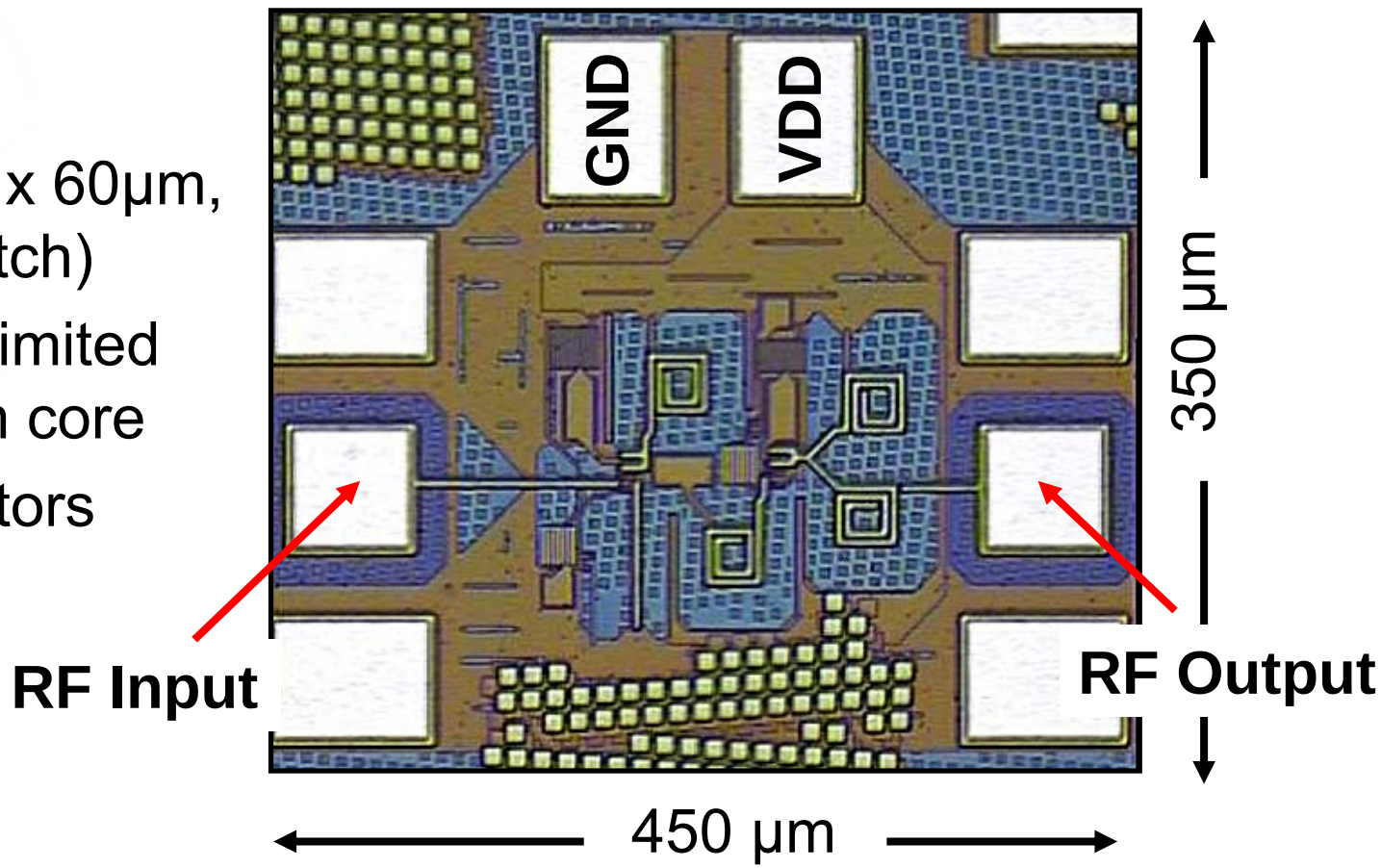
440 pH inductor



Fabrication

- Fabricated in Jazz Semiconductor's production 0.18 µm SiGe120 BiCMOS process

- Standard 60µm x 60µm, pads (100µm pitch)
- Die size is pad limited 250µm x 200µm core
- 4 stacked inductors 2 wire inductors

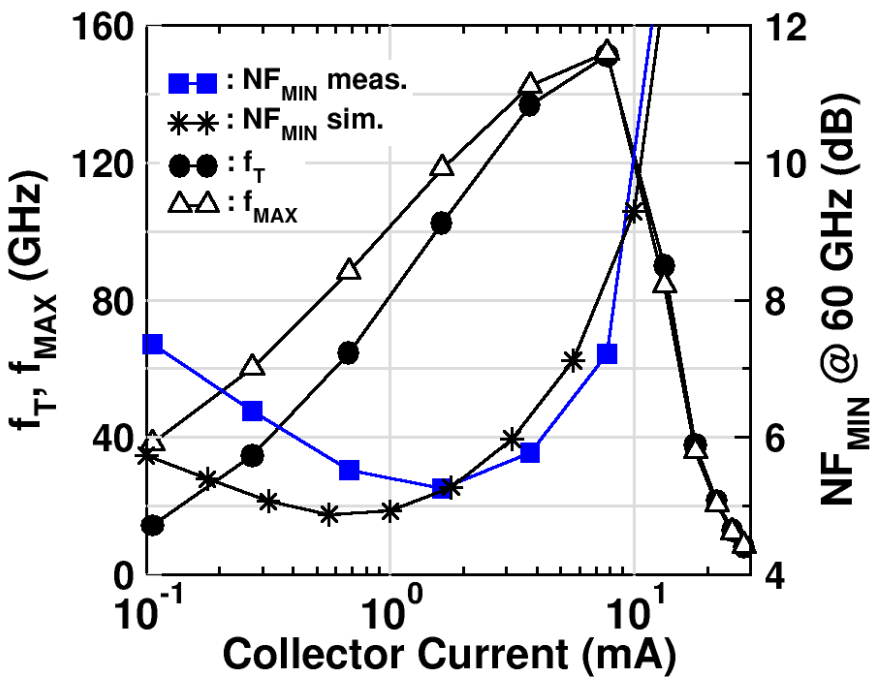


Transistor Measurements

- NF_{min} extracted from measured Y-Parameters
  - Shown to be a valid technique for frequencies below $f_T / 2$ [S. Voinigescu et al, JSSC Sep '97]

- f_T and f_{MAX} = 150 GHz
- NF_{min} @ 60 GHz = 5.2 dB
- Good agreement with HBT model

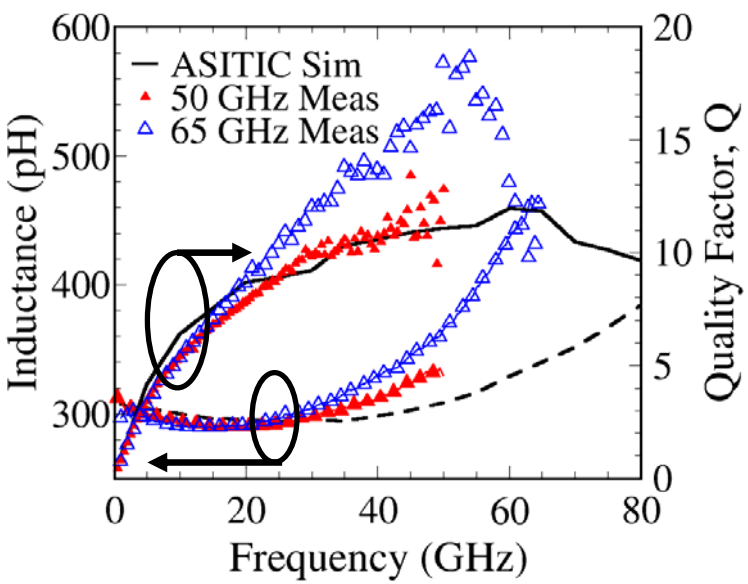
f_T, f_{MAX}, NF_{min} @ 60 GHz
2 x 2.6µm/0.2µm HBT



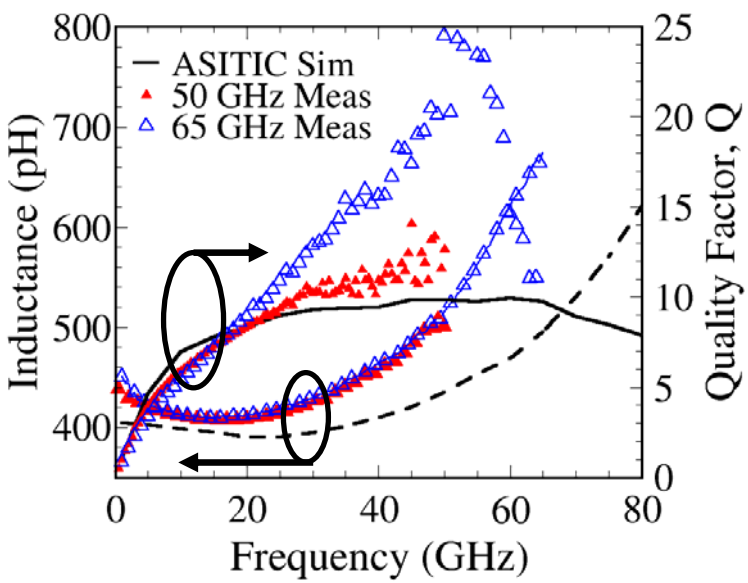
Inductor Measurements

- Short and Open test-structure de-embedding
- Inductance is 15% higher than simulated
- SRF (Self-Resonance-Frequency) is lower for the 3D stacked inductors than simulated
- Measured Q > 10 at 50 GHz

330pH Inductor L and Q



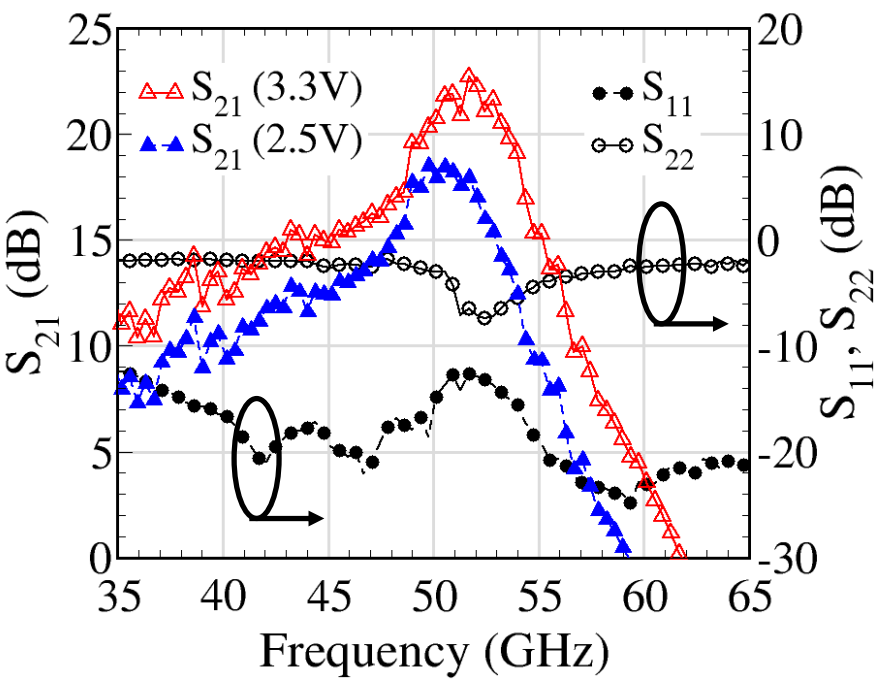
440pH Inductor L and Q



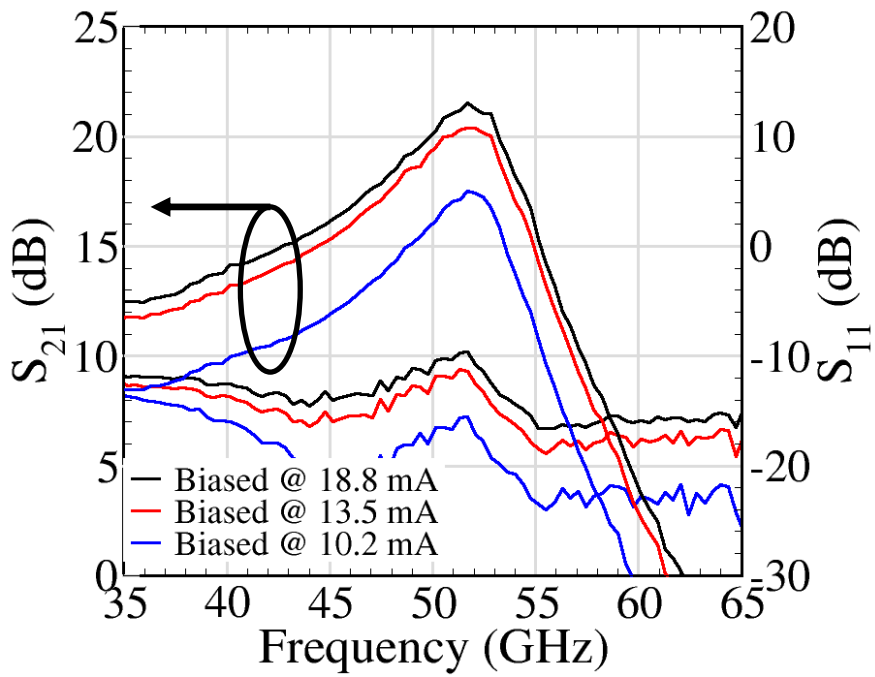
S-parameter Measurements

- **22 dB Gain at 52 GHz**
- **LNA Peak frequency is dictated by tank inductor**
  - Lower inductor SRF shifts the peak to lower frequency
  - Biasing does not affect peak frequency

LNA S-parameters

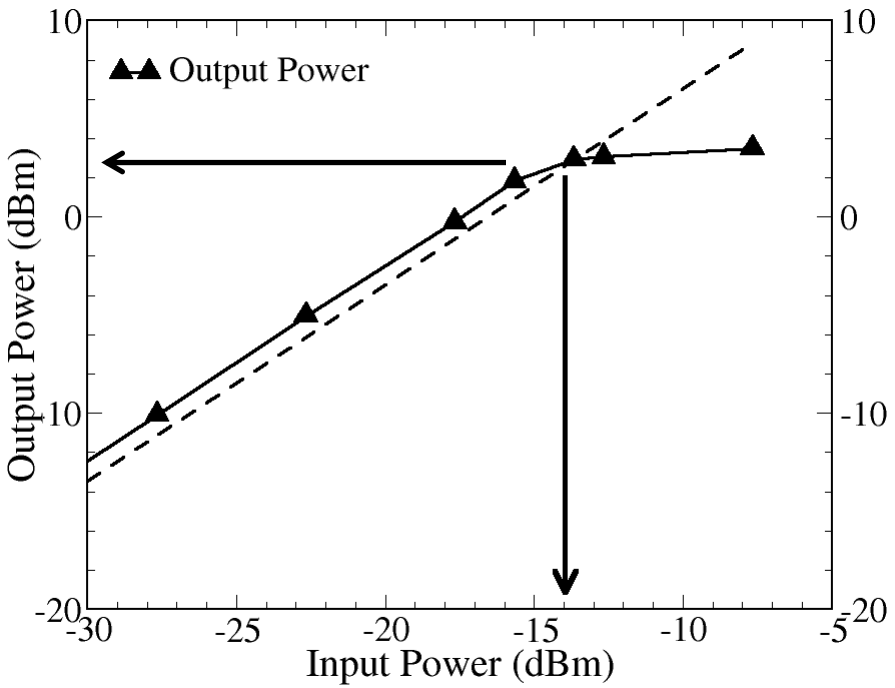


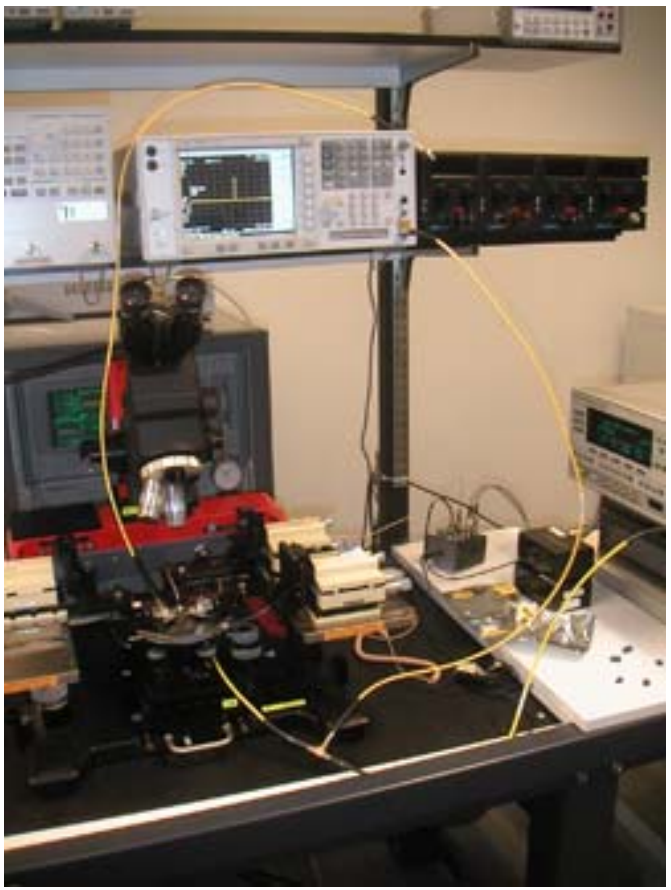
Biasing effect on gain peak



Linearity Measurements

Measured 1dB compression at 50 GHz (V_{CC}=3.3V)





- Input 1 dB compression point of **-14 dBm**
- Output 1 dB compression point of **3 dBm**

Comparison to other work

	Tech	Gain (dB)	NF (dB)	P_{IN1dB} (dBm)	Power (mW)	Area	FOM
22 GHz [X. Guan, JSSC Feb 2004]	0.18µm CMOS	15	6.0	-	24	*0.05 mm²	-
24 GHz [H. Hashemi, ISSCC 2004]	0.18µm SiGe	25	3.8	-	20	-	-
60 GHz [S. Reynolds, ISSCC 2004]	0.12µm SiGe	17	4.2	-20	11	0.77 mm²	1.72
52 GHz This work (3.3V)	**0.18µm SiGe**	**22**	**7.5**	**-14**	**38**	**0.16 mm²**	**1.88****
52 GHz This work (2.5V)	**0.18µm SiGe**	**18**	**7.9**	**-18**	**19**	**0.16 mm²**	**0.53****

$$LNA_{FOM} = \frac{G * P_{IN1dB} * f}{(NF - 1) * P}$$

* Area without pads

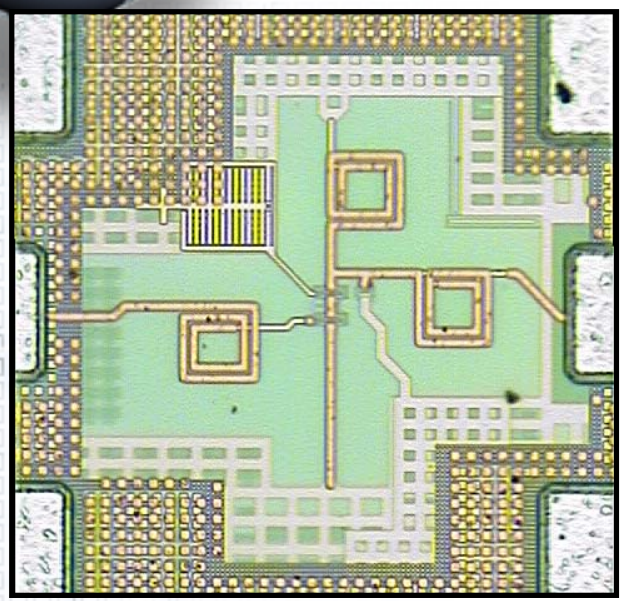
** Simulated Noise Figure

Summary and Conclusion

Gain	22 dB at 52 GHz
S_{11} / S_{22}	< -12 dB / -5 dB
NF	7.5 dB (simulated)
Isolation	< -30 dB
P_{IN1dB} / P_{OUT1dB}	-14 dBm / +3 dBm
Power	38 mW (11.4 mA from 3.3V)

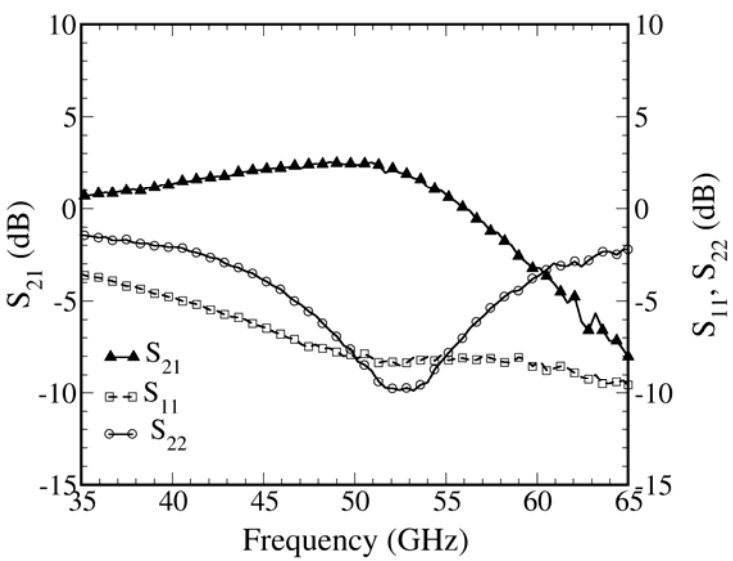
- 52 GHz LNA with 22 dB gain using a production 0.18µm SiGe BiCMOS technology
- Fully inductor-based circuit operating above 50 GHz
- Significant die-area reduction over the use of transmission lines

Future work: 90nm CMOS LNA

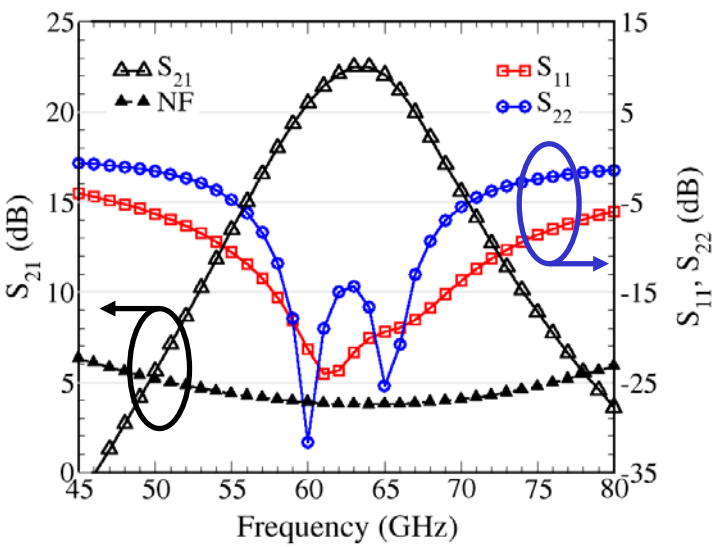


- CMOS f_T and f_{MAX} = 140 GHz
- Single-stage cascode LNA
  - 2.5 dB gain at 52 GHz
  - Uses 3D stacked inductors
- Peak shift down due to tank inductor

Measured 1-stage



Future - Simulated 2-stage



S_{21} = 22 dB

NF = 4 dB

Acknowledgements

- Kenneth Yau for SiGe HBT characterization
- Jazz Semiconductor for financial support and fabrication
- NSERC
- Micronet
- Canadian Wireless Telecom Association