An Inductor-Based 52-GHz 0.18 μm SiGe HBT Cascode LNA with 22 dB Gain

Michael Gordon and Sorin P. Voinigescu

University of Toronto, Toronto, ON, Canada
E-mail: gordon@eecg.utoronto.ca

Abstract

A 52-GHz two-stage cascode LNA implemented in a production 0.18 μm SiGe BiCMOS process is presented. By using inductors rather than transmission lines for matching, it occupies an area of only 200 μm x 250 μm. The circuit features standard 60 μm x 60 μm bond pads, on-chip bias network, and consumes 11.4 mA from a 3.3 V supply. The measured S_{11} is lower than -12 dB from 35 GHz to 65 GHz and S_{21} exceeds 22 dB. The gain remains above 18 dB when the supply voltage and power dissipation are reduced to 2.5 V, and 19.5 mW, respectively.

1. Introduction

The emergence of commercial 3-rd generation SiGe BiCMOS technologies with SiGe HBT cutoff f_T and oscillation f_{MAX} frequencies exceeding 160 GHz [1-3] has recently drawn the attention of the silicon foundry and design communities to mm-wave applications such as 60-GHz WLAN, 77-GHz automotive radar, and wireless GigaBit Ethernet networks in the newly licensed 70-GHz to 80-GHz band [4]. Traditionally, GaAs and InP have dominated this frequency range but silicon, with its high level of integration, is likely to become the technology of choice for these markets. SiGe HBT VCOs have already demonstrated adequate phase noise and output power for automotive radar [5]. More recently, 60-GHz radio receiver blocks implemented in 0.13 μm SiGe HBT technology have been reported [6].

Interest in 60-GHz radio comes from the fact that it can provide similar bandwidth as the 3-10 GHz ultrawideband radio while making use of the same low-cost fabrication technology. Furthermore, simpler narrow-band system architectures can be used at 60 GHz. The greatest advantage, however, stems from the reduced wavelength which makes it possible to integrate the antenna or phased array antennae [7], with the RF and digital circuitry on a single silicon die. The latter feature truly paves the way for wearable gigabit-rate multimedia platforms and mm-wave sensors by elegantly avoiding the potentially high cost of mm-wave packaging.

Given the relatively small wavelength at 60 GHz ($\lambda/4 \sim$ 600 μm in SiO_2), circuits operating at these frequencies typically use transmission lines as matching elements [5,6], a common practice in III-V microwave ICs. Even so, transmission lines account for more than 80% of the total die area. It has been recently demonstrated [8] that mm-wave inductors with Q's exceeding 10 above 50 GHz can be fabricated with an extremely small footprint in silicon. These inductors can replace transmission lines at mm-wave frequencies to achieve the required inductance while occupying much smaller die area.

Compared to the LNA in [6], which features a common-base input stage and transmission lines as matching elements, the circuit proposed in this paper employs inductors to minimize area and uses a cascode topology in concert with an active-matching design methodology to achieve simultaneous optimal noise and input impedance match. To the best of the authors' knowledge, this is the first inductor-only circuit operating above 50 GHz. An analysis of different LNA topologies and the design methodology for cascode stages is discussed in the next section. The experimental results are presented in section 3 followed by the conclusion.

2. LNA Topology and Design Methodology

The design of mm-wave LNAs poses more challenges than at RF frequencies because transistors operating at frequencies close to f_t have low available gain (G_A) and high minimum noise figure (NF_{min}). Biasing at the minimum-noise current density further reduces the gain. This trade-off between noise and gain is illustrated in Fig. 1 for three commonly used LNA stages: common-emitter (CE), common-base (CB), and cascode. Since the gain of the CE and CB configurations is too small for a single stage amplifier, a more appropriate figure of merit to be used in comparing different topologies is the minimum noise measure (M_{min}). The latter captures both noise and gain characteristics and is defined as

$$M_{min} = \frac{F_{min} - 1}{1 - \frac{1}{G_A}}$$

where F_{min} is the minimum noise factor. Fig. 1 shows the simulated G_A and NF_{min} for CE, CB, and cascode topologies as a function of collector current for transistors with total emitter length of 12.8 μm. The noise measure is calculated for each configuration at the minimum-noise bias:

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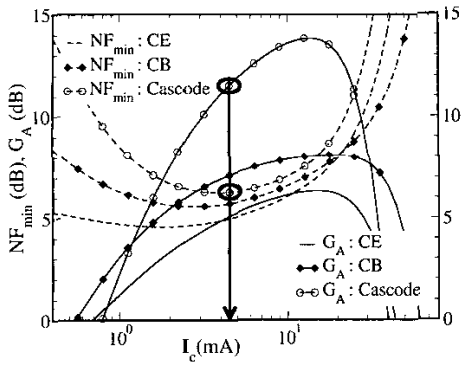

Fig. 1: Simulated NF_{min} and G_A at 52 GHz for common-emitter, common-base, and cascode configuration versus the bias current (V_{CC} is 1.5 V for CE, CB and 2.5 V for cascode).

M_{CE}=3.75, M_{CB}=3.40, M_{casc}=3.47. This analysis shows that a CB topology would result in a slightly better overall noise figure than a cascode stage. However, the calculated noise measure assumes a concomitant optimal noise and power match. The latter is non-trivial, if at all possible, for a CB configuration, leading to a higher M_{min} in practice. The cascode stage can be concurrently matched making it the preferred topology for LNA design, even at mm-wave frequencies. Furthermore, the higher gain per bias current and the better isolation of the cascode stage render the design simpler and more robust to model inaccuracies, an important consideration above 50 GHz.

A design methodology applicable to CE and cascode topologies to realize simultaneous noise and power match was presented in [9] and was applied in the design of cascode LNAs in the 2-GHz to 6-GHz range. That technique, with minor modifications, is extended in this paper to circuits operating above 50 GHz.

A. Low Noise Cascode Design Methodology

The design technique consists of 4 steps which leads to the best possible overall noise figure:

1. With transistors Q_1 and Q_2 sized equally, the cascode is biased at its minimum-noise current density (J_{opt}) as illustrated in Fig. 1. This departs from the original design methodology, in which the optimal bias current density was determined for the individual transistor and which is considerably lower than that of the cascode.
2. While maintaining J_{opt}, the size of Q_1 and Q_2 is modified such that the real part of the optimum noise impedance R_{sop} equals the source impedance Z_0

$$R_{sop} \cong \frac{R_n f_T}{f} \frac{1}{\sqrt{\frac{I_C}{2V_T}(r_e + r_b)\left(1 + \frac{f_T^2}{\beta_0 f^2}\right) + \frac{f_T^2}{4\beta_0 f^2}}}$$

$$R_n \cong \frac{V_T}{2I_C} + (r_e + r_b) - l_e^{-1}$$

where β is the dc current gain, r_e is the series emitter resistance, r_b is the total base resistance, R_n is the noise resistance, and l_e is the emitter length. Given the inverse relation of R_{sop} to frequency and emitter length, a match to 50 Ω can be obtained with a shorter emitter at 60 GHz as compared to a lower frequency design.

3. Next, the input impedance is matched by adding an emitter degeneration inductor L_e and an inductor in series with the base, L_b. The latter also tunes out most of the imaginary part of the optimum input noise impedance. Comparing to design at RF, smaller inductance values are required at 60 GHz.
4. Finally, to complete the cascode stage design, the value of the load inductor L_c is chosen to resonate with the parasitic capacitance of the output-node at the desired operating frequency.

Since smaller devices and inductors are needed for optimum matching, mm-wave LNAs benefit from smaller bias currents, smaller chip area, and, hence, lower cost than their RF counterparts

B. LNA Circuit Description

The full schematic of the proposed 60-GHz, two-stage cascode LNA is shown in Fig. 2. The first cascode stage was designed using the method described above. Fig. 4

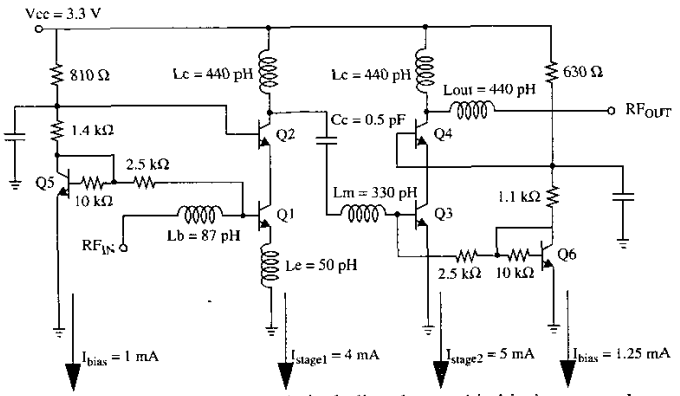

Fig. 2: LNA circuit schematic including the on-chip biasing network.

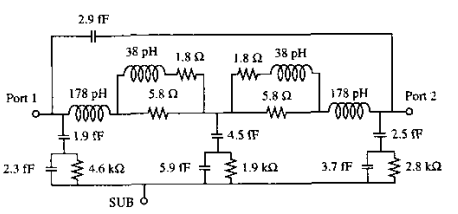

Fig. 3: 440-pH inductor 2-π model.

illustrates the simulated power gain, input return loss, and optimum noise reflection coefficient. The latter two are lower than -20 dB around 60 GHz. In an effort to reduce base and collector resistance, transistors Q1-Q4 have 3 base contacts, 2 emitter, and 2 collector stripes. This transistor layout, 2 x 6.4 μm x 0.2 μm, with total emitter length of 12.8 μm, leads to a lower noise figure and higher f_t and f_{max} values without suffering significant self-heating. As a results of their sub-100 pH values, L_b and L_e are implemented as simple line inductors. The other four inductors are implemented as multi-turn stacked spirals.

A second cascode stage is needed to increase the overall gain of the LNA. It is biased at a slightly higher current density and emitter degeneration is omitted to obtain higher gain. Inductor L_m was added to resonate out the parasitic capacitance between the two stages. As the frequency of operation increases, on-chip inter-stage matching becomes necessary to obtain the best performance.

Both cascode stages are biased using modified current-mirrors. The current mirrors are connected through large 2.5 kΩ resistors which prevent the noise generated by the bias circuit to feed-through to the RF path. The Q1:Q5 and Q3:Q6 size and current ratios is 4:1, corresponding to base resistor ratios of 10 kΩ : 2.5 kΩ. The LNA requires no external components and no bias tweaking.

C. Inductor Design

Inductors used at 60 GHz must have self-resonance-frequencies (SRF) exceeding 100 GHz. For a given technology the L*SRF product is constant and sets a physical limit on the largest inductor value achievable. The main factor degrading the SRF is the parasitic capacitance to the substrate, while Q is primarily limited by the losses in the silicon substrate. Both SRF and Q can be improved by making the inductor footprint as small as possible.

3-D multi-metal spiral inductors were designed following the guidelines described in [8]. By using series stacked windings realized in the top two metals with minimum metal stripe width and spacing, very high inductance per area is obtained. The resulting 330-pH and 440-pH inductors have a total of 4 turns and occupy a die area of 29 μm x 29 μm and 32 μm x 32 μm, respectively. All inductors were modeled using ASITIC [10] from which a 2-π equivalent circuit was extracted and employed in LNA simulations. Skin effect parameters were added to the model to account for the increased resistance at higher frequencies. The full 2-π model for the 440 pH inductor is show in Fig. 3. Reverse-biased p-n junction guard-rings were placed on three sides of each inductor at a distance of 15 μm to reduce cross-talk and improve inductor Q. The contribution of the interconnect lines to the overall inductance was accounted for during extraction. Empirical observations confirmed by ASITIC simulations show that a thin interconnect line has an inductance of about 1 pH / μm. 30-40 pH of interconnect inductance was added to every inductor.

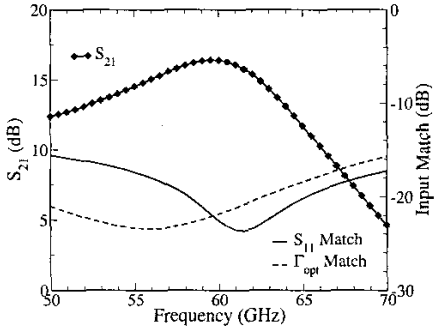

Fig. 4: Simulated gain, input return loss, and optimum noise reflection coefficient Γ_{opt}.

3. Experimental Results

The LNA was fabricated in Jazz Semiconductors' 0.18 μm SiGe120 BiCMOS process [1] with 160 GHz f_t and f_{max}. The resulting die area (Fig. 5) is only 250 μm x 200 μm = 0.05 mm^2 (excluding the pads) and 350 μm x 450 μm = 0.16 mm^2 (including the pads). The circuit features high-Q 60 μm x 60 μm bond pads, shielded from the substrate by a reversed biased, low-resistance n-well. Measurements were performed directly on a 2.5 mm x 5 mm multi-test circuit die using 65-GHz GGB probes and a 65-GHz Anritsu network analyzer.

The measured L_{eff} and Q for the 330-pH and 440-pH inductors used in the LNA are illustrated in Fig. 6 (a) and (b), respectively. Quality factor values above 12 were measured for both inductors at 50 GHz. The pads and interconnect lines were de-embedded using a two-step technique with dummy open and dummy short test structures. The dummy open has 12 fF capacitance while the dummy short has 45 pH inductance and less than 1 Ohm series resistance up to 50 GHz. The measurement error is estimated to be less than one tenth of the dummy open and dummy short capacitance and inductance, respectively. For comparison, the effective L_{eff} and Q predicted by ASITIC prior to tape-out are also plotted in Fig. 6. ASITIC simulations are accurate at lower frequencies,

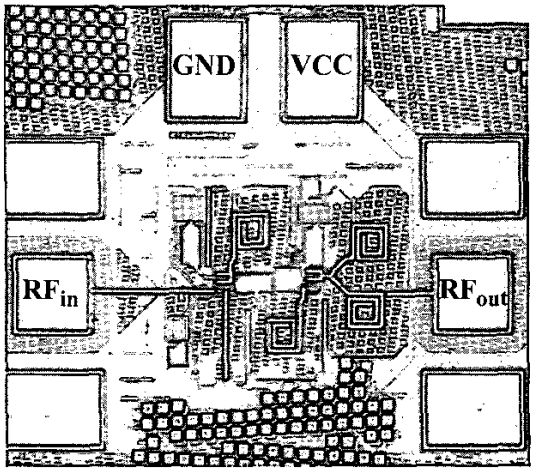

Fig. 5: Die photo of the designed LNA. There are four stacked spiral inductors and two line inductors.

but underestimate L_{eff} by about 15% at 50 GHz.

The measured LNA S-parameters are plotted in Fig. 7. As a result of the strong inductive feedback which ensures that the real part of the input impedance is close to 50 Ω, S_{11} is lower than -12 dB from 35 GHz to beyond 65 GHz, and better than -20 dB from 55 GHz to 65 GHz. The isolation S_{12} is lower than -30 dB up to 65 GHz while the S_{21} peak is 22.7 dB at 52 GHz. The measured peak gain frequency is 15% lower than the target 60 GHz value. This discrepancy can be explained by the larger measured value of L_c and by accounting for 10 fF of interconnect parasitic capacitance at the output of each cascode stage. The resonant peak frequency is insensitive to transistor bias current or supply voltage.

The LNA was designed for a nominal supply of 3.3 V and 11.4 mA. It was still operational with 18.5 dB gain from a 2.5 V supply and a total current of 7.8 mA.

4. Conclusion

A two-stage 52 GHz LNA was designed having peak gain of 22 dB and S_{11} lower than -12 dB from 35 to 65 GHz. When operated from a reduced 2.5 V supply, power consumption is 19.5 mW with more than 18 dB gain. Four stacked mm-wave inductors were used for matching resulting in a die area of only 0.16 mm^2. Compared to a 25 dB gain two-stage cascode LNA reported in [7] for 24 GHz applications and fabricated in a similar 0.18 µm SiGe technology, the LNA presented in this paper achieves similar gain at twice the frequency with comparable power consumption. To the best of the authors' knowledge, this is the first inductor-based circuit operating above 50 GHz.

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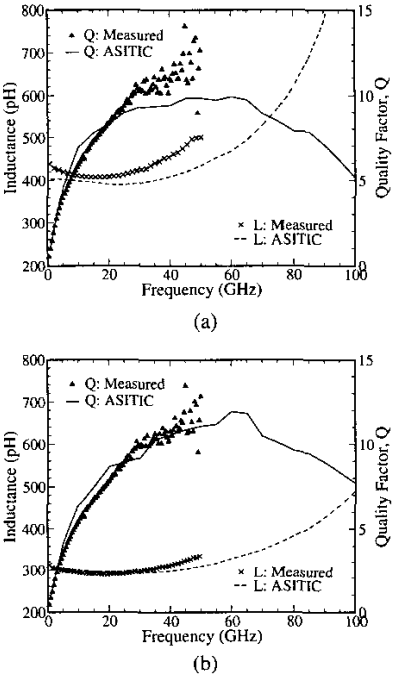

Fig. 6: Measured and modeled L_{EFF} and Q for (a) 440-pH and (b) for 330-pH inductors.

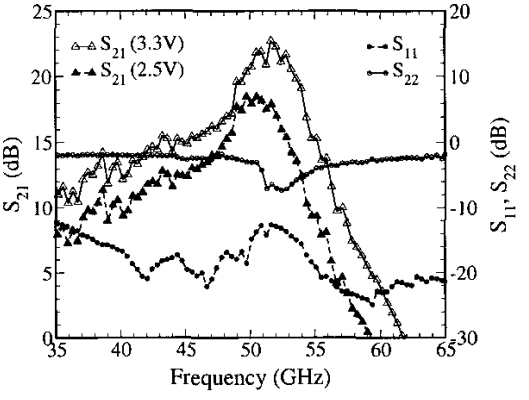

Fig. 7: LNA S-parameter measurements to 65 GHz.