A 3-V Fully Differential Distributed Limiting Driver for 40 Gb/s Optical Transmission Systems

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***Abstract*—A fully differential 40 Gb/s electroabsorption modulator driver is presented. Based on a distributed limiting architecture, the circuit can supply up to 3.0 V peak-to-peak per side in a 50 Ω load at data rates as high as 44 Gb/s. Both the input and output are internally matched to 50 Ω and exhibit return loss of better than 10 dB up to 50 GHz. Additional features of the driver include the use of a single -5.2 V supply, output swing control (1.7 to 3.0 V_{p-p} per side), DC output offset control (-0.15 V to -1.1 V) and pulse width control (30% to 70%).**

I. Introduction

High-performance low-cost physical (PHY) layer ICs are essential for the successful implementation of next generation 40 Gb/s optical communication systems. To realize an advantage over current wavelength-division-multiplexing (WDM) technology, these data rates must be achieved at the single-channel level. This prerequisite imposes significant technological demands on the front-end electro-optical interface (EOI) components.

Modulator drivers are a case in point. Not only must they operate at the high-data rates, but they must deliver high voltage levels as well. For conventional Mach-Zehnder (MZ) or electroabsorption (EA) devices to achieve adequate extinction ratios and thus reach, these modulators must be driven by signals having a swing of at least 3 to 5 V per side. For 40 Gb/s driver applications, the only devices that have so far demonstrated the requisite characteristics are GaAs PHEMTs and InP D-HBTs [1]. SiGe HBTs with f_T values up to 210 GHz have also been suggested – owing to their reproducibility, high yield and low cost [2]. However, there are significant concerns regarding their long term reliability because they exhibit breakdown at 2 V, operate at high current densities (>6 mA/μm^2) and suffer from significant self-heating at peak f_T bias [3,4].

To date, almost all of the reported 40 Gb/s modulator drivers are based on AlGaAs/InGaAs PHEMTs with gate lengths in the range of 0.1 to 0.2 μm [5,6]. In spite of its low f_T of approximately 100 GHz, this technology is by far the most attractive for this application. In addition to its high breakdown and f_{max} of approximately 200 GHz, it has proven yield and reliability, and there exists the capacity to produce 6" wafers. To overcome the f_T limitation, however, the driver must be based on a distributed amplifier topology with cascode gain stages. Not only does this extend the high-frequency performance of the device, but it ensures good broadband input/output impedance matching, while achieving the required output swing.

In this paper, the first full-featured differential 40Gb/s GaAs PHEMT modulator driver is presented. It consists of a lumped predriver circuit followed by a 5–stage distributed amplifier (DA). Compared to previously reported 40 Gb/s drivers, the latter section of the present design is based on a differential distributed limiting architecture, rather than the more conventional single-ended linear approach. As a result, the circuit can significantly exceed its small-signal bandwidth when operated under large-signal conditions. The limiting architecture also simplifies the inclusion of output swing control, DC output offset control, and pulse width control.

II. Device Modelling

Unlike conventional linear drivers, which are based on a relatively small number of device geometries operated in saturation, the differential limiting architecture calls for a non-linear device model that scales accurately over a wide range of gate widths and bias levels. In order to develop a realistic specification for the driver's performance, it should scale with temperature as well. To this end, a fully scalable non-linear model based on Agilent's *EEHEMT*™ was extracted. The nominal model values were derived from *S*–parameters and DC-IV curves over five different gate widths using conventional techniques for both the extrinsic and intrinsic circuit elements. By carefully adjusting the model parameters based on the five extractions, it is possible to obtain good agreement over all possible gate geometries.

As an example of the quality of the extracted model, Fig. 1 and Fig. 2 present measured versus simulated DC characteristics for a transistor having a 2×40 μm gate geometry. Fig. 1 shows an excellent level of agree-

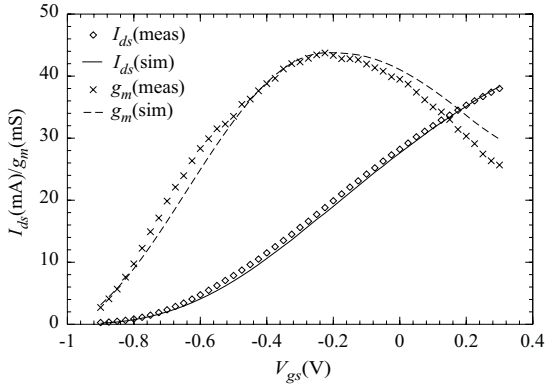

Fig. 1. Measured versus simulated drain current and transconductance for a 2×40 µm GaAs PHEMT.

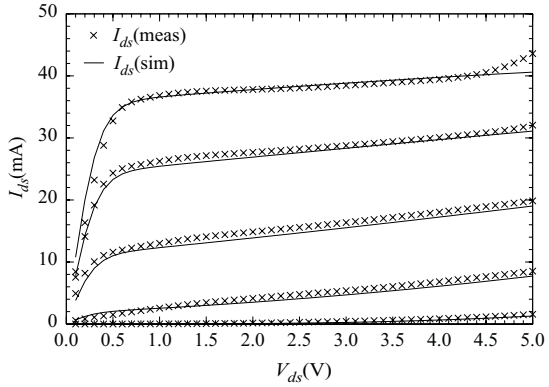

Fig. 2. Measured versus simulated DC-IV curves for a 2×40 µm GaAs PHEMT.

ment for V_{ds} = 2.5 V and V_{gs} from –1 V to +0.5 V. By scaling the model parameters with finger width and number of fingers, a similar fit can be obtained for all five gate geometries. Fig. 3 compares the measured and simulated f_T values, both as a function of gate width and temperature for V_{ds} = 1.5 V and V_{gs} = –0.1 V. Over the entire range, the measured and modelled results are no more than 10% apart. The temperature dependence in the model has been extracted empirically from device measurements made at 18 ºC and 100 ºC.

III. Circuit design

A block diagram of the QT3055 differential limiting driver is shown in Fig. 4. It includes three amplifier blocks, namely a lumped input amplifier, a lumped middle-stage amplifier and a distributed amplifier block, all of which operate from a single –5.2 V supply. The lumped amplifier blocks, as well as the distributed amplifier sections all consist of a double source follower stage with level-shifting diodes and a differential inverter. To enable the modulator to achieve its optimum performance, the driver also includes variable output amplitude (VOA), variable EA modulator offset (VEA) and adjustable pulse width control.

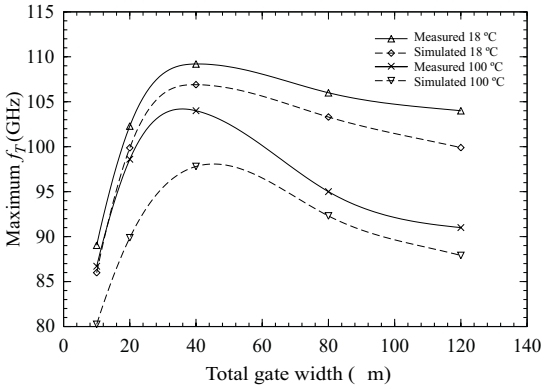

Fig. 3. Measured and simulated maximum f_T values versus total gate width and temperature.

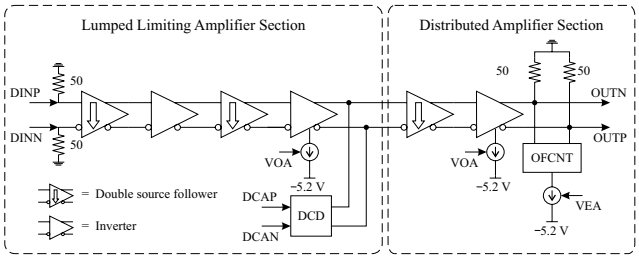

Fig. 4. Block diagram of the QT3055 driver.

The input stage features on-chip 50 Ω resistors to provide good input match and can be DC–coupled to a negative supply serializer-deserializer (SERDES) with current-mode logic (CML) outputs. For 0.5 V_{p-p}, this stage provides an output swing of 1.0 V_{p-p} per side. This signal is then amplified and limited to 1.4 V_{p-p} per side by the middle stage. To avoid any reflections with the DA, the middle limiter is loaded with resistors that are matched to the characteristic impedance of the DA's input transmission lines. A common-mode resistor is used to provide level shifting for the DA. This arrangement is shown in Fig. 5.

The middle stage inverter also includes elements for varying the output amplitude and pulse width. The former is achieved by adjusting the level supplied to the gate of the inverter current source via the VOA input. The pulse width control feature is implemented using a second differential pair connected in parallel with the middle-stage inverter. By default, the DCAP and DCAN pads are biased at the same level and sink equivalent amounts of current. Unbalancing them will introduce a DC offset between the middle-stage output

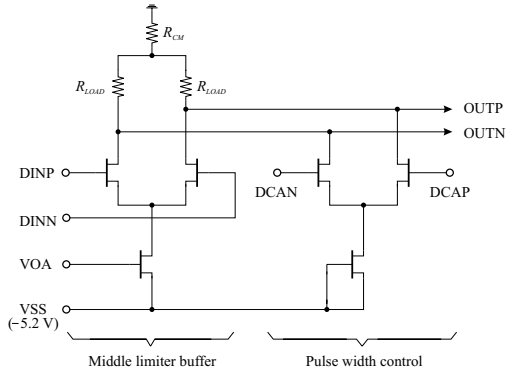

Fig. 5. Pulse width control function implementation.

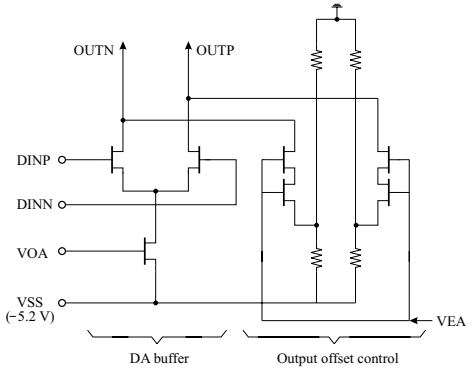

Fig. 7. Output offset control implementation.

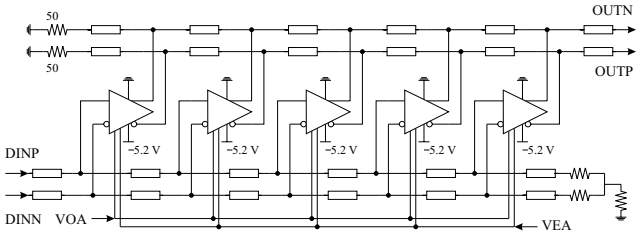

Fig. 6. Block diagram of the distributed amplifier.

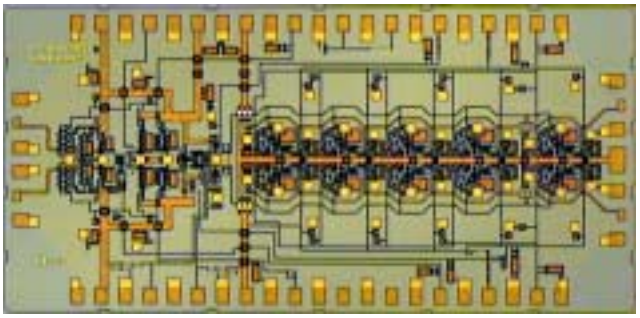

Fig. 8. Microphotograph of the EA driver IC.

signals and if the two signals are then hard-limited, the effect is to lengthen the high pulse in relation to the low pulse (or vice versa). This pulse width control scheme only works if the rise/fall time is commensurate with the pulse period and if it is applied between two limiting circuits (in this case the middle-stage and DA).

Although the 0.1-0.2 μm gate-length GaAs PHEMT has a gate-to-drain breakdown voltage of approximately –6 V, its f_T of 110 GHz and maximum available gain (MAG) of 13 dB at 50 GHz make it, at best, a marginal device for 40 Gb/s applications. For a DC–coupled circuit matched to 50 Ω and having an output swing of 3 $V_{p\text{-}p}$ per side, the required modulation current is 120 $mA_{p\text{-}p}$. While it may be possible to achieve this specification using a lumped output stage at 10 Gb/s [7], the RC time constant is simply too high for 40 Gb/s. The only alternative is to use a distributed amplifier configuration. Not only will this mitigate the size versus speed constraint, but it also has the added benefit of excellent output return loss. To extend the bandwidth further, the distributed amplifier block is designed to operate in a limiting mode. This allows the driver to accommodate data rates significantly beyond that predicted by its small-signal bandwidth. Such an approach has proved successful for 10 Gb/s drivers [8].

The block diagram of the 5–stage differential limiting distributed amplifier is shown in Fig. 6 with the adjustable current control and DC offset control elements of each stage shown in Fig. 7. The distributed amplifier has an overall gain of approximately 7 dB per side and limits the output swing to a maximum of 3 $V_{p\text{-}p}$ per side. The control elements are distributed in each stage of the DA so that the parasitic capacitance of the control transistors is absorbed by the output transmission lines. The DC offset control, which consists of a high-impedance cascoded differential pair, is designed to draw current through the DA loads and thus lower the DC output level. The amount is controlled by the level applied to the VEA pad. The adjustable bias current is controlled from the VOA pad and operates on the same principle as and in conjuction with the middle stage amplitude control feature. Both techniques have been applied previously for 10 Gb/s EA modulator drivers [9].

IV. Fabrication

The die, shown in Fig. 8, has dimensions of 1.95×3.99 mm^2 and was fabricated by Fujitsu Quantum Devices Limited using a 0.15 μm AlGaAs/InGaAs PHEMT process. The substrate height is 28 μm, and with an additional 32 μm of backside metal, the IC has a total thickness of 60 μm. The process features one metal

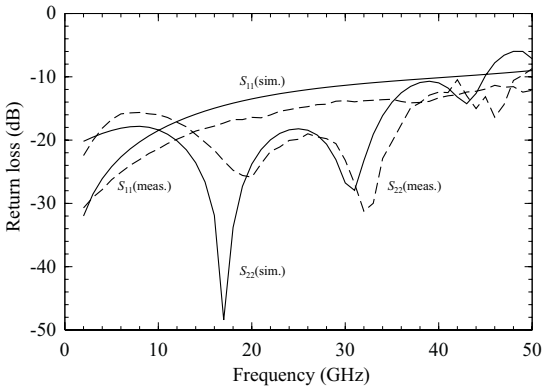

Fig. 9. Measured versus simulated return loss at 18° C.

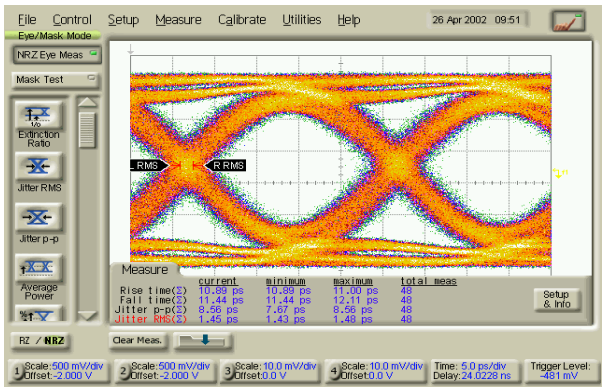

Fig. 10. Measured 40 Gb/s eye-diagram with 3.0 V swing.

layer, an underpass layer, through-wafer vias, interdigital PHEMTs and Schottky diodes, epitaxial resistors (110 Ω/□), and MIM capacitors. The circuit itself has 240 transistors and includes on-chip bias decoupling filters.

V. Measurement Results

The complete driver exhibits an overall gain of 16 dB per side when DC–coupled to an EA modulator and external 50 Ω load, and consumes 2.8 W. The measured and simulated single-ended input and output return loss are shown in Fig. 9. The results indicate excellent agreement with simulations and better than 10 dB return loss from 0 to 50 GHz. The die also exhibits 60 dB isolation up to 35 GHz. Fig. 10 presents the measured 40 Gb/s eye-diagrams for a 2^{31}–1 PRBS pattern. The output swing is 3.0 $V_{p\text{-}p}$ per side for a differential input signal having 0.8 $V_{p\text{-}p}$ per side. It should be noted that a good portion of the jitter evident in Fig. 10 can be traced to the input PRBS signal itself. The eye-closure is partly a result of inadequate bandwidth in the measurement setup, which is only 17 GHz (two 12", 2.4 mm cables and a pair of 65 GHz GGB probes). The output swing is controllable between 1.7 $V_{p\text{-}p}$ per side and 3.0 $V_{p\text{-}p}$ per side. A duty cycle variation of 30% to 70% is also achieved. The output DC offset can be varied between –0.15 and –1.1 V.

VI. Conclusion

A differential distributed limiting EA modulator driver IC using 0.15 µm GaAs PHEMTs has been designed and fabricated for optical transmission systems operating at data rates in the 39.8 to 42.8 Gb/s range. The IC achieves 3.0 $V_{p\text{-}p}$ per-side and features output swing control, DC offset control and pulse width control. It promises to be a valuable component for the implementation of 40 Gb/s optical communication systems.

Acknowledgment

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