6-kΩ, 43-Gb/s Differential Transimpedance-Limiting Amplifier with Auto-Zero Feedback and High Dynamic Range

Hai Tran[1], Florin Pera[2], Douglas S. McPherson[1], Dorin Viorel[1] and Sorin P. Voinigescu[3]

[1] Quake Technologies Inc., 80 Hines Rd. Ottawa, ON, K2K 2T8 Canada, htran@quaketech.com,
[2]Insyte Corporation, Ottawa, ON, K2K 3C9 Canada,
[3] ECE Dept., University of Toronto, 10 King's College Rd. Toronto, ON, M5S 3G4, Canada, sorinv@eecg.toronto.edu

Abstract

A high-gain, 43-Gb/s InP HBT Transimpedance-Limiting-Amplifier (TIALA) with 100-μA_{pp} sensitivity and 4.5-mA_{pp} input overload current is presented. The circuit also operates as a limiting amplifier with 40-dB differential gain, better than -15-dB input return loss, and a record-breaking sensitivity of 8 mV_{pp} at 43 Gb/s. It features a differential TIA stage with inductive noise suppression in the feedback network and consumes less than 450 mW from a single 3.3-V supply. The TIALA has 6-kΩ (76 dBΩ) differential transimpedance gain, 35-GHz bandwidth, and comprises the transimpedance and limiting gain functions, an auto-zero DC feedback circuit, signal level monitor and slicing level adjust functions. Other important features include 45-dB isolation and 800-mV_{pp} differential output.

INTRODUCTION

It has been demonstrated recently that it is possible to integrate the transimpedance and limiting amplifier (TIALA) functions on a single die [1]-[4]. In 40-Gb/s implementations such an amplifier has to cover a wide dynamic range from 100 μA_{pp} to 4 mA_{pp} [4]. In order to drive SERializer-DESerializer (SERDES) chips with sensitivity in the 50-mV_{pp} range, and to account for PCB and connector losses, a minimum output swing of at least 100 mV_{pp} per side must also be achieved, resulting in a minimum single-ended gain of 1 kΩ per side or 2 kΩ differential. This paper describes an InP HBT TIALA with functionality, sensitivity, gain, power dissipation and integration levels so far unparalleled in 40-Gb/s designs [4]-[6]. Since its input impedance is close to 50 Ω up to 50 GHz, it also doubles up as a low-noise limiting amplifier or voltage preamp. Such performance was made possible by a noise and bandwidth optimized differential TIA stage with resistive as well as inductive feedback, and by the choice of auto-zero DC feedback topology and on-chip isolation techniques.

CIRCUIT DESIGN ISSUES

The block diagram, shown in Fig.1, features a TIA stage with transimpedance gain T_z, a multi-stage limiting amplifier with voltage gain A_I, an auto-zero feedback amplifier with voltage gain A_o and dominant pole f_0, and an output buffer with adjustable swing and a gain of 2.

The schematic of the TIA stage is shown in Fig.2. Although the conventional use of this circuit is to drive the DINP input with the photo-diode and the AC-ground at the DINN input, it should be noted that it is also possible to employ it in a BPSK application where the inputs are driven by two out-of-phase photo-diodes. In the former case, a slicing level adjustment signal can be applied on the AC-grounded input pad.

Low-noise performance is the prime consideration in the TIA stage design. First, resistors rather than current sources are employed to bias the transistors in the feedback network. Secondly, the size and bias current density of the input transistors in the TIA stage are optimized in an effort

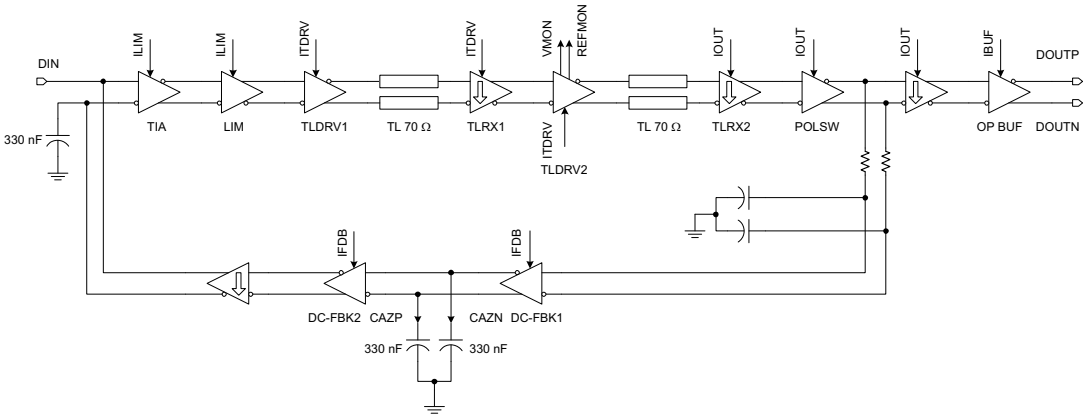

Figure 1. Block diagram of the TIALA with single photo-diode input. The unused TIA input is AC-coupled to ground in order to reduce noise. Emitter-follower stages are identified by a downward pointing arrow.

to reduce the input noise while ensuring that a small-signal bandwidth of at least 36 GHz is maintained over process and temperature corners. Thirdly, by placing the inductor L_f in the feedback network, the input-referred noise contribution of the feedback resistor R_f is reduced by a factor of $1+(\omega L_f/R_f)^2$ and the input match and small-signal bandwidth are improved by tuning out part of the PIN photo-diode and input capacitance. The bandwidth requirement also imposes an upper bound of about 300 Ω for the value of the feedback resistor. The simulated input equivalent noise, including the impact of the photo-diode's 60 fF capacitance and 15 Ω series resistance, and the 350 pH bond wire, is less than 27 $pA/\sqrt{(Hz)}$ up to 40 GHz.

The limiting amplifier block that follows the TIA stage consists of a Cherry-Hooper stage followed by a chain of emitter-follower and inverter stages. Inverters also act as drivers for two differential transmission line sections that are employed to ensure good isolation between the analog and digital portions of the die. The characteristic impedance of the transmission lines is 70 Ω per side, which represents a compromise between power dissipation and bandwidth. A signal level peak detector, which operates in linear mode for most of the input current range, is implemented in the second transmission line driver. The tail current in each inverter stage is set to the minimum possible value that still allows for the maximum data rate of 45 Gb/s to be achieved for all process, bias and temperature corners.

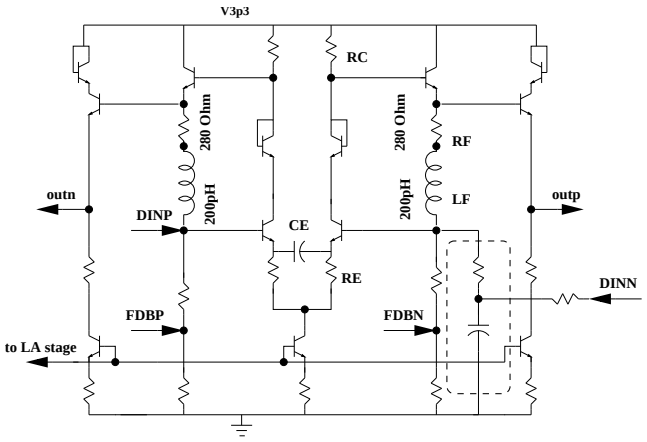

Figure 2. Differential TIA stage schematic.

The auto-zero DC feedback effectively cancels any systematic or input current-induced DC offset for the entire range of input photodetector currents. It must only be active below the low-frequency cutoff of a SONET system, which is typically 70 kHz. The high gain and noise contribution of the auto-zero feedback amplifier pose a serious design challenge. The feedback amplifier is implemented with two cascaded inverters and two emitter-follower stages. The latter ensure that the appropriate DC level is provided to the differential TIA stage. The gain of the DC feedback amplifier was derived from the requirement that, at the maximum input current level (2.5 mA average in this case), the differential DC output offset should be lower than +/-80 mV (10% of the differential output swing) in order to avoid significant duty cycle distortion. To increase its effectiveness, the output of the auto-zero feedback is injected differentially to the TIA stage at the nodes FDBP and FDBN. Its noise contribution to the input of the TIA is reduced by RC-filtering. Over 50 pF of on-chip and 330-nF external capacitors are needed to ensure stability, *1/f* noise suppression and the low-frequency bandwidth of 70 kHz.

FABRICATION

The circuit was fabricated in HRL Laboratories' InP SHBT process having an f_T and f_{max} of 160 GHz. The substrate thickness is 100 μm. The process features two metal layers, 50 Ω/sq thin film resistors and MIM capacitors. The microphotograph of the 1.0x1.8 mm^2 differential TIALA die is shown in Fig.3. The circuit draws 140 mA from a single 3.3 V supply and has 200 HBTs, two inductors, and 40 MIM capacitors which are employed for bias de-coupling and low-pass filtering. All transmission lines are implemented as grounded CPWs.

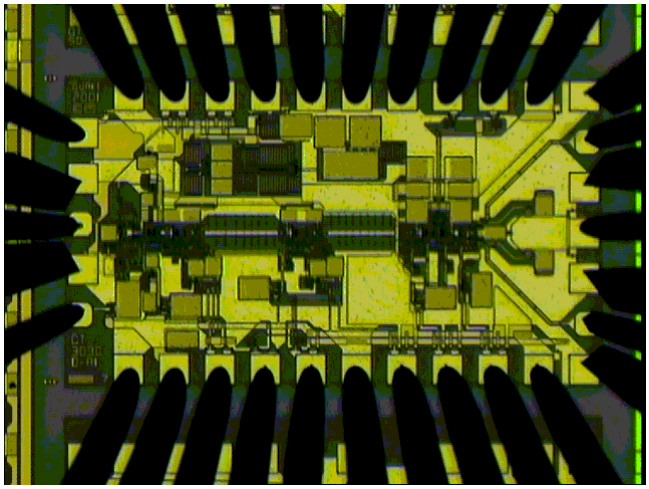

Figure 3. Layout of the TIALA with HF wafer probes.

MEASUREMENT RESULTS

The input current range and output offset were first verified by sweeping the input with a DC current up to 3 mA, corresponding to a maximum ac current of 6 mA_{pp}. As illustrated in Fig.4, the measured differential output offset remains less than 40 mV.

Fig.5 presents the on-wafer measured gain, input and output reflection coefficients, as well as the isolation of the differential TIALA. S_{11}, S_{22} and S_{12} are lower than -15, -10 dB, and -45 dB, respectively, up to 50 GHz. The small-signal (-65 dBm) and large-signal (-25 dBm) S_{21} are also plotted in order to illustrate the limiting action on the 3-dB bandwidth. The small-signal 3-dB bandwidth of the TIALA is larger than 35 GHz while the small-signal power gain exceeds 34 dB per side. The corresponding

small-signal transimpedance gain is 70 dBΩ per side or 76 dBΩ differential. The differential Z_{21} vs. frequency characteristics of the TIA stage were measured on a separate test structure and are also shown in Fig.5. Its bandwidth is 38 GHz and it features intentional gain peaking to compensate for the input capacitance of the limiting amplifier and for the frequency-dependent loss in the two transmission line sections.

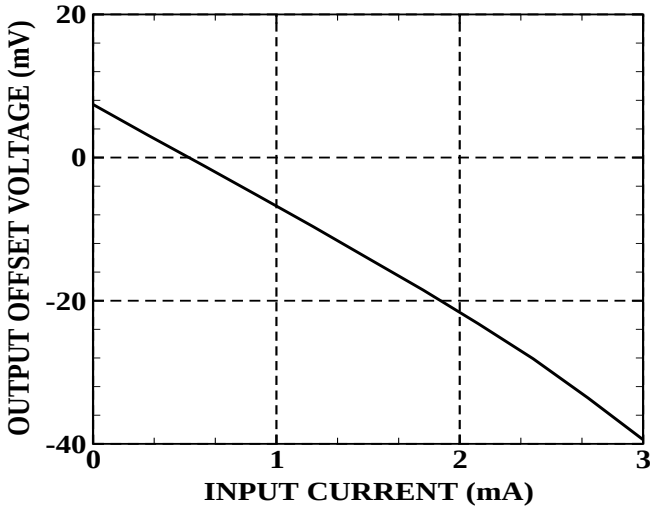

Figure 4. Measured DC output offset as a function of DC input current.

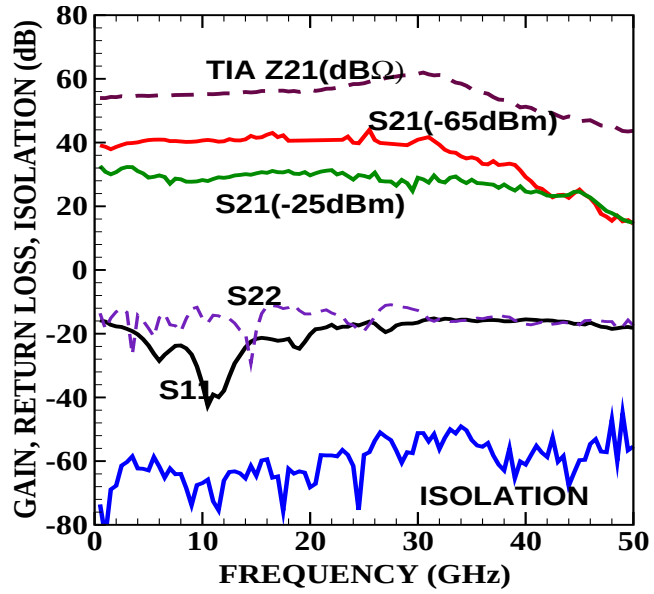

Figure 5. On-wafer input/output return loss, isolation, small-signal (with -65-dBm input signal) and large-signal (-25-dBm input signal) differential TIALA power gain. The differential Z_{21} measured for a test structure consisting of the TIA stage alone is also shown.

The Anritsu MP1801A 43.5-Gb/s MUX and BERT and the Agilent 86100A DCA with 85484A 50-GHz sampling heads were used for on-wafer eye diagram and electrical sensitivity measurements, shown in Fig.6. The sensitivity is 90 μA_{pp} and 110 μA_{pp} at 40 Gb/s and 43 Gb/s, respectively, when using 2^{31}-1 pattern and accounting for the 65-Ω input impedance. The corresponding signal level monitor output is shown in Fig.7. The jitter resolution of the setup, including the effects of the probes and two 6" cables, is limited to 1 ps_{rms}. Figs. 8 and 9 show the error-free differential output eye diagrams at 43 Gb/s with 2^{31}-1 pattern for input currents of 4.5 mA_{pp} and 250 μA_{pp}, respectively. In both cases the output is limited to 360mV_{pp} per side.

The circuit was next mounted as a limiting amplifier in a customer module and its electrical sensitivity was found to be better than 8 mVpp, as illustrated in Fig. 10. The measured jitter of the input and output eye diagrams is 994 fs_{rms} and 1.11 ps_{rms}, respectively, with 0.5 ps_{rms} due to the TIALA. This sensitivity value represents a factor of two improvement over the best sensitivity reported for 40-Gb/s limiting amplifiers or SERDES. It recommends the TIA stage as the lowest noise circuit topology for high data rate voltage pre-amplifiers.

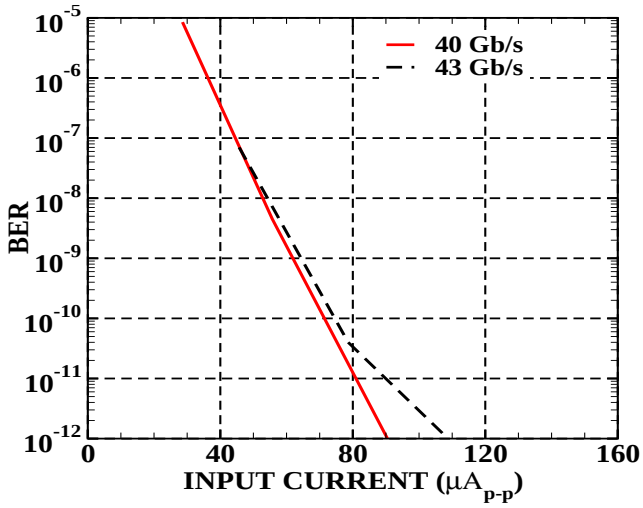

Figure 6. Measured sensitivity with a 2^{31}-1 PRBS.

CONCLUSIONS

A high-gain, high-dynamic range 43 Gb/s transimpedance-limiting amplifier has been fabricated in InP/InGaAs HBT technology. The TIALA exhibits 6-kΩ gain, 100-μA_{pp} sensitivity, 4.6-mA_{pp} input overload current and high levels of functional integration while consuming less than 450 mW from a 3.3-V supply. When measured as a 43-Gb/s limiting amplifier with a 2^{23}-1 PRBS, the sensitivity was 8 mV_{pp}, a factor of two improvement over the best data reported to date.

ACKNOWLEDGEMENTS

The authors thank Dr. M. Tazlauanu and S. Szilagyi for transistor, inductor and transmission line models. Discussions on InP HBT technology with Dr. M. Sokolich and Dr. M. Delaney of HRL Labs are greatly appreciated.

REFERENCES

[1] Rein, H-M., "Si and SiGe Bipolar IC's for 10 to 40 Gb/s Optical-Fiber TDM Links", *IJHSE. Syst.*, vol.9, pp.1-37. (1998).

[2] Mullrich, J., et al., "40Gb/s transimpedance amplifier in SiGe bipolar technology for the receiver in optical-fiber TDM links", *Electron. Lett.*, 34, pp-452-453, (1998).

[3] Voinigescu, S.P., et al., "Circuits and Technologies for Highly Integrated Optical Networking IC's at 10 Gb/s to 40 Gb/s," *Proc.IEEE CICC*, pp. 331-338, (2001).

[4] Wu, C. Q., et al., "40 GHz Transimpedance Amplifier with Differential Outputs using InP/InGaAs Heterojunction Bipolar Transistors", *GaAs IC Symposium, Technical Digest*, pp.63-66, (2002).

[5] Caruth, D., et al., "A 40 Gb/s Integrated Differential PIN+TIA with DC Offset Control using InP SHBT Technology," *GaAs IC Symposium, Technical Digest*, pp.59-62, (2002).

[6] Kobayashi, K.W., "An InP HBT Common-Base Amplifier with Tunable Transimpedance for 40 Gb/s Applications," *GaAs IC Symposium, Technical Digest*, pp.155-158, (2002).

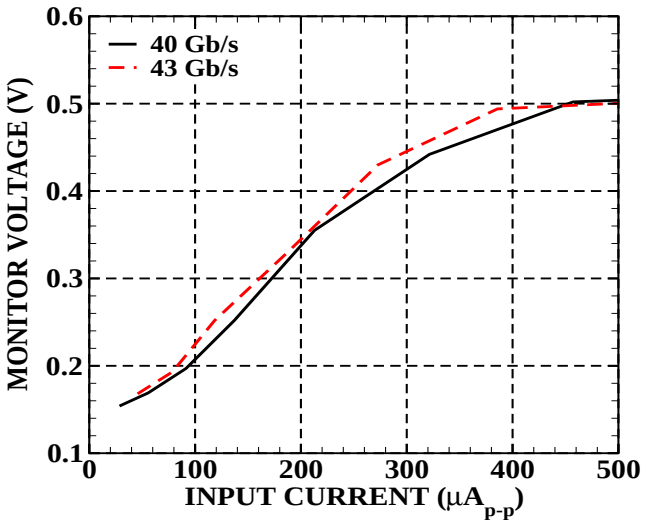

Figure 7. Measured signal level monitor output as a function of the 2^{31}-1 PRBS signal level.

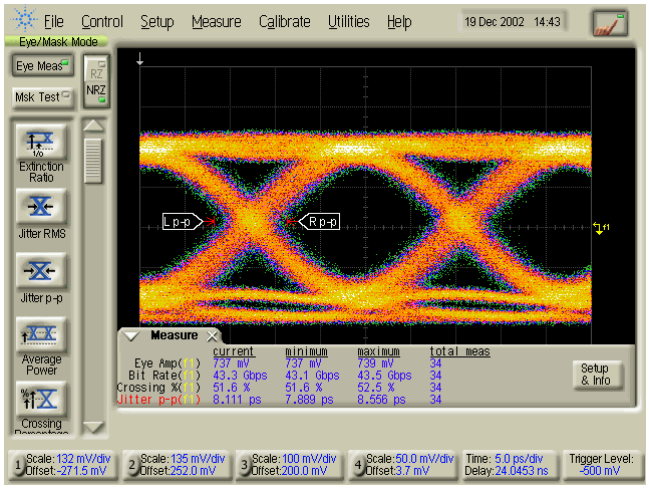

Figure 8. On-wafer measured 43-Gb/s, 2^{31}-1 differential output eye-diagram with 4.5-mA_{pp} input.

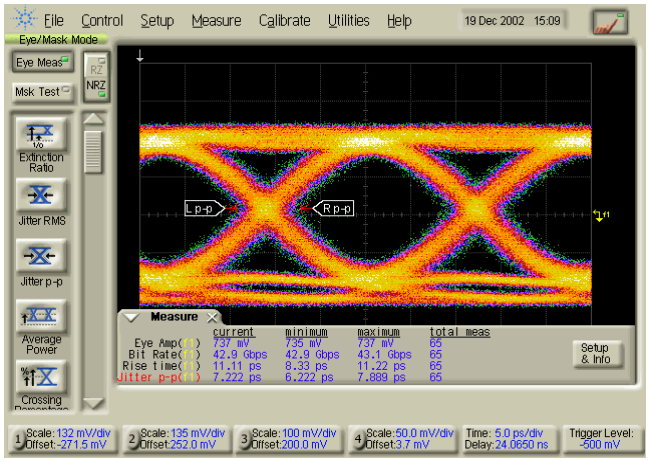

Figure 9. On-wafer measured 43-Gb/s, 2^{31}-1 differential output eye-diagram with 250-μA_{pp} input.

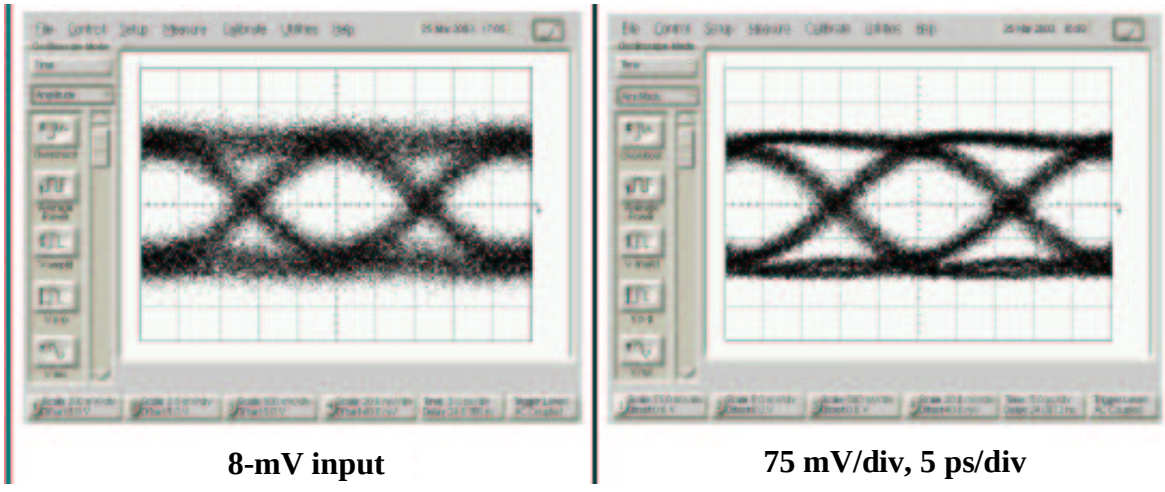

Figure 8. Measured 43-Gb/s, 2^{23}-1 input (8 mV_{pp}) and output (320 mV_{pp}) single-ended eye-diagram of the TIALA mounted in a customer module as a limiting amplifier.