65-GHz Receiver in SiGe BiCMOS Using Monolithic Inductors and Transformers

Michael Gordon,

Terry Yao,

Sorin P. Voinigescu

University of Toronto

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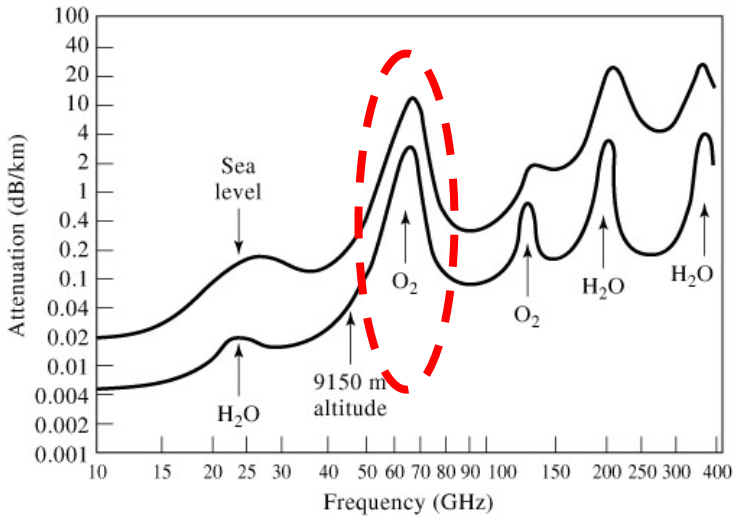
Outline

- Motivation
- 65-GHz Receiver Overview
- Receiver Design
  - Active and passive components
  - Circuit building blocks
  - Full 65-GHz receiver integration
- Summary

Work Motivation

- 7 GHz of unlicensed spectrum (57-64 GHz)
  - High data rate 60-GHz WLAN (500Mb/s to 2Gb/s)
  - mm-wave sensors for medical / security applications
- Design advantages over 5-10 GHz RF
  - Simpler radio architecture - A lot of bandwidth available
  - Smaller devices → higher integration → smaller die area

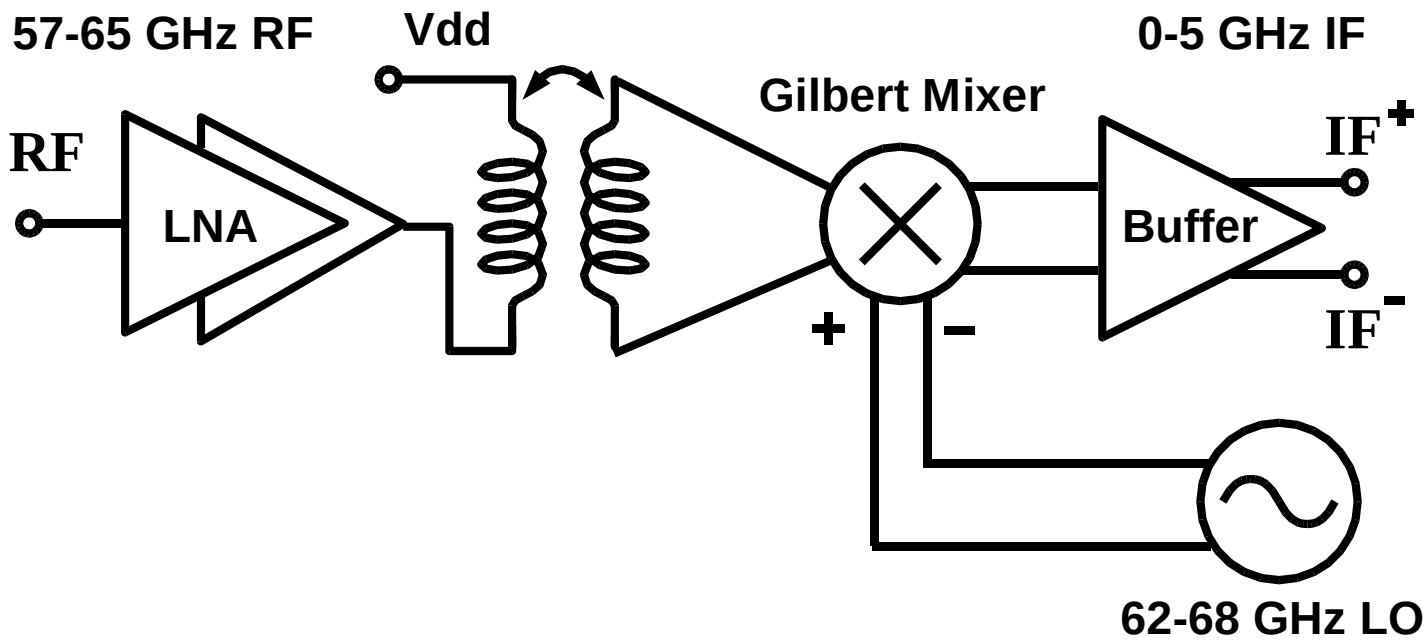


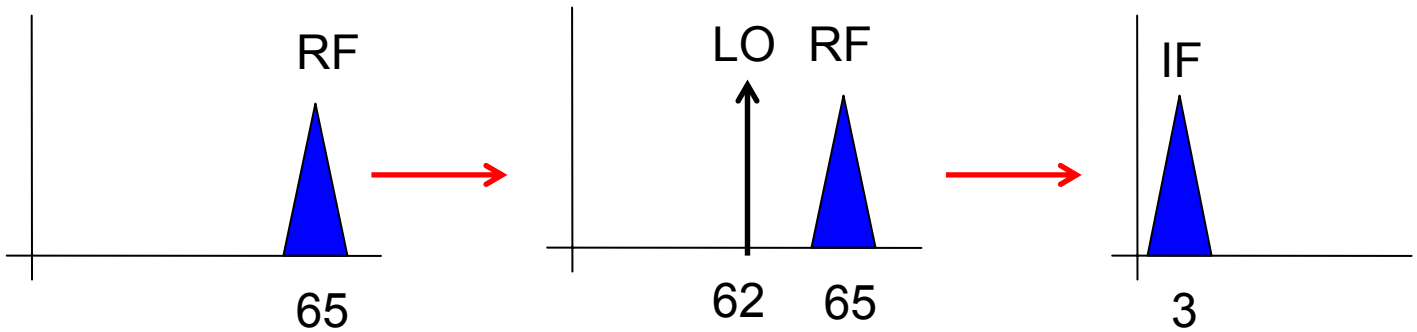
Atmospheric attenuation due to oxygen

Research Goals

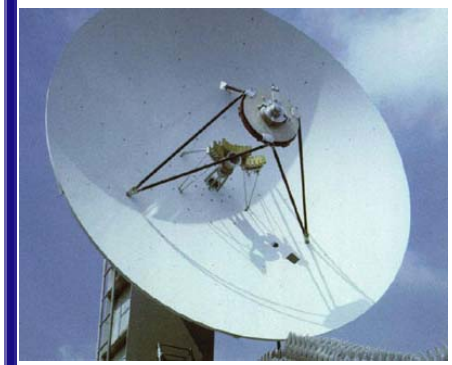
- Demonstrate a highly integrated 65-GHz receiver in silicon including the VCO
- Develop and apply low-noise design techniques across different mm-wave receiver building blocks
- Validate the use of monolithic inductors in mm-wave circuits

65-GHz Receiver Overview





Link Budget Estimation



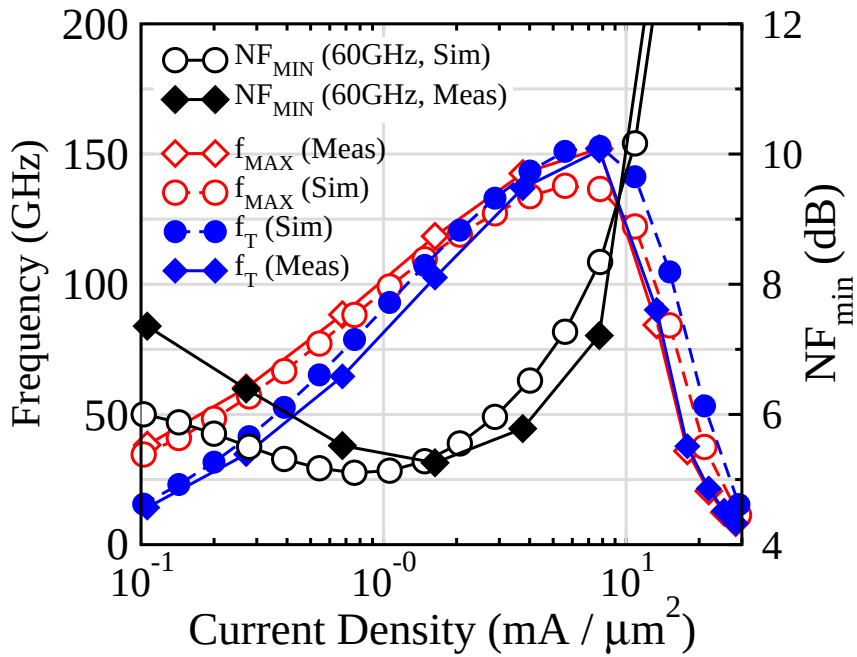
$$Sensitivity_{dBm} = 10\log kTB_{RF} + NF + SNR + 30$$

- Sensitivity for 1 GHz BW, SNR=10 dB, NF=10 dB
  - -52.3 dBm
- For a dynamic range of 30 dB need an input compression point of at least **-22 dBm**!
- Must optimize both **linearity** and **noise** in receiver design

Technology Characterization: Active Devices

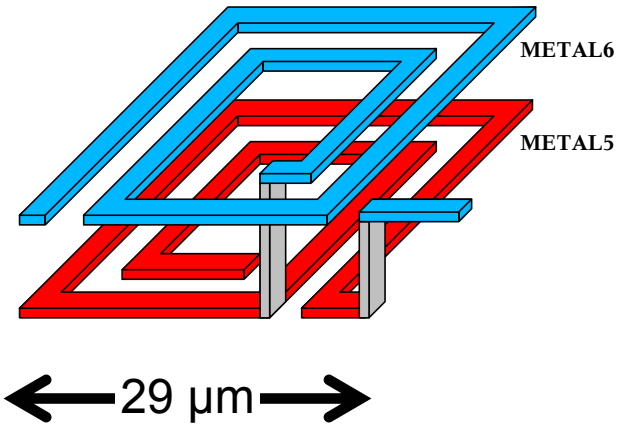
- Production Jazz Semiconductor SBC18HX SiGe BiCMOS process
- NF_{min} extracted from measured Y-Parameters
  [S. P. Voinigescu et al, JSSC Sep '97]
  [K. H. Yau et al, SiRF 2006]
  - Valid below $f_T/2$

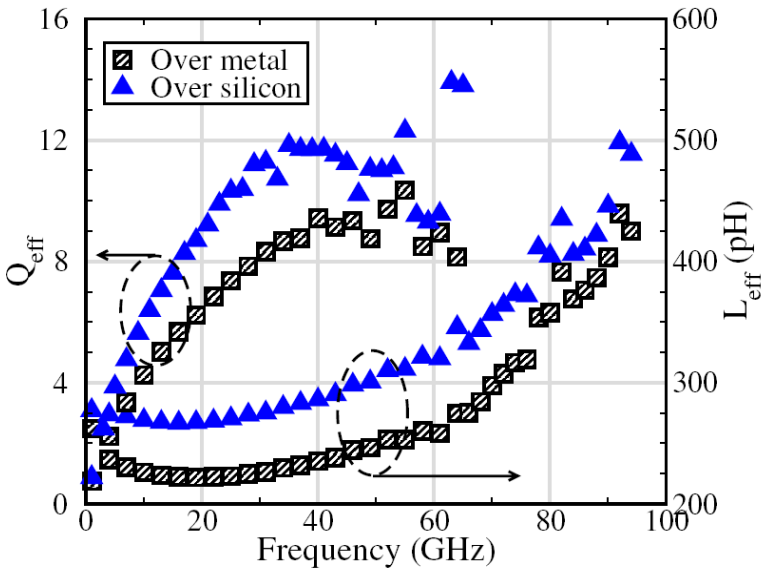
- 5.24µm x 0.2µm HBT
- f_T, f_{MAX} = 150 GHz
- Good agreement with simulator
- Validates HBT model



Technology Characterization: Passive Devices 1

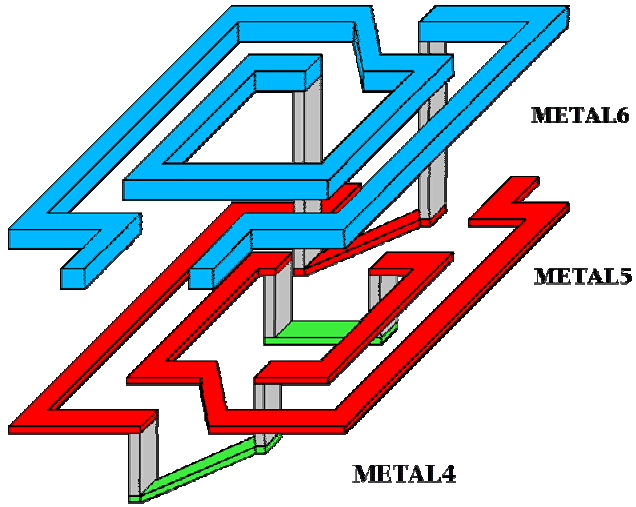
- Stacked multi-metal spiral inductors
- Occupy smaller area compared to CPW or μ-strip t-lines
- Tested unconventional "inductor-over-metal" structure

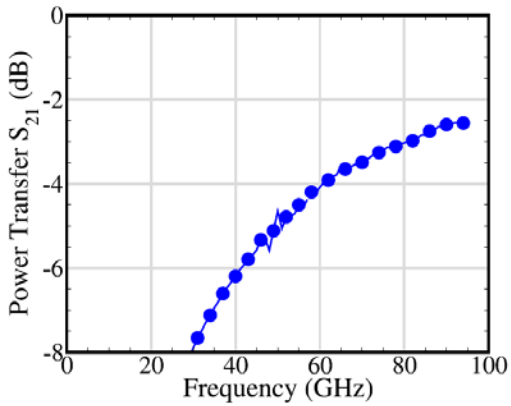


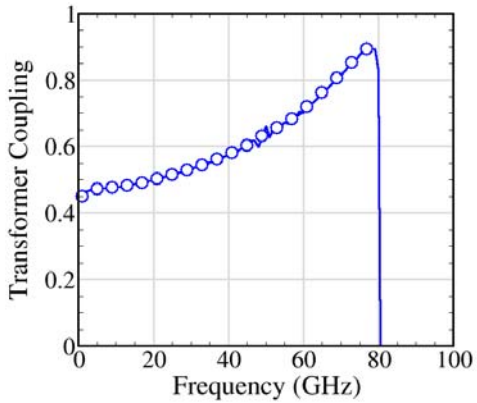


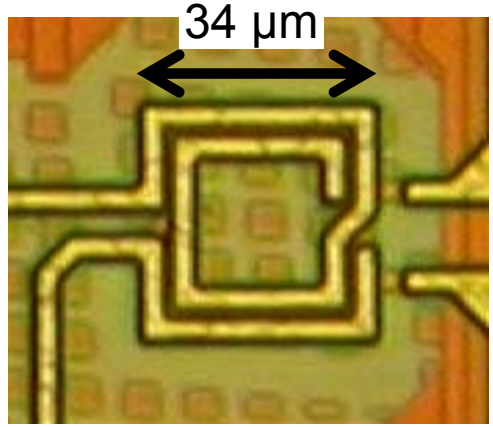
Technology Characterization: Passive Devices 2

- 1:1 vertically stacked transformer
- Implemented in adjacent metal layers for tighter coupling
- Compact and low-loss
- Operates up to 80 GHz





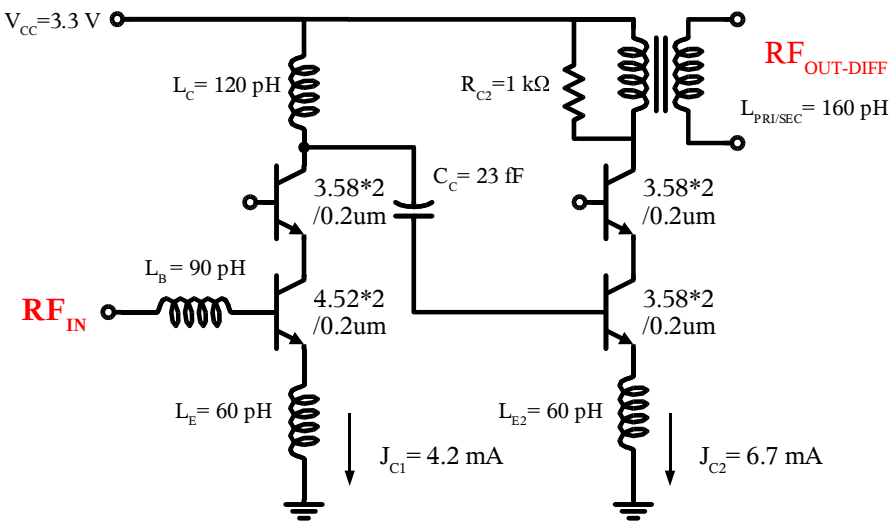


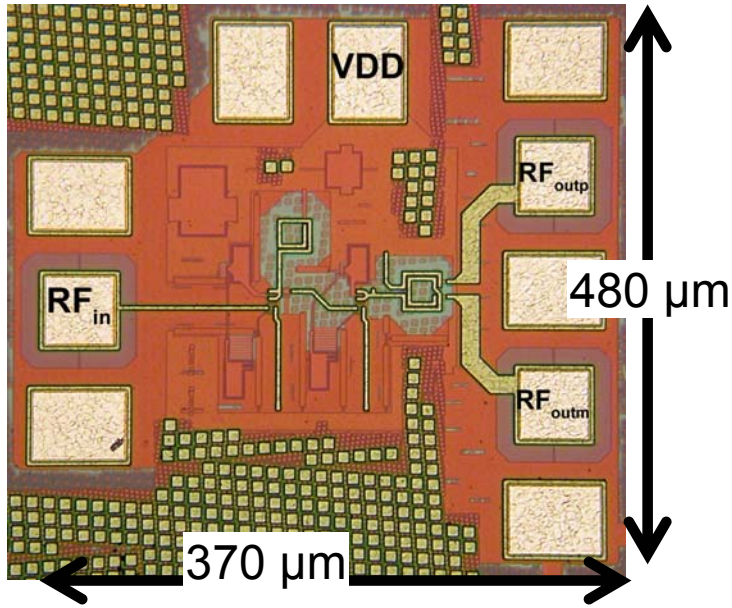


Single-ended measurements

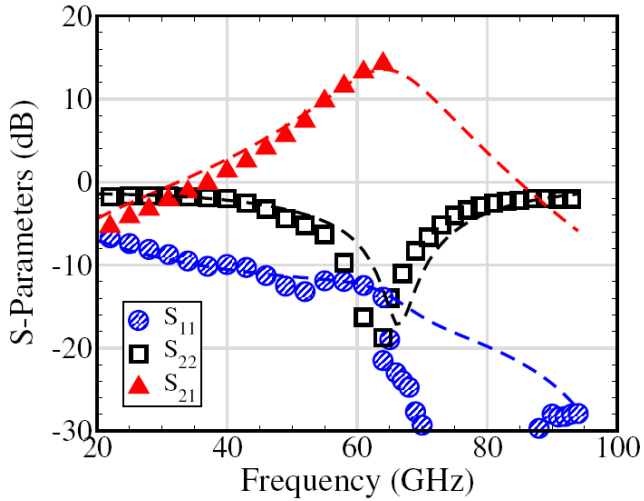
240 pH each winding

Building Blocks: 65-GHz LNA

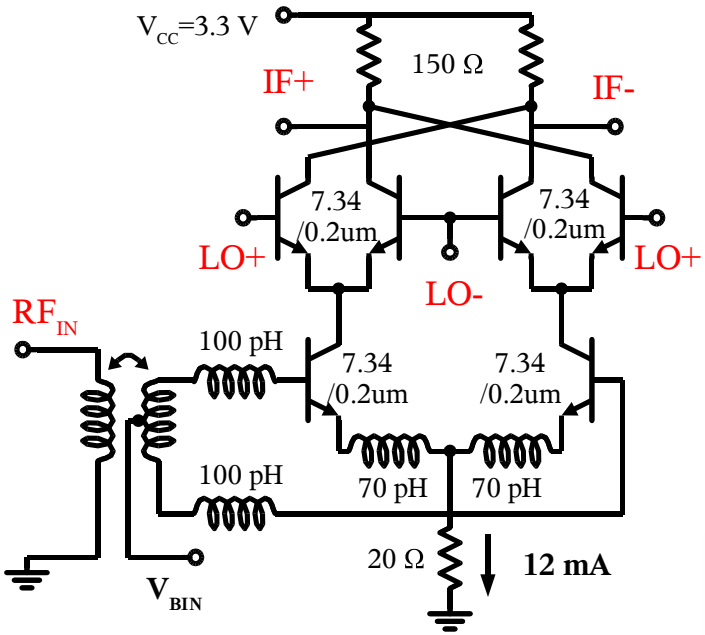




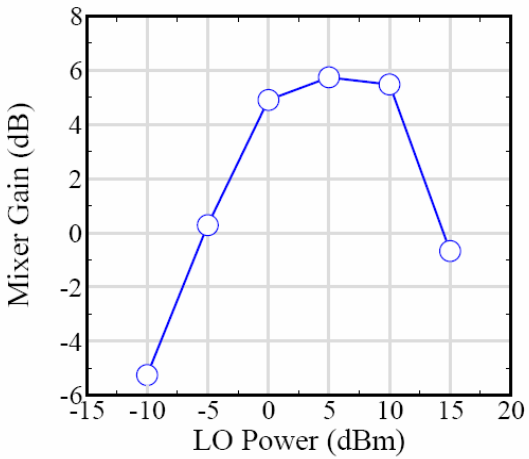
- Designed for concurrent power and noise matching [M. Gordon, ESSCIRC 04]
- 2 variants of 65-GHz LNA:
  - Inductor matched output network
  - Transformer matched output network
- Simulated NF = 10.5 dB
- Input P_{1dB} = -12.8 dBm
- Consumes 45 mW from 3.3V

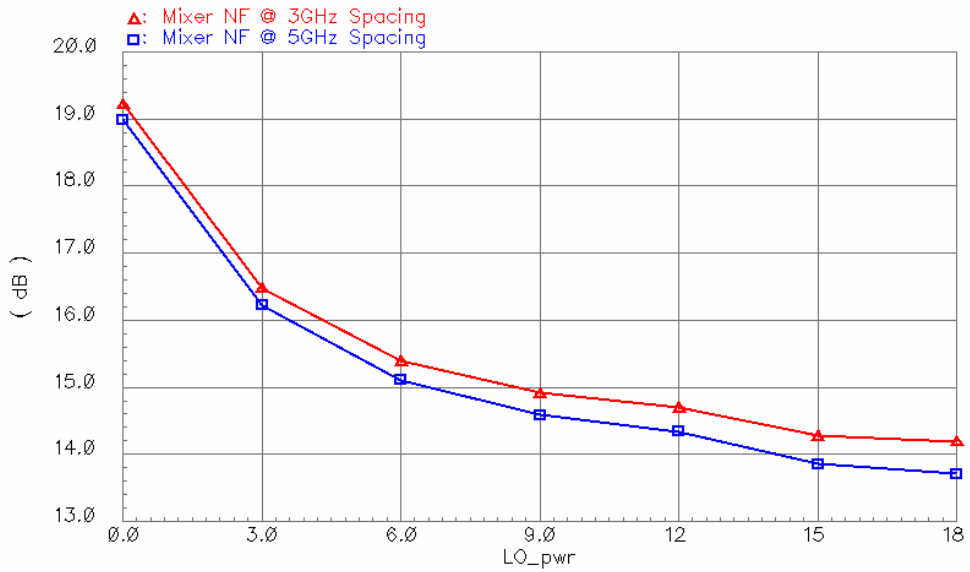


Building Blocks: Mixer

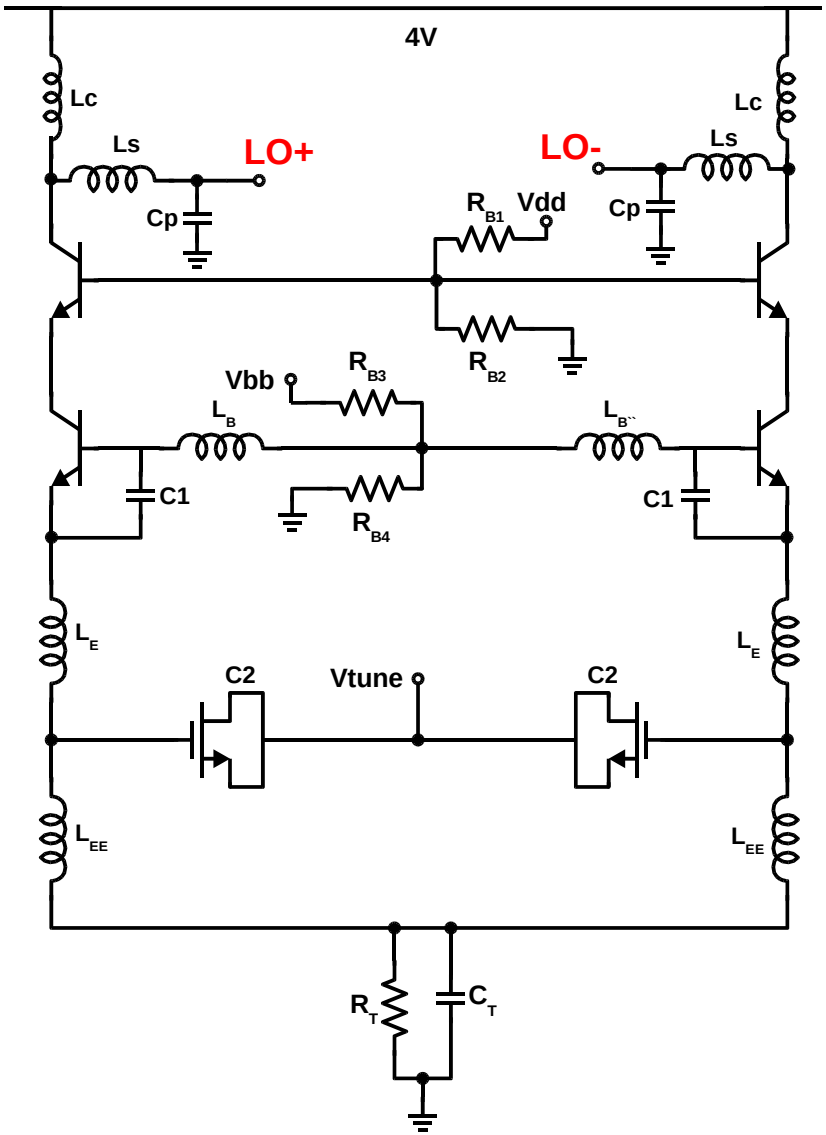


- Gilbert Cell Topology
- Simulated:
  - Conversion gain of 6 dB
  - NF ~ 16 dB
  - Differential Input P_{1dB} = -1 dBm
- Requires LO > +3 dBm



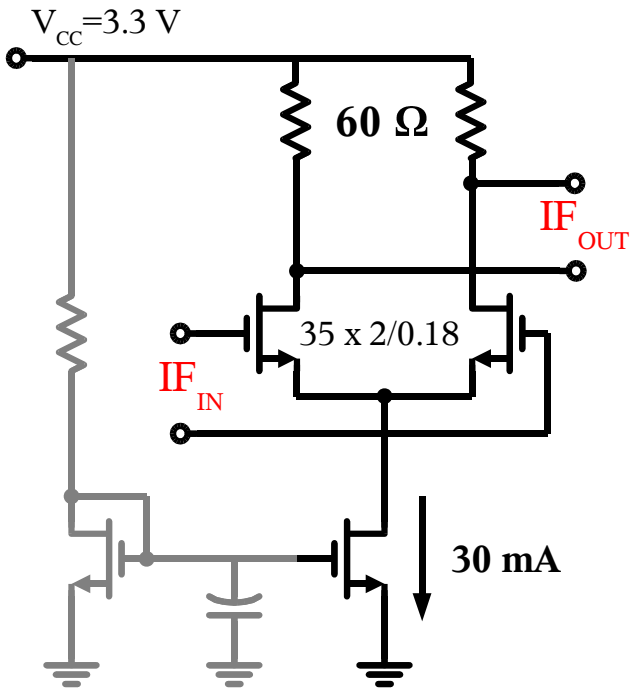


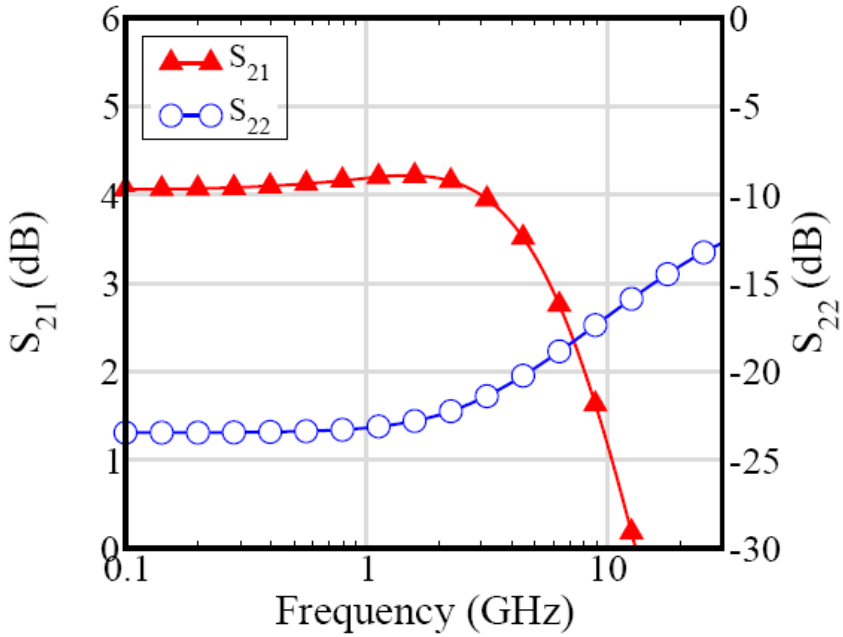
Building Blocks: VCO



- Differential Colpitts Topology
  - Based on 59 GHz VCO from [C. Lee, CSICS 2004]
  - LC-varactor tank
  - Need high output power and low phase noise for mixer
  - Requires 4V supply (60 mA tail)
- Differential LO power +4 dBm
- PN_{1MHz} = -104 dBc / Hz
- Frequency Range 62-68 GHz
- EF Buffer to isolate from mixer

Building Blocks: IF Amplifier

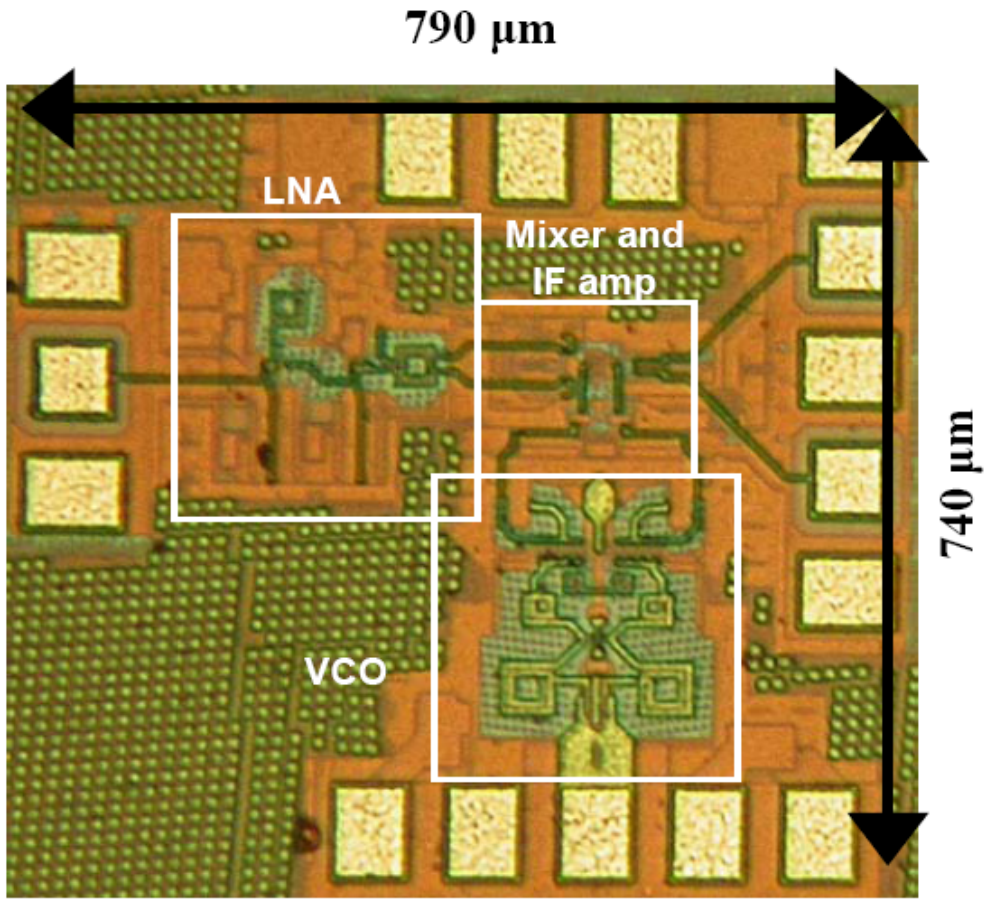




- MOS differential pair biased at 0.2 mA/μm for maximum linearity
- 3-dB bandwidth is 10 GHz
- Differential Input P_{1dB} = +1.7 dBm
- The limiting linearity block in the receiver chain

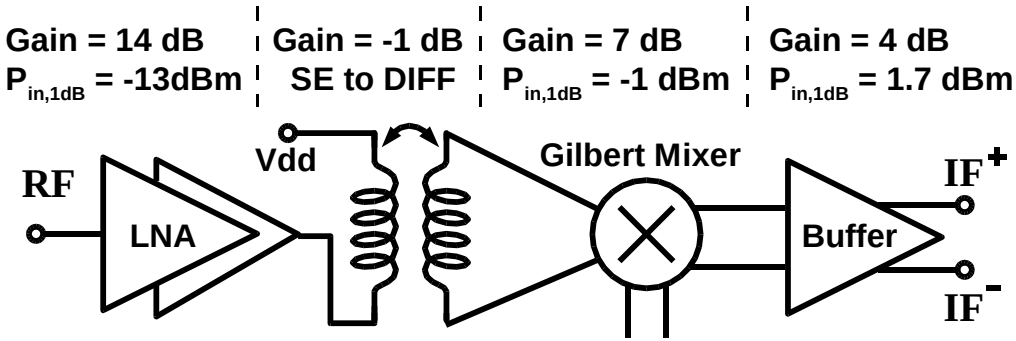
Fully Integrated Receiver 1

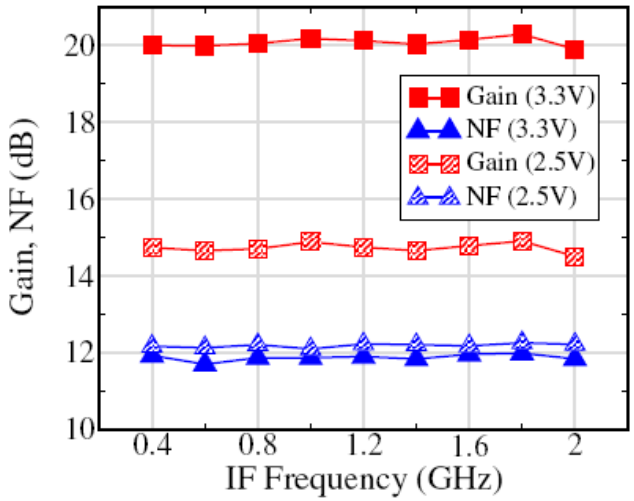
- First 65-GHz receiver in silicon to integrate VCO
- Total power is 540 mW
  - LNA + Mixer = 80 mW
  - VCO + Buffer = 360 mW
  - IF Amp = 100 mW
- Core is 550µm x 440µm
  - Compact passives
  - Tight layout important to reduce parasitics at 65 GHz

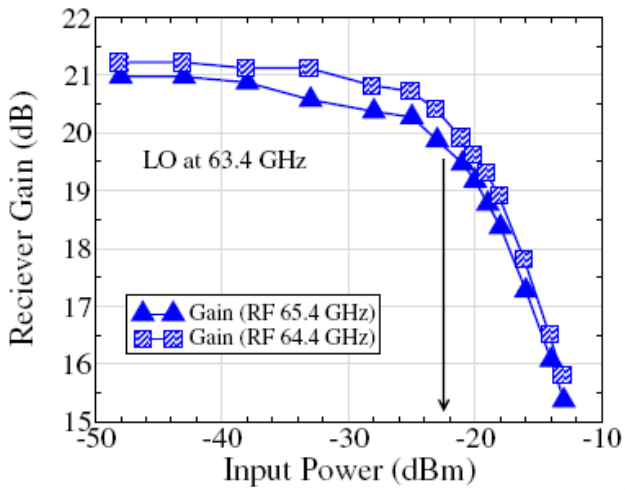


Fully Integrated Receiver 2

- Nominal operation
  - Gain = 24 dB differential
  - Input P_{1dB} = -22 dBm
  - NF = 12 dB (11.5 dB simulated)
  - Dynamic range = 28 dB
- Rx can operate from 2.5V (VCO still at 4V)
  - 450 mW
  - Gain = 15 dB, NF = 12.2 dB







State of the Art Comparison

Technology (fT / fMAX)	0.12µm SiGe (200/290 GHz)	0.13µm CMOS (70/135 GHz)	0.13µm CMOS (80/- GHz)	0.18µm SiGe Bipolar (150/150 GHz)	
Integration Level	LNA, mixer, branch-line coupler, tripler	LNA	LNA, µ-strip balun, quadrature mixer	LNA	LNA, mixer, VCO, transformer balun, IF amplifier
Freq.	61.5 GHz	60 GHz	60 GHz	65 GHz	65 GHz
Gain	16 dB	12 dB	28 dB Voltage gain	14 dB	24 dB
NF	14.8 dB	8.8 dB	12.5 dB (extracted)	10.5 dB (sim)	12 dB
P_{1dB}	-17 dBm	-9 dBm	-22.5 dBm	-12.8 dBm	-22 dBm
DC Power	300 mW (2.7V)	54 mW (1.5V)	9 mW (1.2V)	36 mW (2.5V)	540 mW (3.3V, 4V for VCO)
Die area	1.9 x 1.65 mm	1.3 x 1.0 mm	0.3 x 0.4 mm (no pads)	0.37 x 0.46 mm	0.79 x 0.74 mm
Reference	Floyd et al, JSSCC Jan '05	Doan et al, JSSCC Jan '05	B. Razavi, ISSCC 05	**This work**	

Summary

- First 65-GHz silicon receiver to integrate a VCO
- Excellent agreement between simulated and measured results
  - Diligent layout → Small parasitics → matched performance
  - Current silicon technology is mature enough for mm-wave radio SoCs
- Advancement of monolithic inductor research
  - Demonstrated stacked transformer in a tuned circuit
  - New proposed “inductor-over-metal” structures

Acknowledgments

- Jazz Semiconductor for fabrication
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