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# Direct Extraction Methodology for Geometry-Scalable RF-CMOS Models

Sorin P. Voinigescu[1], Mihai Tazlauanu[2], P.C. Ho[3], and M.T.Yang[3]

1) ECE Department, University of Toronto, 10 King's College Rd. Toronto, ON, M5S 3G4, Canada,
2) Quake Technologies Inc., 80 Hines Rd. Ottawa, ON, K2K 2T8 Canada,
3) TSMC, No.9, Creation Rd. 1, Science-based Industrial Park, Hsin-Chu, Taiwan, R.O.C.

*Abstract*-A new method to directly extract the MOSFET small-signal parameters - including non-quasi-static effects - from *Z* and *Y* parameter measurements is presented. This technique is employed to generate a scalable BSIM3v3 model valid for standard, low and high-threshold p- and n-channel MOSFETs at frequencies up to *50 GHz*. The model accurately captures cutoff frequency degradation for unit gate finger widths below 1 μ m and was employed to verify the measured jitter of a 10-Gb/s MOS-CML output driver.

## INTRODUCTION

As the minimum feature size of MOSFETs approaches 100 nm, the gate-source and gate-drain overlap and fringing capacitances become comparable to the internal gate capacitance and contribute significantly to the degradation of RF and high-speed device performance. The degradation of logic performance is particularly severe because most digital cells rely on minimum size transistors with W/L ratios lower than 5, where gate-bulk overlap capacitance further reduces speed and inevitably leads to increased power dissipation.

Following a trend set by bipolar model extraction techniques, it has been recognized recently [1]-[2] that fitting, or a combination of fitting and direct extraction of capacitances and substrate network from *S* parameters measured on typical size transistors is a crucial step towards improving MOSFET models for RF and high-speed applications. Even in that case, unless the source, gate, and drain series resistance are adequately de-embedded at high frequency, the extracted device capacitance values can be underestimated by as much as 20%.

This paper extends the direct extraction approach [1] to avoid these pitfalls and proves that it is possible to construct a *scalable, multiple-threshold, non-quasi-static* NQS RF equivalent circuit (Fig. 1) directly from measured *Z* and *Y* parameters.

## SINGLE-TRANSISTOR EXTRACTION TECHNIQUE

The extraction methodology is based on the small signal circuit of Fig.1. NQS effects are represented by the channel source and drain resistance $R_i$ and $R_{gd}$, respectively, and by the transconductance delay $\tau_g$. First, a two-step series-shunt de-embedding technique is employed to remove the 15-fF pad capacitance and series interconnect inductance (30-50 pH and resistance (0.5 -1 Ω). As shown in Fig. 2, the pads behave as ideal, lossless capacitors up to 50 GHz. This is important in minimizing de-embedding errors and makes it possible to accurately extract gate capacitance values in the fF-range. Second, with the MOSFET biased in strong inversion $V_{GS}$ = *0.8 V* and $V_{DS}$ = *0.01 V*, the extrinsic resistive elements $R_s$, $R_g$, and $R_d$ are extracted from the high-frequency limit of the measured $Re\{Z_{12}\}$, $Re\{Z_{11}-Z_{12}\}$, and $Re\{Z_{22}-Z_{12}\}$ data, respectively. The *Y* matrix of the intrinsic equivalent circuit (dashed box in Fig. 1) is then obtained by *Z*-to-*Y* matrix conversion after de-embedding $R_s$, $R_g$ and $R_d$ from the measured *Z* matrix. Next, the majority of the intrinsic circuit parameters are extracted directly, at each bias point, as illustrated in Figs. 3-6, using the eqns. (1)-(4) below.

$$R_i=\Re\{(Y_{11}+Y_{12})^{-1}\} \qquad R_{gd}=\Re\{-Y_{12}^{-1}\} \quad (1)$$

$$C_{gs}=\frac{\partial}{\partial\omega}(\Im\{(Y_{11}+Y_{12})^{-1}\})^{-1} C_{gd}=\frac{\partial}{\partial\omega}(\Im\{-Y_{12}^{-1}\})^{-1} \quad (2)$$

$$g_m=\left|\frac{Y_{21}-Y_{12}}{Y_{11}+Y_{12}}\right|\times\left[\Im\left\{\frac{1}{Y_{11}+Y_{12}}\right\}\right]^{-1} \quad (3)$$

$$\tau_g=-\frac{\partial}{\partial\omega}\left[phase\left\{\frac{Y_{21}-Y_{12}}{Y_{11}+Y_{12}}\right\}\right] \quad (4)$$

The measurement accuracy and the validity of the NQS equivalent circuit are first confirmed by the fact that the values of $C_{gs}$, $C_{gd}$, $g_m$, $R_{gd}$ calculated at each frequency are practically constant over a large frequency range up to *50 GHz*. $\tau_g$ is obtained from the slope of the measured phase curves (4), as shown in Fig. 4. The output conductance and the total output capacitance are derived from the sub *1-GHz* range of

$$g_{ds}=\Re\{Y_{22}+Y_{12}\};\; C_{ds}+C_{db}=\frac{\partial}{\partial\omega}(\Im\{Y_{22}+Y_{12}\}) \quad (5)$$

Finally, processing the measured data above *40 GHz* and removing $g_{ds}$, the substrate network parameters $R_{db}$, $C_{ds}$, and $C_{db}$ are obtained, using eqns. (5-6) as illustrated in Fig.7.

$$R_{db}\approx\Re\{(Y_{22}+Y_{12}-g_{ds})^{-1}\};\; C_{ds}\approx\frac{\partial}{\partial\omega}(\Im\{Y_{22}+Y_{12}\}) \quad (6)$$

Figs. 8-13 summarize the impact of de-embedding $R_s$, $R_g$, and $R_d$ on the accuracy of the small-signal equivalent circuit parameters. By not adequately de-embedding these series parasitics from the measured S parameter data, transconductance and capacitance can be overestimated by more than 15%, and the NQS parameters $R_i$, $R_{gd}$, and $\tau_g$ by more than 200%. The latter are particularly sensitive to the values of $R_s$, $R_g$, and $R_d$ and their accurate experimental extraction remains questionable.

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## SCALABLE MODEL VERIFICATION

The single-transitor extraction methodology was applied to a minimal set of appropriately selected low, standard, and high-$V_T$ transistors from which a single scalable BSIM3v3 model was built around the convetional digital core model provided by TSMC. The latter was extracted from DC and low-frequency C-V measurements. $R_g$, $R_{gd}$, $C_{ds}$, as well as gate and drain fringing capacitances were appended to the core model using a subcircuit. Figs. 13-17 illustrate the extraction of the series resistance, overlap and area capacitance. Comparison of measured and simulated results demonstrates the excelent scalability of the model over gate width (Figs. 18-22) and over threshold voltage (Figs. 23 and 24). The model accurately captures $f_T$ degradation (Fig. 22) for minimum gate width, as well as the continued improvement in $f_{MAX}$ beyond 120 GHz as the unit finger width, and hence gate resistance, is reduced. Note that the transconductance remains unchanged at 1mS/μ m even for a unit finger width of 0.5 μ m indicating that $f_T$ degardation is solely due to gate-bulk overlap capacitance.

The model was next (Figs 25-28) employed to simulate the performance of a MOS-CML driver, using low- and staandard $V_T$ MOSFETs, and operating at 10-to-20 Gb/s data rates from a 1.2-V supply. The agreement is very good for both small-signal S-parameters, as well as for the jitter and rise/fall times of eye diagrams measured at 10- to-14-Gb/s data rates.

## CONCLUSIONS

A technique for the direct extraction of the NQS equivalent circuit parameters of 0.13-μ m MOSFETs was presented. This allowed for the development of a scalable RF subcircuit usable for devices with variable gate length, width and thershold. The model accurately captures $f_T$ and $f_{MAX}$ behaviour for the entire bias range and useful device geometries. Its validity was verified on the S-parameter and jitter performance of 10-Gb/s output drivers.

## REFERENCES

[1] F.X. Pengg, "Direct parameter extraction on RF-CMOS," *RFIC-Symp. Digest*, pp.271-274, 2002.

[2] Y-S. Lin, S-S. Lu, T-H.Lee and H-B.Liang, "Characterization and modeling of small-signal substrate resistance effect in RF CMOS," *RFIC-Symp. Digest*, pp.161-164, 2002.

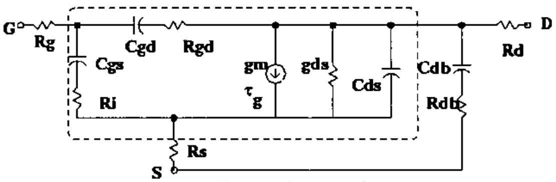

*Figure 1 Small signal equivalent circuit.*

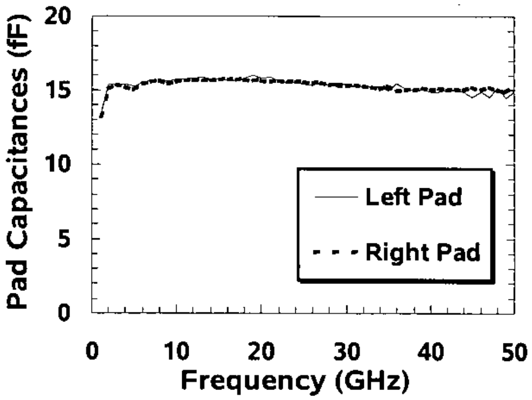

*Figure 2 Measured input pad and output pad capacitance as a function of frequency for a typical transistor test structure. Note that there is no noticeable resistive loss.*

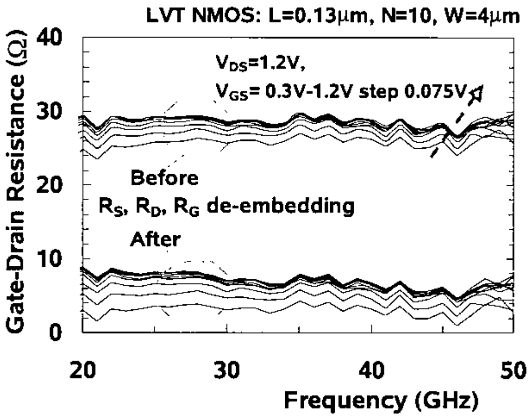

*Figure 3 Frequency dependence of the extracted $R_{gd}$ using eqn. (1) with and without de-embedding $R_s$, $R_g$ and $R_d$.*

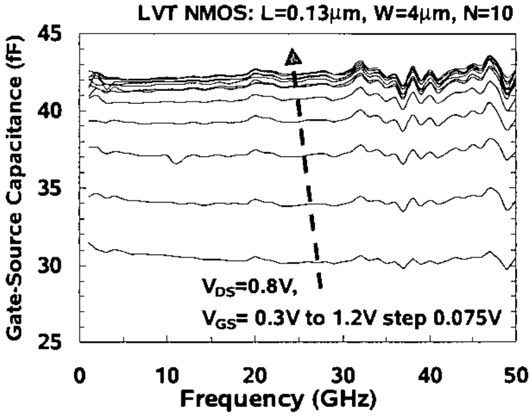

*Figure 4 Extracted $C_{gs}$ after de-embedding $R_s$, $R_g$ and $R_d$.*

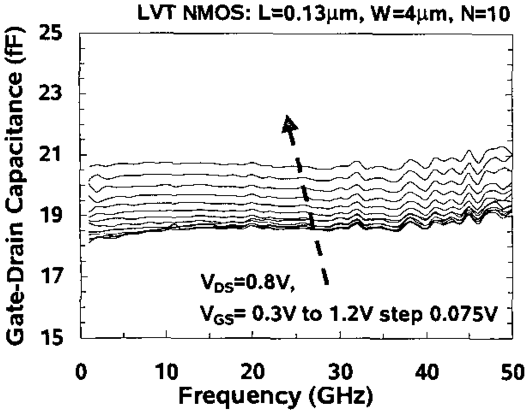

*Figure 5 Extracted $C_{gd}$ after de-embedding $R_s$, $R_g$ and $R_d$.*

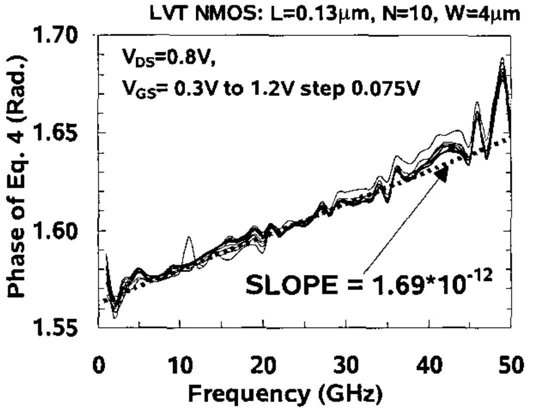

*Figure 6 Extraction of tau as from the slope of the measured phase in eqn. (4).*

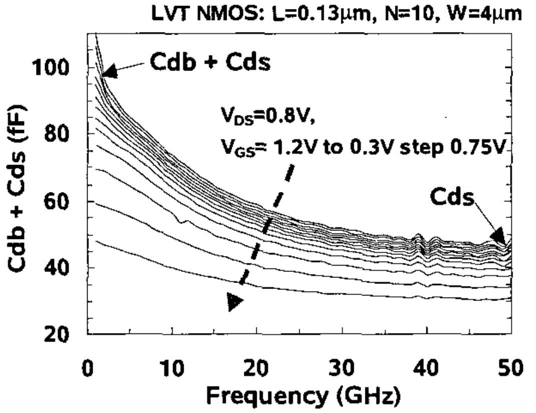

*Figure 7 Extraction of $C_{ds}$ and $C_{db}$ after de-embedding $R_s$, $R_g$ and $R_d$.*

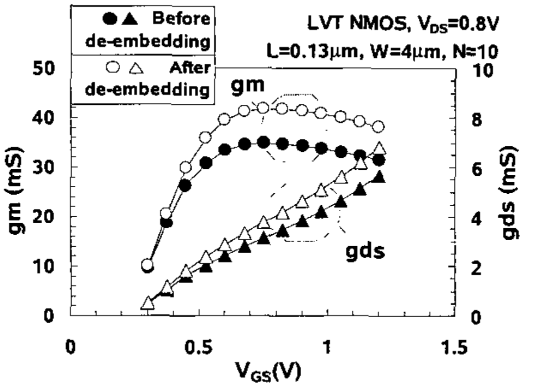

*Figure 8 Extracted transconductance and output conductance as a function of $V_{gs}$ before and after de-embedding of $R_s$, $R_g$ and $R_d$..*

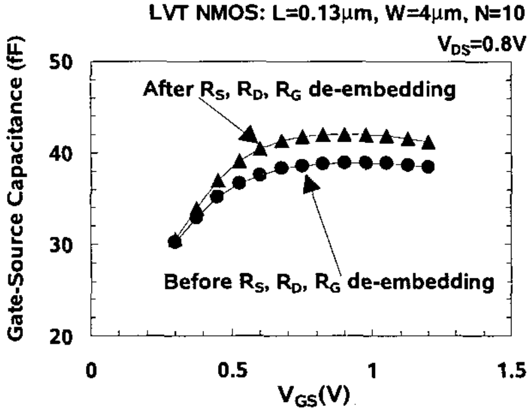

*Figure 9 Extracted $C_{gs}$ as a function of $V_{gs}$ before and after de-embedding of $R_s$, $R_g$ and $R_d$.*

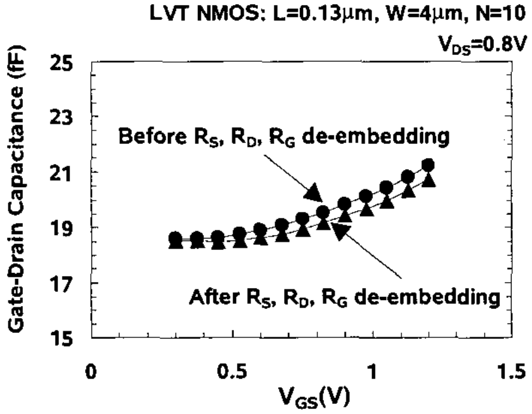

*Figure 10 Extracted $C_{gd}$ as a function of $V_{gs}$ before and after de-embedding of $R_s$, $R_g$ and $R_d$.*

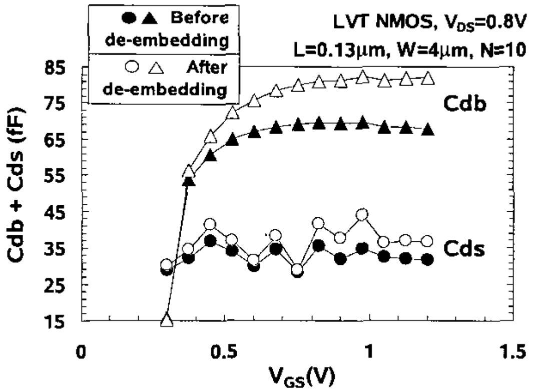

*Figure 11 Extracted $C_{ds}$ and $C_{db}$ as a function of $V_{gs}$ before and after de-embedding of $R_s$, $R_g$ and $R_d$.*

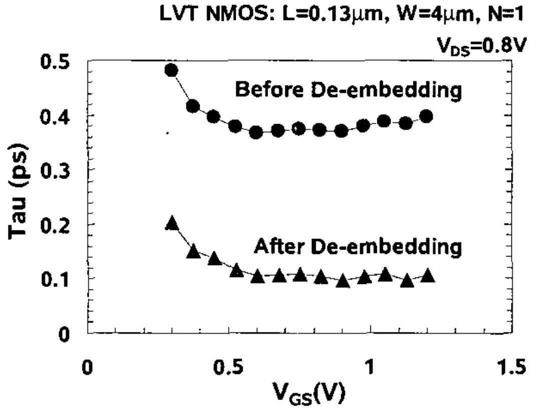

*Figure 12 Extracted transconductance delay as a function of $V_{gs}$ before and after de-embedding of $R_s$, $R_g$ and $R_d$.*

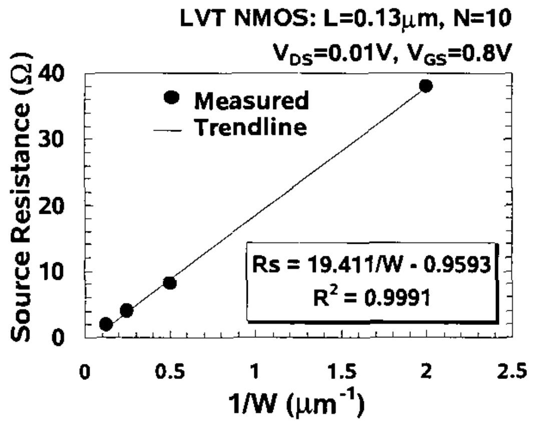

*Figure 13 Extracted source series resistance $R_s$ as a function of unit gate finger width, W.*

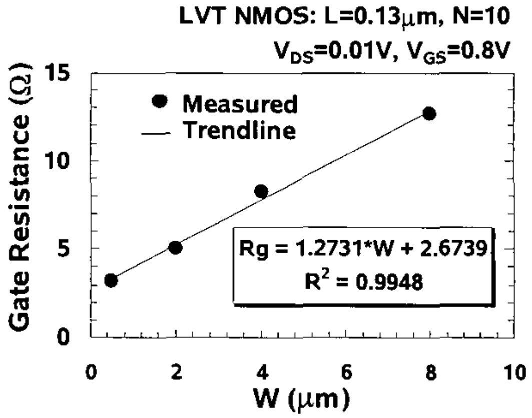

Figure 14 Extracted gate resistance $R_g$ as a function of unit gate finger width, W.

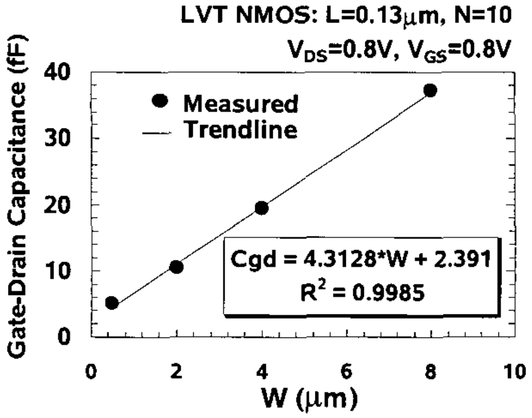

*Figure 15 Extracted gate-drain capacitance as a function of unit gate finger width, W.*

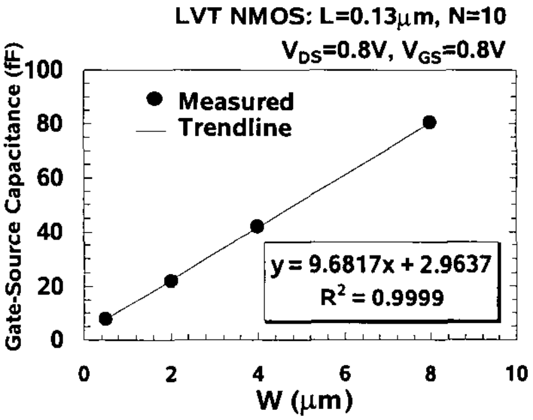

*Figure 16 Extracted gate-source capacitance as a function of unit gate finger width, W.*

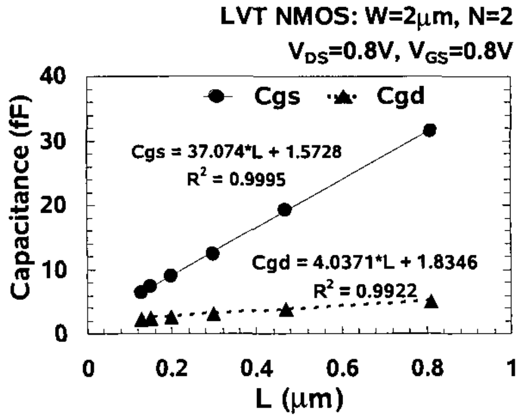

*Figure 17 Extracted $C_{gs}$ and $C_{gd}$ as a function of unit gate length, L.*

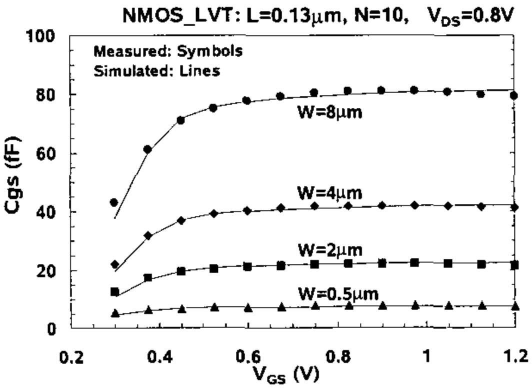

*Figure 18 Measured vs. simulated $C_{gs}$ as a function of $V_{gs}$ and unit gate finger width, W.*

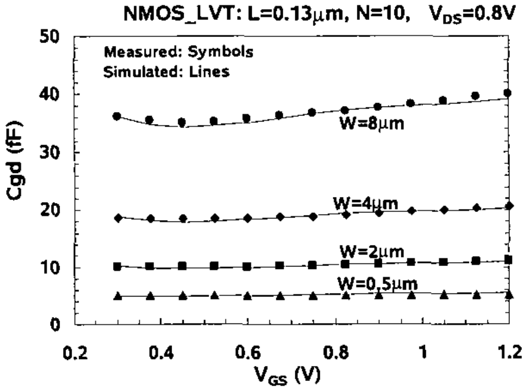

*Figure 19 Measured vs. simulated $C_{gd}$ as a function of $V_{gs}$ and unit gate finger width, W.*

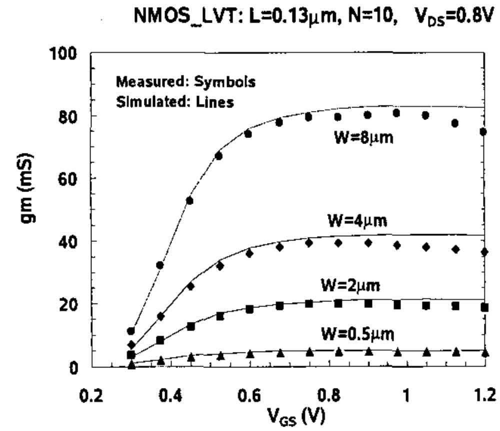

*Figure 20 Measured vs. simulated $g_m$ as a function of $V_{gs}$ and unit gate finger width, W.*

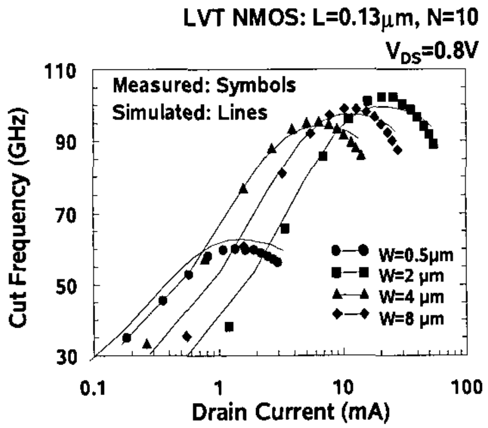

*Figure 21 Measured vs. simulated $f_T$ as a function of $I_{DS}$ and unit gate finger width, W.*

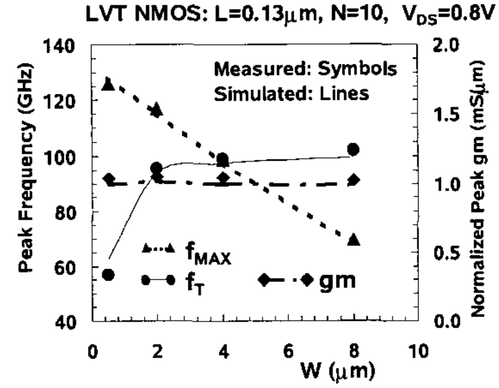

*Figure 22 Measured vs. simulated peak $f_T$, $f_{MAX}$, and $g_m/(NW)$ as a function of unit gate finger width, W.*

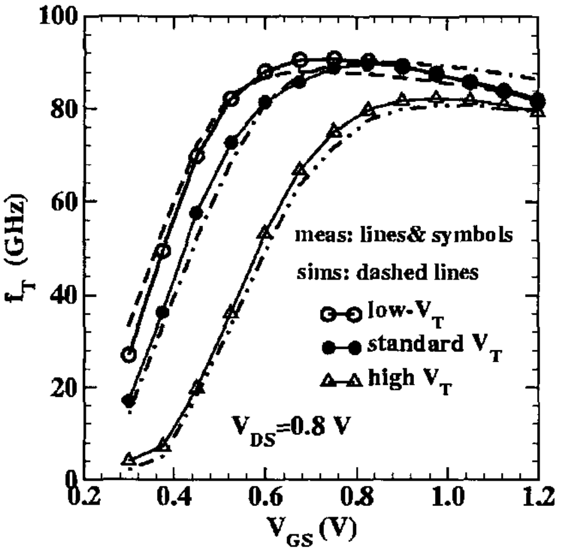

*Figure 23 Measured vs. simulated $f_T$ as a function of $V_{gs}$ for 0.13-μ m n-MOSFETs with 10x4μ m gate fingers.*

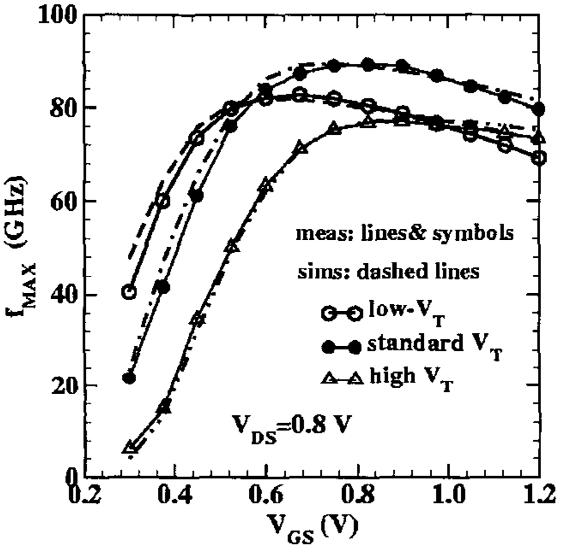

*Figure 24 Measured vs. simulated $f_{MAX}$ as a function of $V_{gs}$ for 0.13-μ m n-MOSFETs with 10x4μ m gate fingers.*

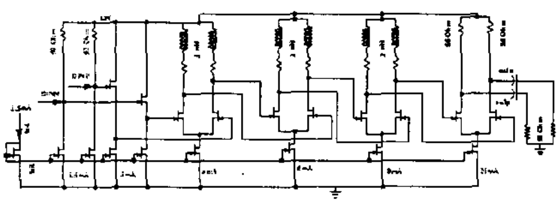

*Figure 25 Schematics of broadband driver test structure with three inductively-peaked gain cells, 50-Ω output stage, and source-follower input.*

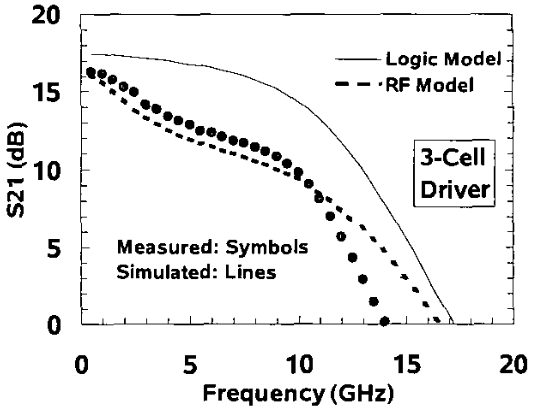

*Figure 26 Measured vs. simulated (using logic and RF-models) single-ended gain vs. frequency characteristics of driver test structure.*

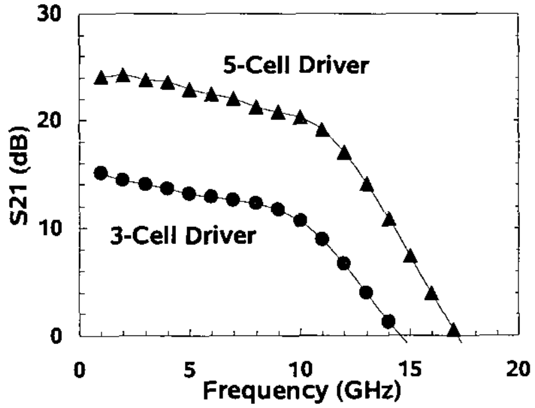

*Figure 27 Measured gain of 3-cell and 5-cell driver test structures after redesign using the RF scalable model.*

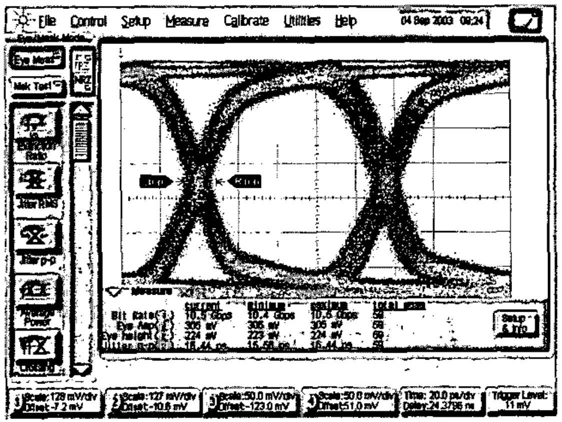

*Figure 28 Measured 10-Gb/s eye of 3-cell driver test structure with 50-mVp-p input signal.*