Optimized Ge Channel Profiles for VLSI Compatible Si/SiGe p-MOSFET's

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Abstract

Theoretical and experimental support is provided to demonstrate that, with the design constraint of a fixed Ge dose, the effective hole mobility and carrier confinement in SiGe MOSFET's are maximized by employing positively graded triangular Ge profiles in the channel. Hole mobilities in excess of 400 cm^2/Vs were obtained experimentally for transistors with 0-50% triangular Ge channel profiles. When compared to devices with rectangular Ge profiles, the MOSFET's with triangular profiles demonstrated 30-40% improvement in mobility, transconductance and cutoff frequency. These results were observed for both MBE- and CVD-grown wafers.

Introduction

Type I Si/SiGe/Si p-channel MOSFET's [1,2], shown in Fig. 1(a), are relatively easy to fabricate in a VLSI process [3] and have exhibited hole mobilities higher than in Si devices, but well below those measured in type II Schottky gate, Modulation-Doped FET's.

Previous refinements in the design of Si/SiGe p-MOSFET's have involved the placement of a δ-doped boron layer underneath the SiGe channel, as shown in Fig. 1.b, in order to control the threshold voltage, and a trapezoidal Ge channel profile that resulted in a sharper turn-on [4]. However, the peak Ge mole fraction was limited to 25% [4,5] and the carrier mobility and confinement remained practically unchanged from the values measured in devices with rectangular Ge profile [1-3].

It is probable that a significant increase in performance can only be attained if channels with very large (in excess of 40-50%) Ge mole fractions are used. However, practical implementations of large Ge mole fractions in Type I p-MOSFET's have been hampered by the necessity of complying with the Matthews-Blakeslee critical layer thickness [6], by the rectangular [1-3] or trapezoidal shape [4,5] of the Ge profile, and by interface scattering at very abrupt Si/SiGe interfaces [5]. The latter severely degrades mobility. We have recently demonstrated, through simulation [7] and experiments [8], that a practical solution to these problems may be achieved by using a triangular 0-40% Ge profile in the channel.

This work focuses on a design methodology for Si/SiGe MOSFET's with triangular Ge profiles, as well as on a comprehensive comparison of triangular and rectangular Ge channel profiles.

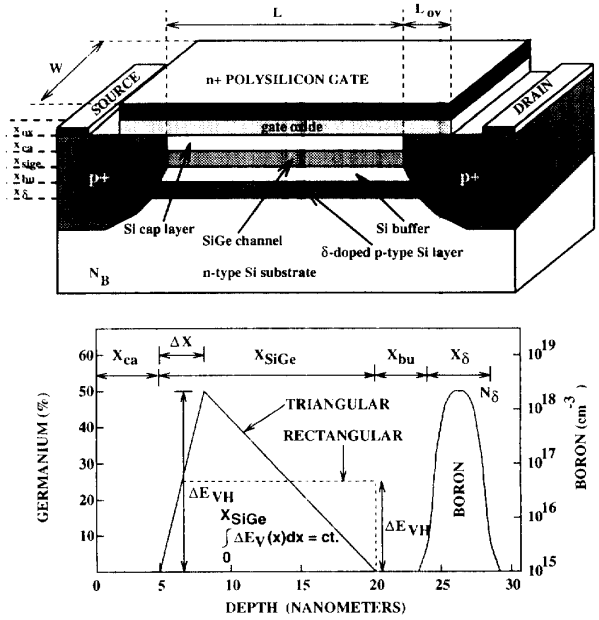

Fig. 1: a) Layer structure of a Si/SiGe/Si p-MOSFET. b) Vertical cross section showing schematic germanium and boron profiles considered in this work.

Design Optimization

The design of Type I Si/SiGe p-MOSFET's should aim for the simultaneous maximization of hole mobility and confinement in the SiGe channel within the bounds of a fixed Ge dose. The theoretical prediction of hole mobility as a function of the Ge profile is at best controversial. Considerations based on the effective mass suggest that hole mobility increases at higher Ge mole fractions but, because of the interplay of additional variables such as alloy and interface scattering, validation can only be provided by experiments.

Carrier confinement, however, is readily predictable and can be expressed in terms of the gate voltage window ΔV_T, defined as the difference between the threshold voltage of the buried SiGe channel V_{TH} and that of the surface Si channel V_{TS} [9]

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$$\Delta V_T = V_{TH} - V_{TS} \quad (1)$$

where

$$V_{TH}=V_{FB}+\phi_{TH}-q\left[N_B x_{dmax}-N_\delta x_\delta\right]\left(\frac{x_{ca}}{\varepsilon_{Si}}+\frac{x_{ox}}{\varepsilon_{ox}}\right) \quad (2)$$

and

$$V_{TS} = V_{FB} - 2\phi_F + f(\Delta E_{VH}, x_{ca}, x_{ox}, N_B) \quad (3)$$

ϕ_{TH} and ΔE_{VH} are the threshold potential and the valence band offset at the top Si/SiGe heterojunction. ϕ_F is the Fermi potential in the silicon substrate

$$\phi_{TH} = -2\phi_F+\frac{\Delta E_{VH}}{q}, \quad \phi_F = \phi_T \ln\left(\frac{N_B}{n_{iSi}}\right)$$

x_{ox}, x_{ca}, x_{bu}, x_δ and x_{dmax}, defined in Fig. 1, are the thicknesses of the oxide, the Si cap, the Si buffer, the δ-doped layer, and of the Si substrate depletion layer, respectively. $f(\Delta E_{VH}, x_{ca}, \Delta x, x_{ox}, N_B)$ has a complex form, but does not depend on the boron dose, as shown in Fig. 2. V_{TH} is almost linearly dependent on the boron dose, whereas V_{TS} remains insensitive to it. V_{TS} is strongly dependent on ΔE_{VH}, the gate-to-channel spacing ($x_{ca} + \Delta x$), and on the gate oxide thickness. Δx, defined in Fig. 1, is the distance over which the Ge profile is graded at the top heterojunction in order to reduce interface scattering.

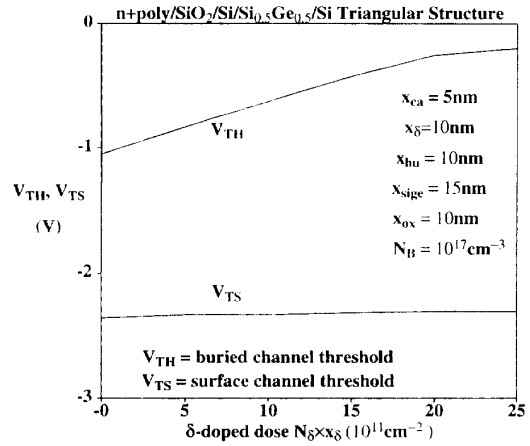

Fig. 2: Numerically computed threshold voltages as functions of the boron dose in the δ-doped layer. The maximum boron dose, beyond which V_{TH} is no longer controlled, is 2×10^{12} cm^{-2}.

For effective gate-to-channel voltages ranging between V_{TH} and V_{TS}, the SiGe MOSFET operates under ideal conditions, with 100% carrier confinement in the SiGe channel. At larger gate voltage swings, by the time the crossover voltage [5] is reached, the small signal performance of the SiGe MOSFET is considerably degraded and becomes comparable to that of a Si MOSFET.

Maximization of the gate voltage window as well as a large effective carrier mobility lead to optimal device performance in terms of current driving capability, transconductance and cutoff frequency [10]. To that end, the vertical layer structure design should proceed as follows.

a) For a given bias supply V_{DD} and channel length L, select the gate oxide thickness as in a conventional Si p-MOSFET.

b) Also as for Si p-MOSFET's, select the Si substrate doping N_B that satisfies the condition for the suppression of the drain-induced barrier lowering effect [10].

c) To reduce scattering at the Si/SiO_2 interface and to maximize ΔV_T, the Si cap layer thickness should be chosen in the 5 nm to 8 nm range.

d) Maximize the Ge mole fraction and valence band offset at the top of the channel ΔE_{VH}, while keeping the total Ge dose below the critical limit, so that

$$|V_{TS}| \geq V_{DD} \text{ and } |V_{TH}| + \Delta V_T \geq V_{DD} \quad (4)$$

e) To reduce interface scattering, the top Si/SiGe heterojunction must be graded over 2-3 nm, but the total gate-to-channel spacing ($x_{ca}+\Delta x$) should be kept below 10 nm.

f) Choose the boron dose in the δ-doped layer to meet the threshold voltage specification. To prevent degradation of the subthreshold characteristics, the boron dose must not exceed the value beyond which the boron layer is no longer depleted of carriers.

g) To avoid mobility degradation, caused by impurity scattering, the thickness of the undoped Si buffer should lie between 5 nm and 10 nm.

Because of the large Ge mole fractions involved, condition (4) is hard to implement in practice with rectangular or trapezoidal profiles. As illustrated in Fig. 3 -- where the gate voltage window is plotted as function of the Ge mole fraction grading from the bottom to the top of the channel -- using a triangular profile, in conjunction with a SiGe channel thickness of 10 to 15 nm, maximizes ΔV_T and V_{TS} for a given Ge dose.

Experimental

To verify these design principles, devices with triangular and rectangular Ge profiles were fabricated, using both MBE and CVD techniques. The MBE devices were fabricated on the same wafer with Si MOSFET's, in a CMOS-compatible, LOCOS isolated process [8]. CVD transistors were fabricated on blanket wafers using field oxide for isolation [5]. The boron dose in the δ-doped layer was 1.5×10^{12}cm^{-2} and the substrate doping was 3.5×10^{16}cm^{-3}. The nominal layer structure of the five test wafers is described in Table 1. The thickness of the SiGe film on all wafers was 15 nm. The peak Ge mole fraction was calibrated based on data obtained from heterostructure MOS capacitor measurements [11]. C-V measurements

were also used to confirm the value of the silicon cap layer thickness obtained by Auger Electron Spectroscopy.

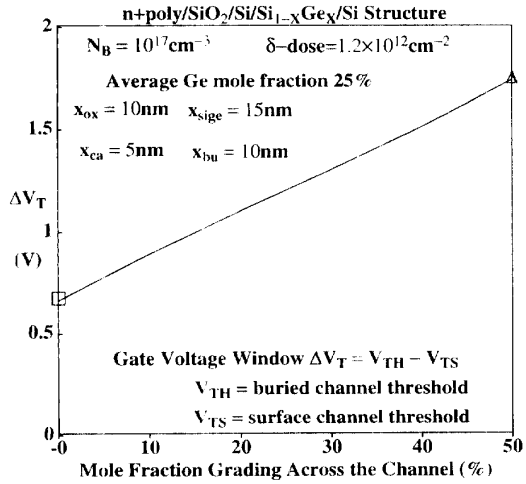

Fig. 3: Numerically computed gate voltage window as a function of the Ge mole fraction grading from the bottom to the top of the channel. The cases of the rectangular 25% Ge and of the triangular 0-50% Ge profiles are shown at the extreme left and right side, respectively. In-between, the results correspond to trapezoidal profiles.

TABLE 1: NOMINAL LAYER STRUCTURE			
Wafer	Profile	Si Cap Thickness	Oxide Thickness
#21	○ 0-40%Ge MBE	8 nm	16 nm
#23	□ 25%Ge MBE	8 nm	16 nm
#24	Δ 0-50%Ge MBE	8 nm	16 nm
#89-2	Δ 0-50%Ge CVD	2 nm	10 nm
#90-2	■ 25%Ge CVD	2 nm	10 nm

Results and Discussion

The gate voltage window can be extracted from the width of the plateau region of the C-V characteristics [11]. The dependence of the gate voltage window on the peak Ge mole fraction, and not on the total Ge dose, is confirmed by the experimental C-V characteristics of Fig. 4. A widening capacitance plateau is noticed as the Ge profile changes from 25%Ge rectangular, to 0-40%Ge triangular and, finally, to 0-50%Ge triangular. In the latter case, the gate voltage window was approximately 3V.

Hole mobility, the other important parameter for device performance, was measured by a modified split C-V technique [7] and is plotted in Fig. 5. It increases from 250 cm^2/Vs in rectangular 25%Ge MOSFET's, to over 400 cm^2/Vs for devices with 0-50%Ge triangular profiles. In order to avoid crowding the plot, the results for the transistors with 0-40% triangular Ge profiles are not shown. The hole mobility in that case was also 250 cm^2/Vs. The large Ge mole fraction and the grading of the top Si/SiGe interface over 2.5 nm (thereby reducing interface scattering), are responsible for the large hole mobility. This is the first experimental proof that the mobility of holes in type I Si/SiGe/Si channels improves as the Ge concentration is increased beyond 40%. The 400 cm^2/Vs figure is the largest reported for this heterostructure alignment, and indicates a factor of 2.5 improvement over the room temperature hole mobility in Si p-MOSFET's, typically 150 cm^2/Vs.

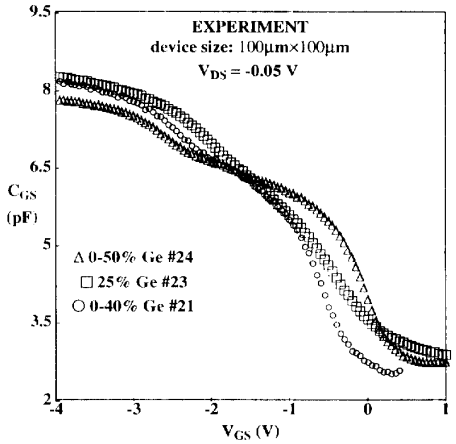

Fig. 4: Comparison of experimental C-V characteristics for SiGe p-MOSFET's with triangular and rectangular Ge profiles.

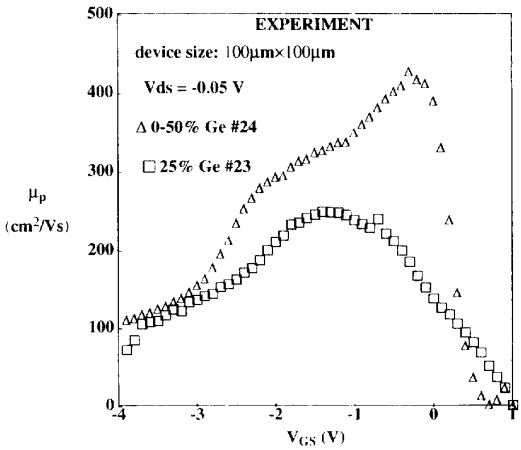

Fig. 5: Comparison of experimental mobility vs. gate voltage characteristics for SiGe p-MOSFET's with triangular and rectangular Ge profiles.

The steeper slope of the mobility characteristics, immediately above threshold, for the transistors with triangular Ge profiles is caused by the built-in grading field. The large mobility value is also an indication of the abrupt boron profiles and that the carriers in the channel are well separated from the impurities located in the δ-doped layer.

The large gate voltage window and carrier mobility translate into improved current driving capability, transcon-

ductance and cutoff frequency, as shown in Figs. 6, 7 and 8, respectively. The peak cutoff frequency depends primarily on the effective carrier mobility and velocity. The curves in Fig. 8 indicate that mobility improvement from rectangular to triangular profiles is obtainable with both MBE and CVD layers. The thinner Si cap layer in the CVD wafers causes Si/SiO_2 interface scattering at large gate voltages. This reflects in the steeper f_T decrease for the CVD devices.

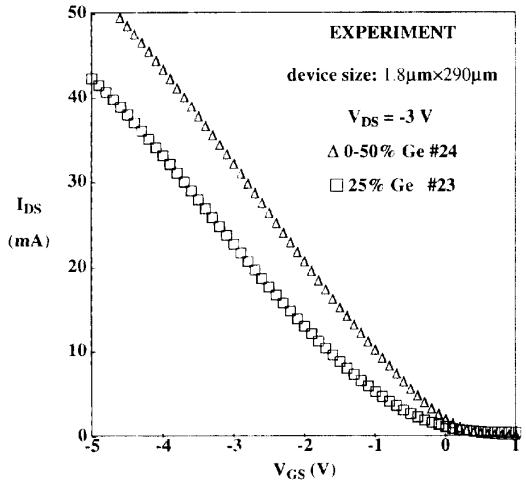

Fig. 6: Comparison of experimental transfer characteristics for Si and SiGe p-MOSFET's with triangular and rectangular Ge channel profiles.

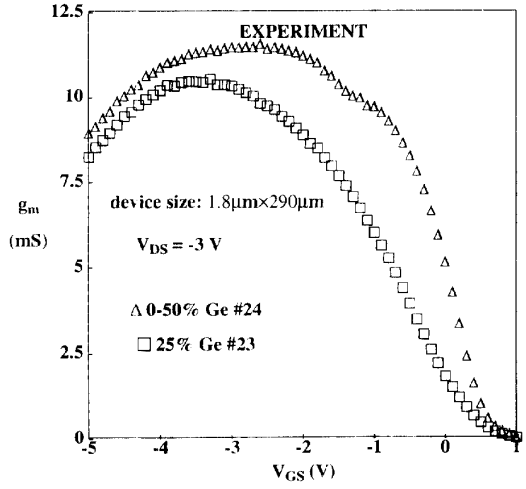

Fig. 7: Comparison of experimental transconductance characteristics in the saturation regime for SiGe p-MOSFET's with triangular and rectangular Ge profiles.

Conclusions

Simulation and experiments have demonstrated that, within the design bounds of a fixed Ge dose, triangular channel profiles yield the largest reported carrier confinement and hole mobility in type I Si/SiGe p-MOSFET's. Carrier confinement increases with the peak Ge mole fraction in the channel, whereas a considerable mobility enhancement can be achieved only if the Ge mole fraction exceeds 40%. Hole mobilities as high as 400 cm^2/Vs were obtained in transistors with 0-50% triangular Ge channel profiles. Transistors with 10 nm thick SiGe channels and peak Ge mole fractions as high as 70% are expected to exhibit even larger hole mobilities and confinement, and appear now to be feasible.

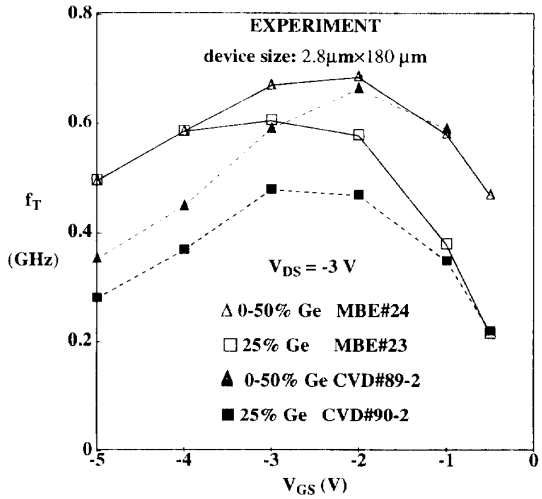

Fig. 8: Comparison of experimental cutoff frequency vs. gate voltage characteristics for MBE and CVD-grown SiGe p-MOSFET's.

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