

65GHz Doppler Sensor with On-Chip Antenna in 0.18 μm SiGe BiCMOS

Terry Yao, Lamia Tchoketch-Kebir, Olga Yuryevich, Michael Gordon, and Sorin P. Voinigescu

Edward S. Rogers Sr. Department of Electrical and Computer Engineering, University of Toronto,
10 King's College Rd, Toronto, ON Canada M5S 3G4

Abstract — A single-chip 65GHz Doppler radar transceiver with on-chip patch antenna is reported. Implemented in a production 0.18 μm SiGe BiCMOS process, it features a differential output transmit power of 4.3dBm, 16.5dB single-ended down-conversion gain and a double-sideband noise figure of 12.8dB. The radar includes a 65GHz 2-stage cascode LNA with $S_{11} < -15\text{dB}$ at 50-94GHz and 14dB gain at 65GHz, a double-balanced down-convert mixer, a SiGe HBT IF amplifier with low 1/f noise, a VCO and a 65GHz output buffer. The LO is provided by an integrated varactor-tuned 61-67GHz VCO optimized for low phase noise. The patch antenna is designed to be impedance-matched for dual-band operation at 62.8 and 64.6GHz. The use of lumped inductors in all blocks and a vertically-stacked transformer for single-ended to differential conversion in the receive path help reduce the transceiver area to 1mm x 1mm.

Index Terms — BiCMOS integrated circuits, Doppler radar, inductors, microstrip antennae, millimeter wave integrated circuits, transformers.

I. INTRODUCTION

Recent advances in SiGe technology have made it an attractive option for the implementation of affordable mm-wave circuits. The significantly smaller form factors of transformers, inductors and antennae at mm-waves bring closer the realization of truly single-chip radios with on-chip antenna. Taking advantage of the performance improvement in transistors and of the reduced size of the passives, several highly integrated mm-wave radio systems have recently been reported [1]-[5], operating in the 60GHz and 77GHz bands.

One of the critical challenges in radio system integration at mm-waves is the tuning bandwidth, phase noise and output power of the VCO. Unlike recent publications which report separate transmitters and receivers [1]-[5], in this paper, a single-chip 65GHz Doppler radar transceiver with on-chip microstrip patch antenna is presented, where the same LO signal is used for both 65GHz transmission and reception, as required for Doppler sensor applications. A fundamental frequency Colpitts VCO operating in the 61-67GHz range is integrated on the same die with all other transceiver components. While avoiding a power- and area-hungry multiplier architecture [1], this chip demonstrates a high level of integration at 65GHz, and addresses the potentially large volume market of mm-wave sensors for a variety of medical and security applications. It was implemented in a production 0.18 μm SiGe BiCMOS process featuring f_T and f_{MAX} values of 160GHz and a 6-metal backend with a thick Aluminum top layer.

II. RADAR TRANSCEIVER OVERVIEW

The block diagram of the radar transceiver is shown in Fig. 1 and includes a varactor-tuned VCO with 50-Ohm output buffer, LNA, downconvert mixer, IF amplifier, and on-chip receive antenna. The single-chip transceiver system makes extensive use of small footprint (less than 30 μm per side) inductors and transformers as matching elements to achieve significant area savings, in contrast to previous mm-wave circuits using distributed elements [1]-[5]. Modeling accuracy of inductors at mm-waves using the ASITIC software [6], verified in previously fabricated inductor test structures [7], results in greater robustness in the design of each tuned circuit. The VCO, LNA, output buffer and mixer all use HBT cascodes for higher gain and superior reverse isolation. In addition, the VCO, the most critical block, is a 61-67GHz replica of the differential Colpitts VCO presented in [8], which had a phase noise of -104dBc/Hz at 1MHz offset from a 60GHz carrier. The receive antenna is implemented as a 1.7x1.3mm² microstrip patch antenna, whose low profile planar configuration make it well-suited for on-chip integration. Details on the design and implementation of each transceiver block are presented in the following sections.

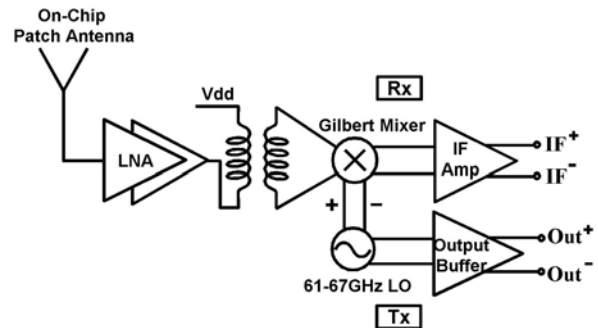


Fig. 1. Block diagram of Doppler radar transceiver.

III. RADAR TRANSCEIVER DESIGN

A. Receive Path

The receive path of the transceiver is illustrated in Fig. 2. The 65GHz RF signal arrives through an on-chip patch antenna connected by a microstrip feedline to the 65GHz LNA, followed by a down-convert Gilbert cell mixer and IF amplifier. A number of circuit techniques were employed to optimize the overall receiver gain, linearity and noise performance. The 2-stage cascode LNA is a modified version of that presented in [9], with a vertically stacked transformer output to drive the mixer differentially. Measurements of the

LNA breakout show $S_{11} < -15\text{dB}$ between 50 to 94GHz, 14dB gain, -12.8dBm $P_{1\text{dBm},\text{in}}$ and an IIP3 of -6dBm at 65GHz. The vertically stacked transformer is implemented in two adjacent metal layers for increased coil coupling and area efficiency. The down-convert mixer is designed to be simultaneously noise and power matched [9] to the 200-Ohm differential output impedance of the LNA. Inductive degeneration in the mixer ensures optimal linearity with minimal increase in noise. The mixer is driven by the 61-67GHz VCO through emitter follower buffers. Finally, since $1/f$ noise is more important than receiver noise figure in determining the overall sensitivity of a Doppler sensor, the IF amplifier is implemented with bipolar rather than MOS transistors [9].

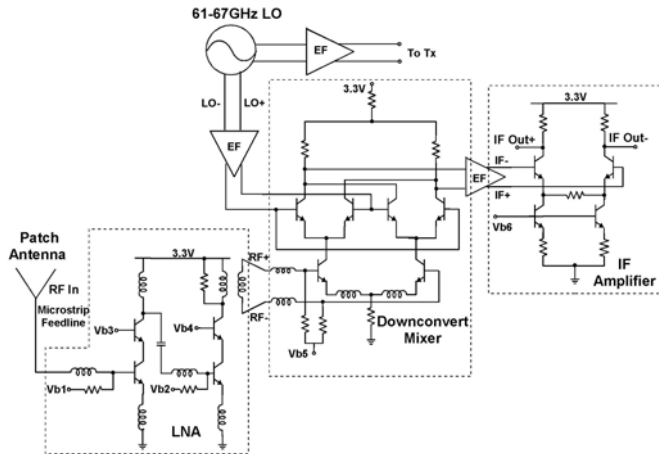


Fig. 2. Receive path of Doppler radar transceiver.

B. Transmit Path

The transmit path of the Doppler radar transceiver, shown in Fig. 3, consists of the VCO (shared with the receive side), two-stage emitter followers and a 65GHz output buffer driving 50-Ohm loads per side. The emitter followers provide DC level-shifting between the VCO output and the input differential pair of the output buffer. The output buffer is implemented as a differential cascode with inductive degeneration for improved linearity. Both the output buffer and VCO operate from a 4V supply and consume a total 394mW.

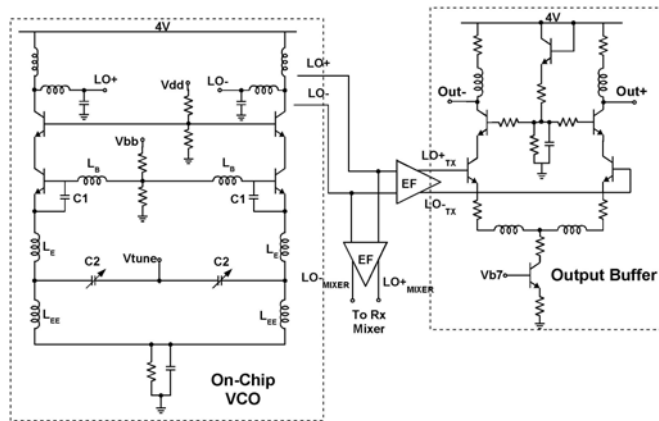


Fig. 3. Transmit path of Doppler radar transceiver with on-chip VCO, emitter followers and output buffer.

C. Microstrip Patch Antenna

The design of the microstrip patch antenna began with a hand analysis of the required antenna dimensions for operation in the 59-65GHz range. The analysis is based on the transmission-line model, which provides good physical insight in the design of microstrip-line inset-fed patch antennae. The high-frequency electromagnetic field solver, Sonnet, was then employed to model and simulate the patch antenna using the more accurate Method of Moments analysis. The antenna was realized in metal 6 with a metal 1 ground plane and SiO_2 as the low-loss dielectric. Both top and ground metals were slotted to meet chemical mechanical polishing density rules. Substrate contacts were placed throughout the ground plane to minimize coupling into the substrate. The metal ground plane is critical in maximizing on-chip isolation. Injection of signals into the substrate constitutes the main disadvantage of other antennae recently integrated in silicon [2,4,5], making them inadequate for CW Doppler sensors. Fig. 4 shows a cross-section of the patch antenna.

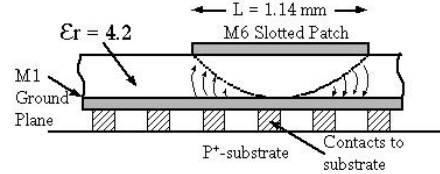


Fig. 4. Cross-sectional view of microstrip patch antenna.

The feedline position and the inset length were optimized using Sonnet to achieve a good input impedance match to 50-Ohm at the resonant frequency. The feedline is a $15\mu\text{m}$ wide and $800\mu\text{m}$ long transmission line, with the inset length being $400\mu\text{m}$. Simulated results of the patch antenna (Fig. 5) show dual-band operation at 62.8GHz and 64.6GHz with return loss better than 10dB. The final antenna dimensions are $1.7 \times 1.3\text{mm}^2$.

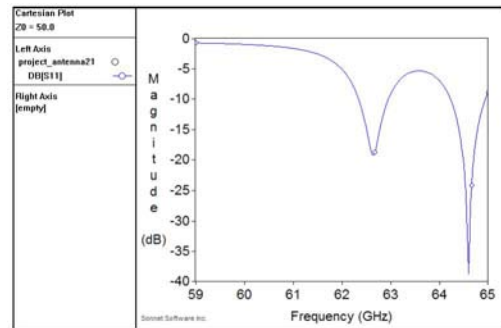


Fig. 5. Simulated return loss of microstrip patch antenna on silicon dioxide substrate.

IV. RADAR TRANSCIEVER FABRICATION AND MEASUREMENT

A. Fabrication

Two radar transceiver structures were fabricated on a $2.5 \times 2.5\text{mm}^2$ die, one with patch antenna and feedline connected directly to the LNA, and another without antenna to

allow for separate transceiver characterization through on-wafer probing. The differential nature of all blocks, with the exception of the LNA, results in a layout that is highly symmetric along the center axis. The full transceiver consumes 640mW. Fig. 6 shows the die micrograph of the 2.5x2.5mm² die and a close-up view of the radar transceiver structure.

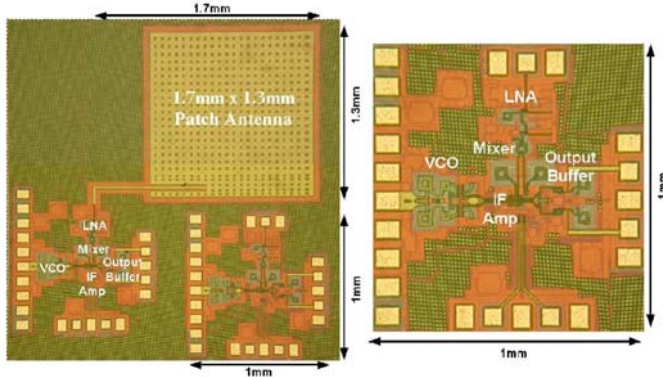


Fig. 6. Die micrograph of Doppler radar transceiver with and without patch antenna and close-up view of transceiver.

B. Measurement Setup and Results

The radar transceiver without patch antenna was first characterized through on-wafer probing using 65GHz GGB coaxial probes. Shown in Fig. 7 is a screen capture of the radar IF signal at 730MHz with an externally applied RF signal of -48dBm at 64GHz, demonstrating a single-ended down-conversion gain of 16.5dB. The spectrum was captured using an Agilent E4448A 3Hz-50GHz spectrum analyzer.

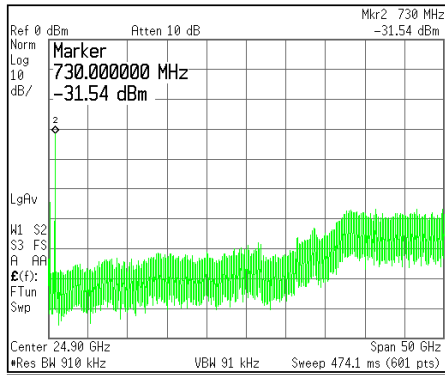


Fig. 7. Spectrum of Radar IF signal at 730MHz with RF input at 64GHz, -48dBm .

The single-ended receiver linearity measurements on the breakout without patch antenna show an input-referred $P_{1\text{dB}}$ of -30dBm , IIP3 of -20dBm (Fig. 8) and single-ended conversion gain of 16.5dB at IF frequencies between 10 MHz and 800 MHz. The operation of the receiver with on-chip antenna was verified by applying the 65GHz signal from an external source through a 65GHz GGB coaxial probe, or, through a 50-75GHz horn antenna with waveguide-to-coaxial adaptor, placed above the on-die patch antenna. In each experiment, five different conversion gains were recorded

corresponding to five different probe elevations with respect to the die. Fig. 9 reproduces the single-ended radar receiver conversion gains for the cases of on-wafer probing, probe suspended over patch antenna and horn antenna over the die. Fig. 10 shows the conversion gains for different elevations of the horn antenna above the die. The largest single-ended conversion gain was -24.5dB for the probe and -26dB for the horn antenna, indicating a loss of conversion gain of $\sim 40\text{dB}$ in comparison to the on-wafer probed receiver without antenna. A final experiment, whose setup is shown in Fig. 11, verified the non-line-of-sight operation of the Doppler radar receiver over a distance of a few meters when the signal from the horn antenna was reflected by an adjustable tin-foil plate to the on-chip patch antenna.

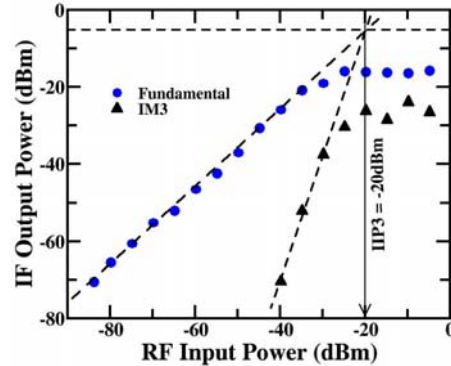


Fig. 8. Radar receiver IIP3 measured with 40MHz tone spacing.

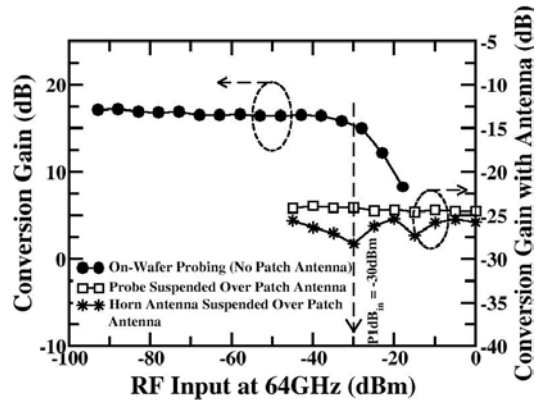


Fig. 9. Radar receiver conversion gains with 730MHz IF.

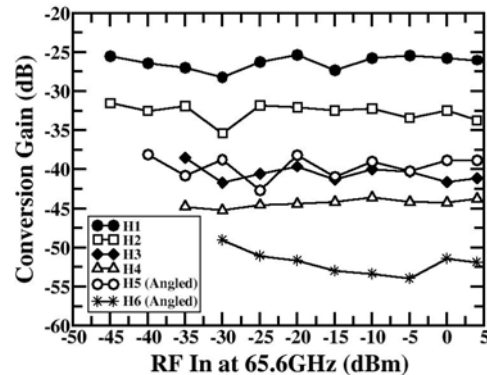


Fig. 10. Radar single-ended conversion gain at 730MHz IF with 6 different elevations of the 50-75GHz horn antenna over the on-chip patch antenna.

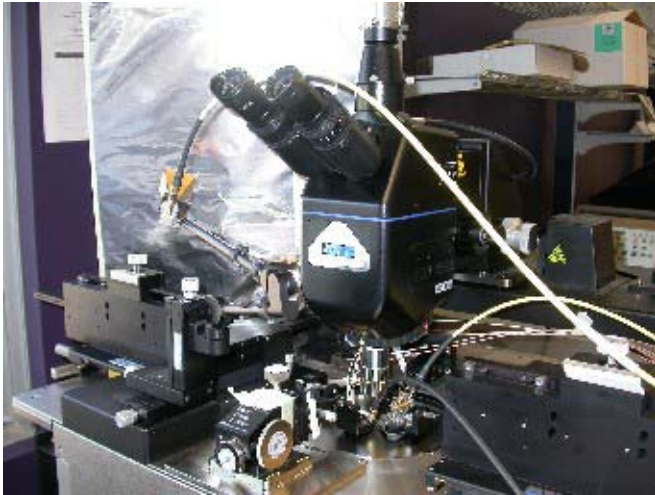


Fig. 11. Measurement setup of the horn antenna signal reflecting off an adjustable tin-foil plate to the on-chip patch antenna in Doppler radar non-line-of-sight experiment.

The radar receiver has a double-sideband noise figure of 12.5-13dB over an IF range of 0.4-2GHz. The measurement was performed using an HB8970B Noise Figure Meter and a 50-75GHz noise source from Noise Com. Losses in the measurement setup were de-embedded through calibrations at IF using a 0.01-18GHz noise source. The gain from the noise figure measurement is in close agreement with that obtained in the large signal spectral measurements. The measured noise figure and single-ended conversion gain are illustrated in Fig. 12.

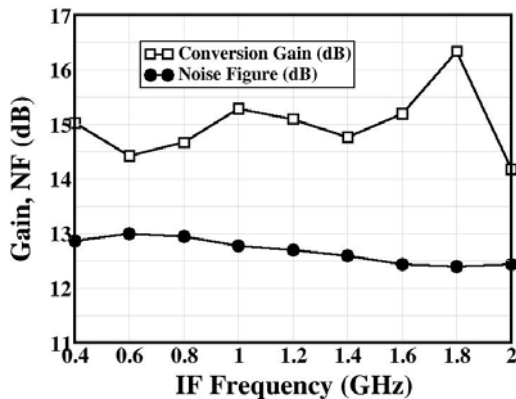


Fig. 12. Radar receiver single-ended conversion gain and noise figure vs. IF frequency, at nominal operating conditions.

A single-ended output spectrum of the radar transmitter is shown in Fig. 13, where the losses in the setup have not been de-embedded. The transmitter spectral measurements in the V-band were performed on the Agilent E4448A PSA with an external Agilent 11970V mixer. The single-ended output power of 1.3dBm (4.3dBm differential) was measured more accurately, after de-embedding setup losses at 64.8GHz using the Agilent E4419B EPM Series Power Meter with the Agilent V8486A Power Sensor.

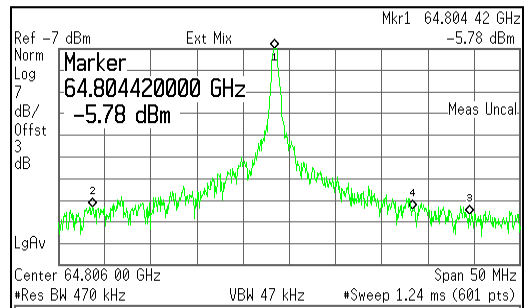


Fig. 13. Radar transmitter output spectrum.

V. CONCLUSION

A compact 65GHz Doppler sensor with on-chip patch antenna has been presented. It demonstrates the high level of integration achievable today in silicon, and hence the feasibility of low-cost implementations of mm-wave sensors for medical and security applications. The extensive use of lumped passive components, such as spiral inductors and stacked transformer, offers an area-efficient approach to mm-wave system integration.

ACKNOWLEDGEMENT

This work was supported by NSERC and Micronet, and chip fabrication was made possible by Jazz Semiconductor. The authors would also like to thank Kenneth Yau and Shahriar Shahramian at the University of Toronto for their assistance in the measurement process.

REFERENCES

- [1] B. Floyd *et al.*, "A Silicon 60GHz Receiver and Transmitter chipset for Broadband Communications," *ISSCC Dig. Tech. Papers*, pp. 184-185, February 2006.
- [2] C.H. Wang *et al.*, "A 60GHz Transmitter with Integrated Antenna in 0.18 μ m SiGe BiCMOS Technology," *ISSCC Dig. Tech. Papers*, pp. 186-187, February 2006.
- [3] B. Razavi, "A 60GHz Direct-Conversion CMOS Receiver," *ISSCC Dig. Tech. Papers*, pp. 400-401, February 2005.
- [4] A. Babakhani *et al.*, "A 77GHz 4-Element Phased Array Receiver with On-Chip Dipole Antennas in Silicon," *ISSCC Dig. Tech. Papers*, pp. 180-181, February 2006.
- [5] A. Natarajan *et al.*, "A 77GHz Phased-Array Transmitter with Local LO-Path Phase-Shifting in Silicon," *ISSCC Dig. Tech. Papers*, pp. 182-183, February 2006.
- [6] ASITIC <http://rfic.eecs.berkeley.edu/~niknejad/asitic.html>
- [7] T. Dickson *et al.*, "30-100GHz Inductors and Transformers for Millimeter-Wave (Bi)CMOS Integrated Circuits," *IEEE Trans. Microwave Theory and Techniques*, vol. 53, pp. 123-133, January 2005.
- [8] C. Lee *et al.*, "SiGe BiCMOS 65GHz BPSK Transmitter and 30 to 122GHz LC-Varactor VCOs with up to 21% Tuning Range," *IEEE Compound Semiconductor Integrated Circuits Symposium*, pp. 179-182, October 2004.
- [9] M. Gordon *et al.*, "65-GHz Receiver in SiGe BiCMOS using Monolithic Inductors and Transformers," *Silicon Monolithic Integrated Circuits in RF Systems, Technical Digest*, pp. 265-268, January 2006.