A Low-Voltage 77-GHz Automotive Radar Chipset

Sean T. Nicolson[1], Keith A. Tang[1], Kenneth H.K. Yau[1], Pascal Chevalier[2], Bernard Sautreuil[2], and Sorin P. Voinigescu[1]

1) Edward S. Rogers, Sr. Dept. of Electrical & Comp. Eng., University of Toronto, Toronto, ON M5S 3G4, Canada
2) STMicroelectronics, 850 rue Jean Monnet, F-38926 Crolles, France

***Abstract* — This paper presents the first complete 2.5V, 77GHz chipset for Doppler radar and imaging applications fabricated in 0.13μm SiGe HBT technology. The chipset includes a voltage-controlled oscillator with -101.6dBc/Hz phase noise at 1MHz offset, an 25dB gain low-noise amplifier, a novel low-voltage double-balanced Gilbert-cell mixer with two mm-wave baluns and IF amplifier achieving 12.8dB noise figure and an OP1dB of +5dBm, a 99GHz static frequency divider consuming a record low 75mW, and a power amplifier with 19dB gain, +14.4dBm saturated power, and 15.7% PAE. Monolithic spiral inductors and transformers result in the lowest reported 77GHz receiver core area of only 0.45mm × 0.30mm. Simplified circuit topologies allow 77GHz operation up to 125ºC from 2.5V/1.8V supplies. Technology splits of the SiGe HBTs are employed to determine the optimum HBT profile for mm-wave performance.**

***Index Terms* — Automotive radar, millimeter-wave receivers and transmitters, millimeter-wave imaging, low-noise amplifiers, power amplifiers, monolithic inductors and transformers.**

I. Introduction

Using the latest SiGe processes with f_T/f_{MAX} above 200GHz [1], circuits for W-band radar and millimeter-wave imaging are under developement. State-of-the-art demonstrations of silicon technology in W-band applications include circuit blocks at 77GHz [2]-[6], and 94GHz [7]-[9], [19], and 77GHz receivers and transmitters [10]-[14], [18].

A transceiver array is required in imaging applications, and therefore power consumption and reliability are critical. The power supply voltage of the SiGe mm-wave transceiver must be reduced from the nominally used values of 5.5V/3.3V [3]-[6], [8]-[14], to 2.5V, or even 1.8V [2]. Circuit architectures must be simplified to decrease the device count, further reducing power consumption, and improving reliability. Furthermore, the HBTs must be optimized for mm-wave performance. The simultaneous mm-wave and DSP demands of W-band imaging and radar systems make a fine lithography SiGe BiCMOS process [16] an attractive technology choice at mm-waves [15].

This paper presents a 2.5V, 77GHz SiGe BiCMOS chipset for automotive and mm-wave imaging applications. Unlike other efforts to date, this chipset contains all critical blocks (VCO, LNA, PA, mixer, and static frequency divider) required to fabricate a fully integrated 2.5V, 77GHz transceiver with PLL. In the following sections, an overview of the transceiver architecture is given, the novel aspects of each circuit block are described, and circuit measurement results over wafer splits and temperature are presented.

II. Transceiver Architecture

A block diagram of the direct conversion Doppler transceiver is shown in Fig. 1, where boxes with dashed lines indicate circuit blocks. The transceiver employs mm-wave baluns for single-ended to differential conversion, similar to [17]. The first stage of a static frequency divider is demonstrated to show that a robust PLL can be added to the transceiver. A robust, low phase noise PLL and VCO require MOSFETs, once again pointing to the need for a BiCMOS process for mm-wave radar and imaging systems [15], [16].

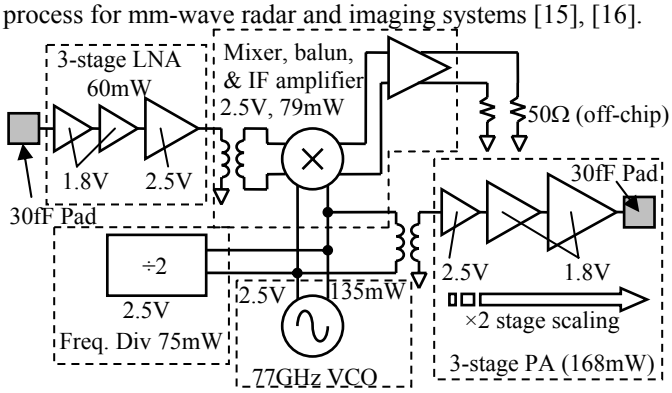

Fig. 1. 77GHz Doppler transceiver architecture.

III. Circuit Building Blocks

A. Low Noise Amplifier and Power Amplifier

The schematic of the LNA is shown in Fig. 2. The first two stages are common-emitter (CE) to allow 1.2-1.8V operation, and to minimize the noise figure. All stages are simultaneously noise and impedance matched using the techniques described in [9]. The LNA consumes a total of 40mW from 1.5V/1.8V supplies or 60mW from 1.8V/2.5V supplies. The simulated noise figure and gain are 5.3dB and 21dB, respectively.

Fig. 3 illustrates a simplified PA schematic. The later stages are common-emitter to minimize power consumption and maximize power-added-efficiency (PAE); the transistors and bias currents are scaled by a factor of 2 from stage to stage. In simulation, the PA achieves 23dB gain, 14.5dBm saturated output power, and 16.4% PAE.

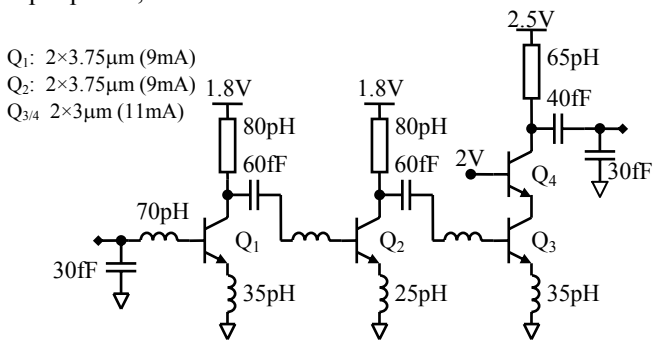

Fig. 2. 1.8V/2.5V, 3-stage, 77GHz LNA schematic.

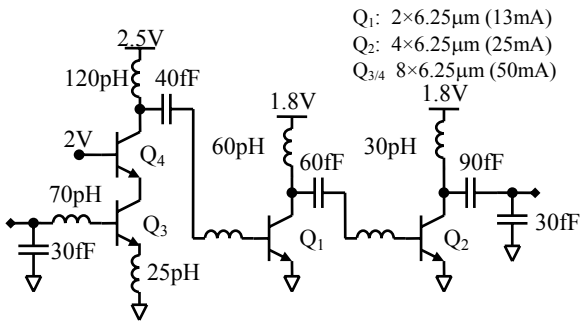

Fig. 3. 1.8V/2.5V, 77GHz, 3-stage power amplifier schematic.

C. Voltage-controlled oscillator

The VCO schematic is shown in [7], along with the design methodology for minimum phase noise. In this bipolar-only version, the VCO is designed to provide 5dBm of differential output power and 4GHz of tuning range (5%) using HBT varactors, and consumes 135mW from a 2.5V supply.

D. Mixer, Balun, and IF Amplifier

A novel low-voltage, mm-wave, Gilbert cell mixer is illustrated in Fig. 4. To allow reduction of the supply voltage down to 2.5V, the RF pair is replaced by the secondary coil of a transformer, and the primary coil becomes the load inductor of the final LNA stage. A current source biases the mixing quad through the center tap of the secondary winding. The 2.5V design used here allows 1.5V swing per side (1.2dBm) at the mixing quad output, and consumes only 12.5mW. Using this mixer topology, the bias current in the mixing quad can be set independently without added current sources, unlike the conventional Gilbert cell.

The IF amplifier is a resistively degenerated differential pair with 50Ω load. Consuming 66mW, it provides 3dB of power gain and a simulated OP1dB of 6.5dBm at 1GHz IF. In simulation, the transformer, mixer, and IF amplifier together have conversion gain of 12dB at 1GHz IF, using a +1dBm 77GHz LO. Optimization of degeneration resistances and bias currents achieves high linearity without resorting to complex circuit topologies [4] that require higher supply voltage.

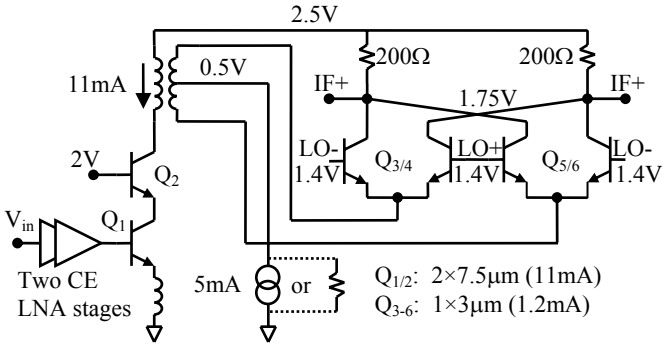

Fig. 4. Low-voltage double balanced mixer without RF pair.

E. Static Frequency Divider

To reduce the supply voltage and improve the self-oscillation frequency of the latch, all current sources are replaced with resistors, as shown in Fig. 5. Transistor sizes, bias currents, collector-emitter voltages, and output voltage swing are all optimized based on the results in [8].

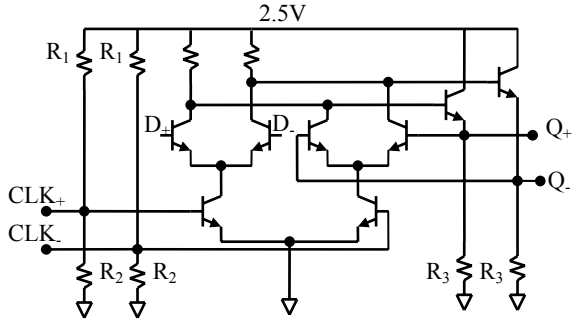

Fig. 5. Low-voltage D-latch used in 100GHz frequency divider.

IV. Measurement Results

The circuit blocks were fabricated in a 0.13μm SiGe HBT process (no MOSFETs) with several HBT profile splits with varied collector doping and emitter-base junction engineering. The SiGe HBT f_T/f_{MAX} for the technology splits are illustrated in Table 1. A die photo of the receiver, including LNA, VCO, and mixer with baluns and IF amplifier, is shown in Fig. 6. Measurement results are reported for wafer 5 (the "reference" split), except where explicitly indicated.

TABLE 1. TECHNOLOGY SPLIT PROCESS PARAMETERS.

Wafer #	f_T	f_{MAX}	Collector doping	EB Junction
5	250	290	Reference=C	Reference
3	245	280	C+	Reference
7	265	255	C++	Reference
2	260	240	C+++	Reference
6	275	275	C+	Scaled

A. Low-Noise Amplifier and Power Amplifier

The LNA gain (S_{21}) is shown in Fig. 10, measured at 1.8V/2.5V and 1.5V/1.8V supplies. The input return loss is shown in the same plot for different bias currents of the input transistor Q_1. The LNA gain was also measured over temperature, and over the wafer splits corresponding to Table 1, as illustrated in Fig. 11 and Fig. 12, respectively. The 3dB bandwidth extends from 81GHz to 90GHz with the highest gain of 25dB centered at 86GHz. Measured S_{11} and S_{12} are better than -20dB and -50dB, respectively. The measured OP1dB is +4dBm at 86GHz.Because a standalone down-converter was not available for W-band noise measurement, the LNA noise figure cannot be measured.

The saturated PA gain and output power were measured from 75-95GHz over temperature, as illustrated in Fig. 13, and, along with S_{11}, across the technology splits, as shown in Fig. 14 and Fig. 16. In Fig. 15, measurements at 77GHz show the PA achieves small-signal S_{21} of 19dB, saturated output power of +14.4dBm, an OP1dB of 12dBm, and PAE of 15.7% (based on 161mW P_{DC}). S_{11} and S_{22} in the PA remain below -10dB from 64-89GHz on all splits; S_{11} is illustrated in Fig. 16.

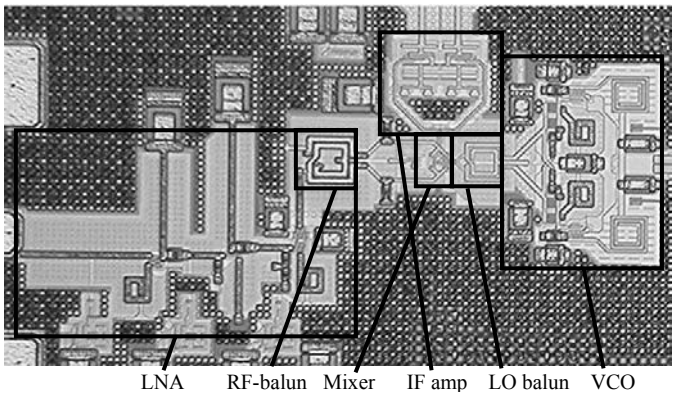

Fig. 6. Micro-photograph of the receiver including LNA, VCO, mixer, IF amplifier, RF-balun, and LO-balun (0.45mm × 0.30mm).

B. Voltage-Controlled Oscillator

The VCO provides +5dBm differential output power at 77GHz (measured using a power meter), a tuning range of 4GHz, and as shown in Fig. 7 has a phase noise for W-band VCOs of -101.6dBc/Hz at 1MHz offset, or approximately -99.1dBc/Hz with linear averaging.

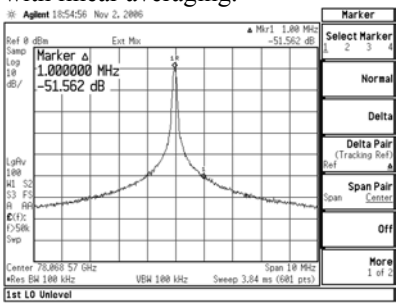

Fig. 7. VCO phase noise at 1MHz offset.

C. Mixer, Balun and IF amplifier

Depending on bias conditions, the mixer, with LO and RF baluns, achieves a differential to single-ended conversion gain of 8-11dB, and a noise figure of 12.5-14.5 dB for a -2dBm, 73GHz LO signal and a 1 GHz IF, as shown in Fig. 8 (a). The mixer noise figure is DSB but its value is pessimistic because the RF input of the mixer is broadband (50 GHz to 80 GHz) and multiple signal source harmonics (multiplier source) are present at the LO port of the mixer which have not been filtered out. The noise figure also includes the insertion loss of the transformer, larger than 2dB, at RF port of the mixer.

With a -2dBm LO signal at 77GHz, the OP1dB of the IF amplifier is +5dBm, as illustrated in Fig. 8 (b).

E. Static Frequency Divider

The static frequency divider achieves a self-oscillation frequency of 83.5GHz at 25ºC and 66.9GHz at 125ºC, the highest ever reported for a silicon frequency divider, while consuming a record low 75mW from a 2.5V supply. The previous silicon record was 76GHz at 25ºC and 122mW from 3.3V [8]. The divider operates correctly up to 99GHz, as illustrated in Fig. 9.

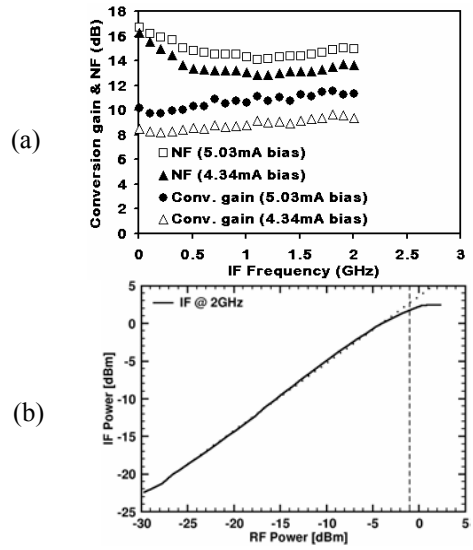

Fig. 8. (a) Mixer differential gain and NF for 73GHz, < -2dBm LO, and (b) single ended OP1dB for 70GHz, < -2dBm LO.

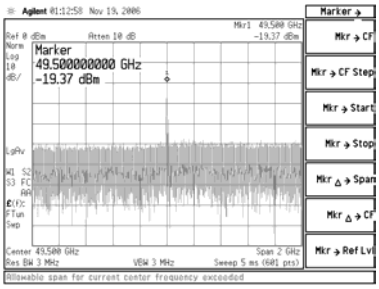

Fig. 9. Measured frequency divider spectrum for 99GHz input signal.

V. CONCLUSION

A state-of-the-art low-voltage, small form factor chipset for 77GHz automotive and imaging applications has been reported. Measured results indicate excellent performance for all circuit blocks across temperature and process at 1.8V/2.5V. Table 2 summarizes the expected performance of a 500mW, 77GHz transceiver made using the circuit blocks presented. Results also show that the LNA and PA gains closely track the HBT f_{MAX} across wafer splits. Wafer 5, with the highest f_{MAX}, shows the best overall circuit performance for all blocks.

TABLE 2. EXPECTED PERFORMANCE OF A 2.5V, 77GHZ TRANSCEIVER FABRICATED USING THE CIRCUIT BLOCKS PRESENTED.

Specification	Result	Notes
Receiver IP1dB (1GHz IF)	-33 dBm	– +5dBm OP1dB minus receiver conversion gain – With -2dBm 70GHz LO and (< -2dBm 77GHz LO)
Receiver conv. Gain (1GHz IF)	36 dB	
Receiver noise figure	5.4 dB	LNA NF sim. Mixer NF meas.
IF bandwidth	> 2GHz	LO: -2dBm, 73GHz
RF input bandwidth	9 GHz	-3dB bandwidth of LNA S_{21}
S_{11}/S_{22} matching	< -15 dB	Worst case for LNA and PA
Transmitter OP1dB	12 dBm	77 GHz meas.
Transmitter P_O sat.	14.6 dBm	77GHz meas. & PAE is 15.5%

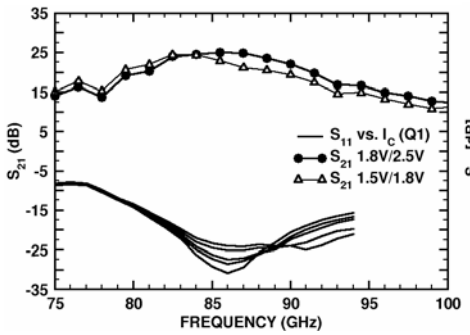

Fig. 10. LNA S-parameters over supply.

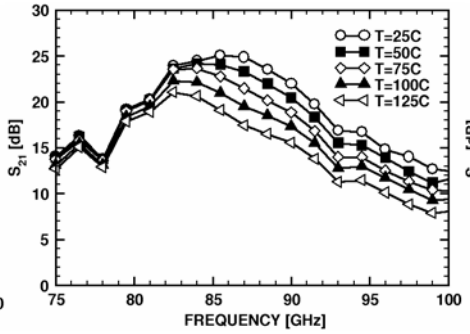

Fig. 11. LNA S_{21} over temperature.

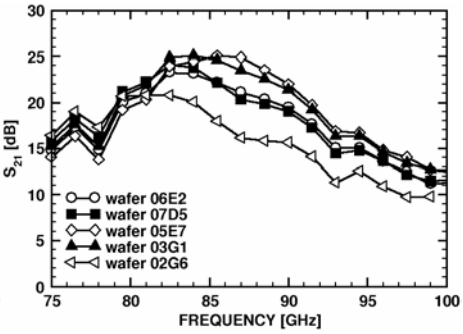

Fig. 12. LNA S_{21} for technology splits.

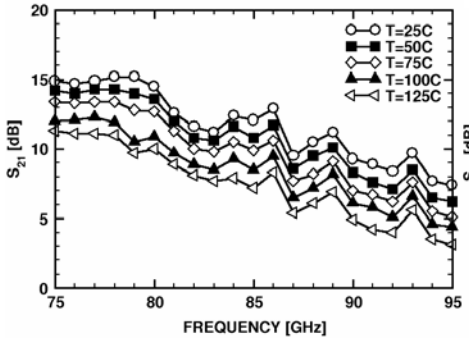

Fig. 13. PA gain over temperature.

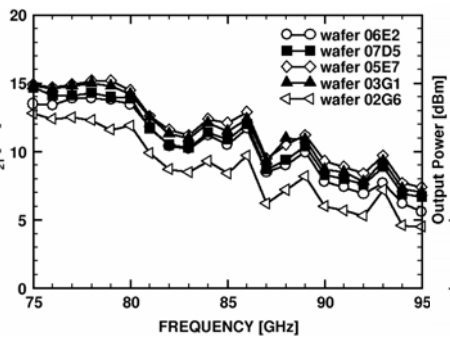

Fig. 14. PA gain across technology splits.

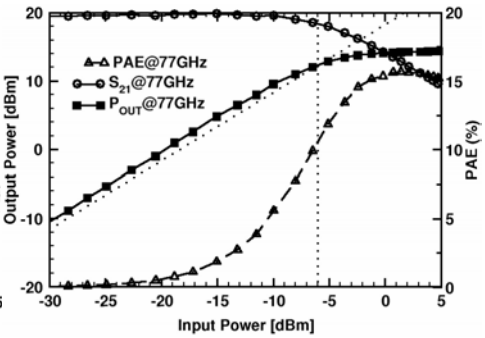

Fig. 15. PA S_{21}, OP1dB, and P_{SAT} at 77GHz

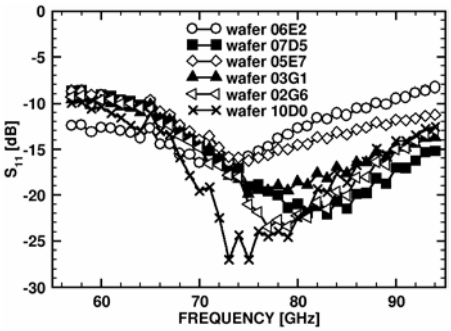

Fig. 16. PA Input return loss across technology splits.

ACKNOWLEDGEMENTS

The authors thank Alain Chantre and Rudy Beerkens for their support, CMC and especially Jaro Pristupa for CAD support, CITO and STMicroelectronics for funding.

REFERENCES

[1] P. Chevalier et al, "230-GHz Self-Aligned SiGe:C HBT for Optical and Millimeter-Wave Applications," IEEE JSSC, vol. 40, no. 10, pp. 2025-2034, Oct. 2005.

[2] Komijani, A. & Hajimiri, A., **"**A Wideband 77-GHz, 17.5-dBm Fully Integrated Power Amplifier in Silicon**,"** IEEE JSSC, vol. 41, pp. 1749 – 1756, Aug. 2006.

[3] Dehlink B. et al., "Low-noise Amplifier at 77 GHz in SiGe:C bipolar technology", *IEEE CSICS*, pp. 287, Oct. 2005.

[4] L. Wang, R. Kraemer, and J. Borngraeber, "An Improved Highly-Linear Low-Power Down-Conversion Micromixer for 77GHz Automotive Radar in SiGe Technology," IEEE MTTS (IMS), San Francisco, June 2006.

[5] J-J. Hung, J.M. Hancock, and G.M. Rebeiz, "A 77GHz SiGe Sub-Harmonic Balanced Mixer," IEEE JSSC, vol. 40,no. 11, pp. 2167-2173, Nov. 2005.

[6] Reuter R. and Yin Y., "A 77GHz (W-Band) SiGe LNA with a 6.2 dB Noise figure and Gain Adjustable to 33 dB", IEEE BCTM, Oct. 2006.

[7] S.T. Nicolson, K.H.K. Yau, P. Chevalier, A. Chantre, B. Sautreuil, and S.P. Voinigescu., "Design and Scaling of SiGe BiCMOS VCOs Operating near 100 GHz," *IEEE BCTM*, pp.142-145, Oct. 2006.

[8] E. Laskin, S.T. Nicolson, P. Chevalier, A. Chantre, B. Sautreuil, and S.P. Voinigescu. "Low-Power, Low-Phase Noise SiGe HBT Static Frequency Divider Topologies up to 100 GHz," *IEEE BCTM*, pp.235-238, Oct. 2006**.**

[9] S. T. Nicolson and S. P. Voinigescu, "Methodology for Simultaneous Noise and Impedance Matching in W-Band LNAs," *IEEE CSICS*, San Antonio, pp. 279-282, Nov. 2006.

[10] W. Mayer, M. Meilchen, W. Grabherr, P. Nuchter, and R. Guhl, "Eight-channel 77 GHz front-end module with high-performance synthesized signal generator for FM-CW sensor applications," *IEEE Trans. MTT*, vol. 52, no. 3, pp. 993-1000, Mar. 2004.

[11] Babakhani, A et al., **"**A 77-GHz Phased-Array Transceiver With On-Chip Antennas in Silicon: Receiver and Antennas" *IEEE JSSC*, vol. 41, no. 12, pp. 2795 – 2806, Dec. 2006.

[12] L. Wang, J. Borngraeber, and W. Winkler, "77 GHz Automotive Radar Receiver Front-end in SiGe:C BiCMOS Technology," *ESSCIRC* 2006, pp. 388-391, Sept. 2006.

[13] C. Wagner, A. Stelzer, and H. Jager, "PLL architecture for 77-GHz FMCW Radar Systems with Highly-Linear Ultra-Wideband Frequency Sweeps," *IMS 2006 Digest*, pp. 399-402, June 2006.

[14] B. Dehlick et al., "An 80 GHz SiGe Quadrature Receiver Frontend," *IEEE CSICS*, pp. 197-200, Nov. 2006.

[15] S.P. Voinigescu et al., "SiGe BiCMOS for Analog, High-Speed Digital and Millimeter-Wave Applications Beyond 50 GHz," *IEEE BCTM*, pp. 223-230, Oct. 2006.

[16] P. Chevalier et al., "Advanced SiGe BiCMOS and CMOS platforms for Optical and Millimeter-Wave Integrated Circuits," *IEEE CSICS*, pp. 12-15, Nov. 2006.

[17] M. Q. Gordon, T. Yao, and S.P. Voinigescu, "65-GHz Receiver in SiGe BiCMOS Using Monolithic Inductors and Transformers" *Si Monolithic ICs in RF Systems*, pp.265-268, Jan. 2006.

[18] H. Knapp, B. Dehlink, H.-P. Forstner, E. Kolmhofer, K. Aufinger, J. Bock, and T. F. Meister, "SiGe Circuits for Automotive Radar," *IEEE SiRF*, pp.231-236, Jan. 2007.

[19] B. Floyd, U. Pfeiffer, S. Reynolds, A. Valdes-Garcia, C. Haymes, Y. Katayama, D. Nakano, T. Beukema, B. Gaucher, and M. Soyuer, "Silicon Millimeter-Wave Radio Circuits at 60-100GHz," *IEEE SiRF*, pp. 213-218, Jan. 2007.