SP 22.5: 5.8GHz and 12.6GHz Si Bipolar MMICs

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Wireless ATM in the 5GHz band is the most recent addition to the family of multimedia applications. As in the case of lower-band and lower-speed wireless systems, the availability of low-cost silicon solutions is a prerequisite for its ubiquitous market presence. A family of circuits aimed at the wireless ATM and broadband multimedia applications is implemented in an implanted-base, double-poly Si bipolar technology. The process features bipolar transistors with f_T and f_{MAX} values of 24GHz and 38GHz, respectively at V_{CE}=1V. The minimum noise figure, NF_{MIN}, is typically 2dB at 5.5GHz, while BV_{CEO} and BV_{CBO} are 4.2V, and 15V, respectively. The three-layer metallization with 2μm thick Al top layer allows for fabrication of inductors with Qs in the 6-10 range and microstrip and coplanar lines with Qs of 6 at 26GHz.

The circuit schematics for the 5.8GHz double-balanced mixer and low-noise amplifier (LNA), and for the broadband 7.1GHz and 12.6GHz Darlington amplifiers are shown in Figure 1. They feature on-chip inductors and are designed using a subcircuit-based, scalable Spice-Gummel-Poon (SGP) model, as well as a physical inductor model [1, 2]. Only one of the 6 transistor sizes employed in the designs had been measured before the circuits were fabricated. The design relies on the scalable SGP model to accurately predict the optimum size of each transistor as required to maximize circuit performance.

The LNA and the double-balanced mixer, intended for a 5.8GHz down-converter, are simultaneously matched for optimum noise and input impedance at the RF port [1]. A cascode configuration is employed with the input transistor as a low-noise amplifier and the common base stage for mixing/input-output buffering. The mixer features an LO-reject, series LC filter at the differential IF output, and a parallel LC resonator, tuned on the second RF harmonic, as an ac current source in the emitter of the input transistor pair [2]. Inductors, L_E, are used for emitter degeneration in lieu of resistors, alleviating to a large degree the trade-off between the input third-order intercept point, IIP3, and the noise figure. However, since IIP3 is proportional to $\omega g_m L_E$, and since for ideal input match $L_E=Zo/2\pi f_T$, IIP3 and input matching become intertwined (IIP3 ~ $\omega g_m Zo/2\pi f_T$). In IC implementations Zo can be changed from 50Ω to meet the IIP3 goal. In these circuits Zo is 50Ω to facilitate on-wafer measurements.

Noise matching is by selecting the proper transistor size, rather than with matching circuitry that, even with Qs of 10, significantly degrades the overall noise figure [1]. The transistor size for optimal noise match depends on operating frequency and bias current density. In the LNA, a 2x0.5x20μm² device, biased at a minimum noise current of 1.8mA, is used. It can be demonstrated that the minimum noise figure of a differential stage is identical to that of the corresponding half-circuit, and that the optimum noise impedance is two times larger. As a result, the 4x0.5x20μm² size and 4mA bias current of the input transistor pair in the double-balanced mixer are two times larger than those of the input transistor of the LNA. Both circuits, LNA and double-balanced mixer, are simultaneously noise and input impedance matched to 50Ω. To maximize gain and bandwidth, the size of the transistors in the mixing quad is chosen 8 times smaller than that of the input pair. The size ratio corresponds to the ratio of the peak-f_T current density to the minimum-noise current density. A similar technique in dimensioning the common base transistor in the LNA increases the gain by 1-2dB. Figure 2 summarizes the on-wafer measured performance of the 5.8GHz LNA. In the version without the input inductor on-chip, the noise figure improves from 4.2dB to 3.8dB. The IIP3 is -4dBm. The measured characteristics of the 5.8GHz double-balanced mixer are shown in Figure 3. The RF-port return loss is verified by S parameter measurements. (The mixer is biased as an amplifier with dc LO inputs only.) The conversion gain, measured with a spectrum analyzer, is 14dB at an IF of 300MHz. The double-sideband noise figure has a minimum of 4.2dB at an IF of 400MHz and the IIP3 is -2dBm.

The scalable model is also applied to the 16dB gain, 7.1GHz bandwidth, and 8dB gain, 12.6GHz bandwidth Darlington amplifiers. The size of the output transistor, Q2, meets the output compression point specification. The length of the input transistor, Q1, is optimized to reduce the group delay ripple within the 3dB bandwidth. Varying the emitter length controls the base resistance without degrading either f_T or f_{MAX}. In this manner, the Q of the resonant circuit associated with the negative resistance of the emitter follower is reduced below 0.71 [4]. The series and shunt feedback resistors, R_{E1}, R_{E2}, R_F, meet the gain and low-frequency input match specification. On-chip input inductors, L_{in}, improve the input return loss at high frequencies. Measured performance is summarized in Figures 4 and 5 for the 12.6GHz and 7.1GHz amplifiers, respectively. The output compression point is 9dBm at 8GHz for the 12.6GHz amplifier, and 12dBm at 5GHz for the 7.1GHz amplifier, respectively.

The circuits occupy 2x1mm². Metal-1 ground planes and 50Ω microstrip M3-to-M1 lines are used extensively. Figure 6 is a chip micrograph.

References:

[1] Voinigescu, S., et al., "A Scalable High Frequency Noise Model for Bipolar Transistors with Application to Optimal Transistor Sizing for Low-noise Amplifier Design," BCTM Proceedings, pp.61-64, Sept., 1996.

[2] Long, J., M. Copeland, "Modeling, Characterization and Design of Monolithic Inductors for Silicon RFICs," CICC Digest, pp.185-188, May, 1996.

[3] Brunel, A., et al., "A Downconverter for Use in a Dual-Mode AMPS/CDMA Chip Set," Microwave J., pp.20-42, Feb., 1996.

[4] Snelgrove, M., *VLSI Circuits*, lecture notes, Carleton University, Ottawa, pp.420-425, 1994.

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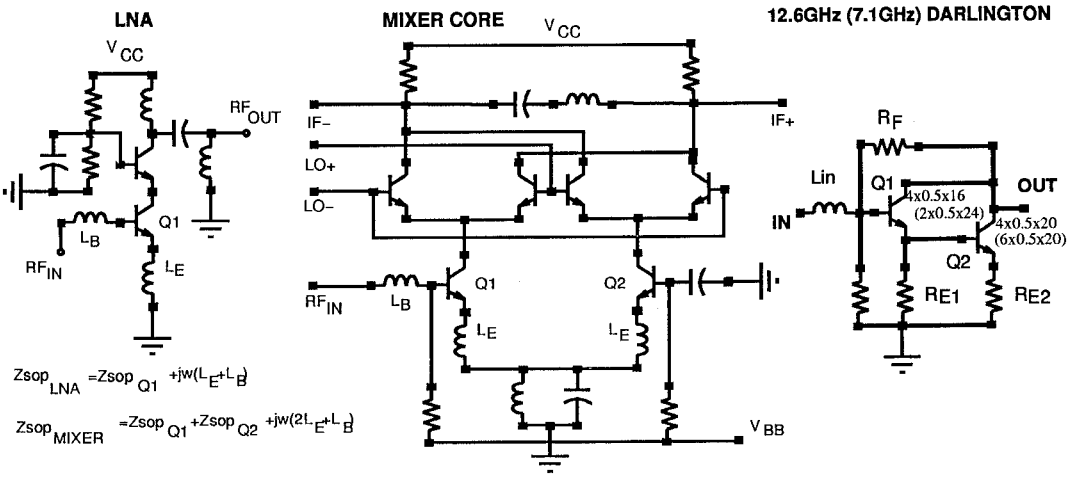

Figure 1: Circuits schematics.

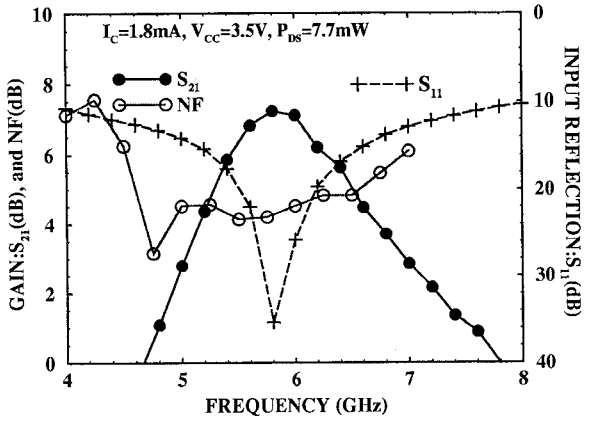

Figure 2: Measured LNA performance.

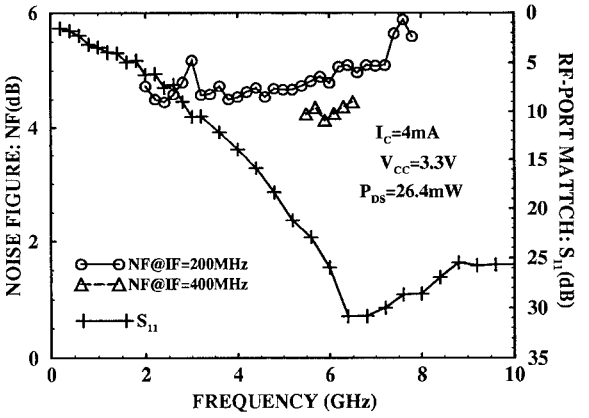

Figure 3: Measured mixer performance.

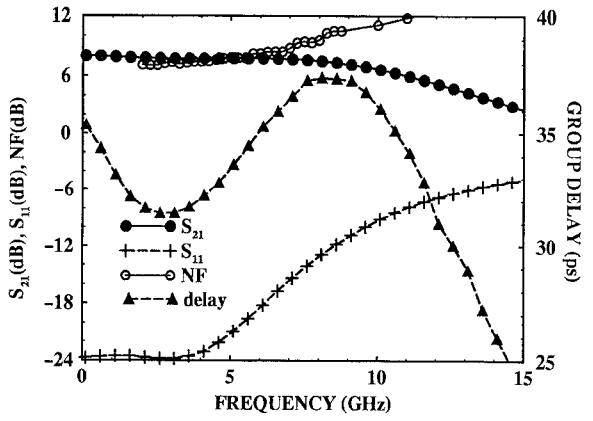

Figure 4: 12.6GHz Darlington amplifier performance.

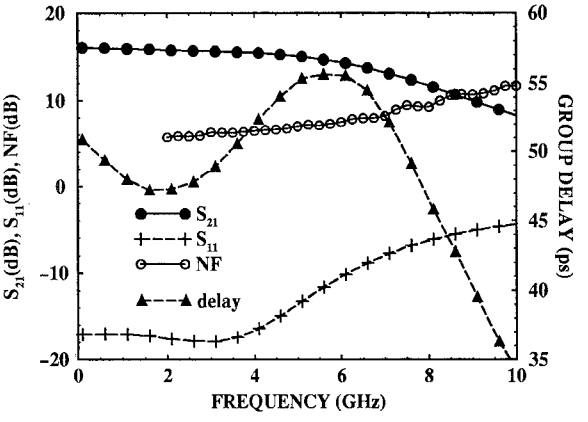

Figure 5: 7.1GHz Darlington amplifier performance.

Figure 6: See page 488.

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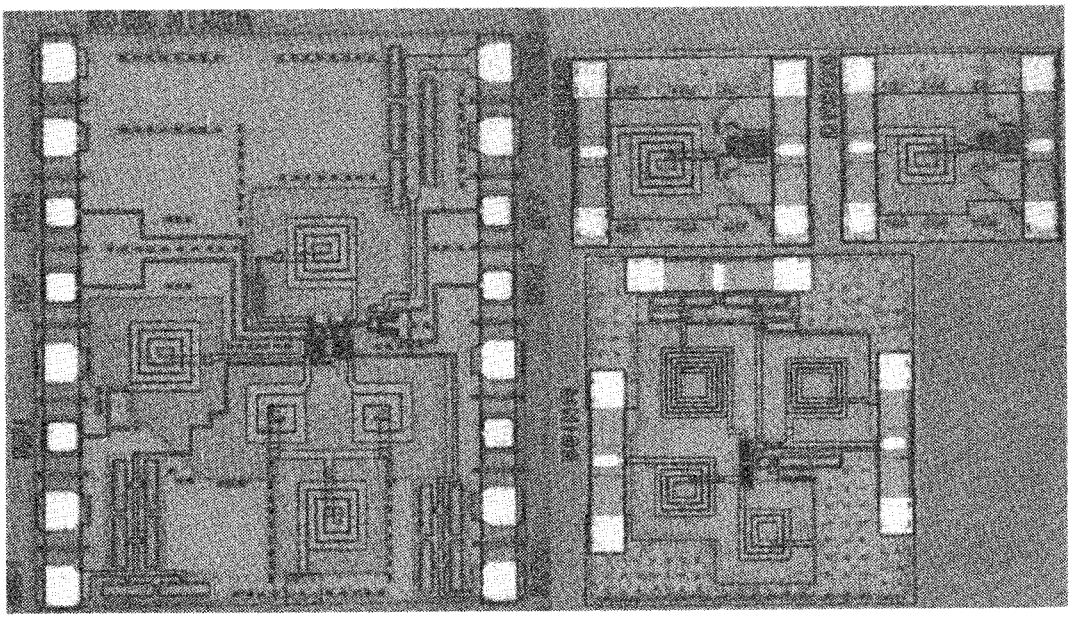

Figure 6: Chip micrograph.

SP 22.6: High Dynamic Range Variable-Gain Amplifier for CDMA Wireless Applications

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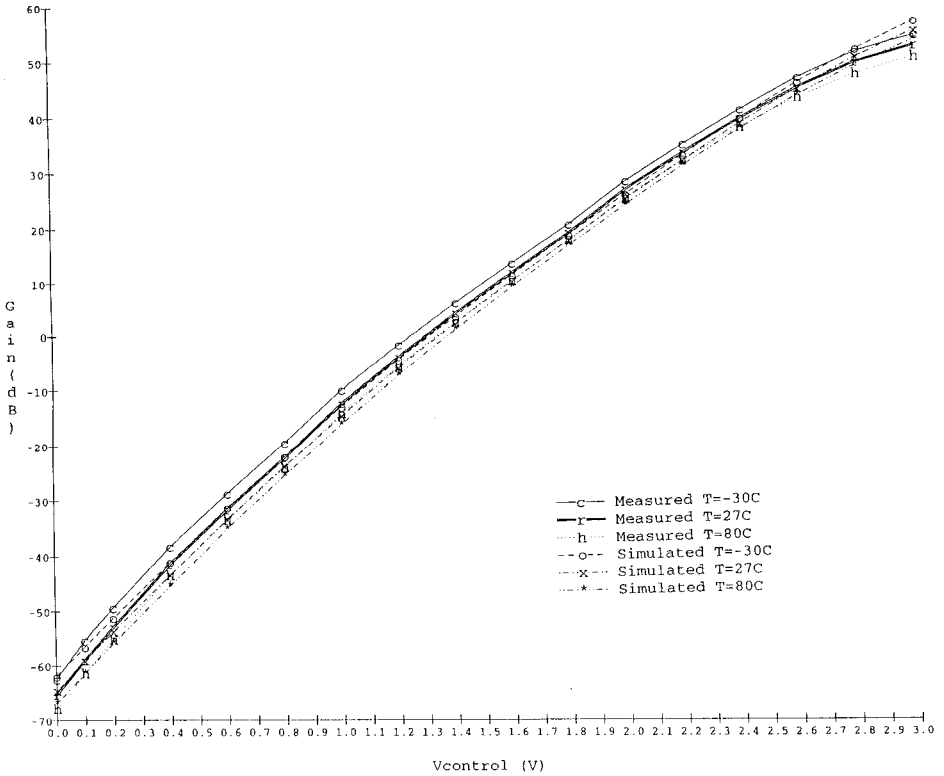

Figure 5: Rx VGA IIP3 and noise figure vs. gain.