6-kΩ 43-Gb/s Differential Transimpedance-Limiting Amplifier With Auto-Zero Feedback and High Dynamic Range

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***Abstract*—A high-gain, 43-Gb/s InP HBT transimpedance-limiting amplifier (TIALA) with 100-μA_{pp} sensitivity and 6 mA_{pp} input overload current is presented. The circuit also operates as a limiting amplifier with 40-dB differential gain, better than 15-dB input return loss, and a record-breaking sensitivity of 8 mV_{pp} at 43 Gb/s. It features a differential TIA stage with inductive noise suppression in the feedback network and consumes less than 450 mW from a single 3.3-V supply. The TIALA has 6-kΩ (76 dBΩ) differential transimpedance gain and 35-GHz bandwidth and comprises the transimpedance and limiting gain functions, an auto-zero dc feedback circuit, signal level monitor, and slicing level adjust functions. Other important features include 45-dB isolation and 800-mV_{pp} differential output.**

***Index Terms*—Auto-zero dc feedback, broadband low-noise amplifier, differential topology, InP heterojunction bipolar transistor (HBT), limiting amplifier, minimum noise figure, OC-768, peak detector, transimpedance amplifier (TIA), transistor sizing for minimum broadband noise, transmission lines.**

I. Introduction

IT HAS BEEN demonstrated recently that it is possible to integrate the transimpedance and limiting amplifier (TIALA) functions on a single die [1]–[4]. In 40-Gb/s implementations, such an amplifier has to cover a wide dynamic range from 100 μA_{pp} to 4 mA_{pp} [4]. In order to drive serializer–deserializer (SERDES) chips with typical sensitivities of 50 mV_{pp} and to account for PCB and connector losses, a minimum output swing of at least 100 mV_{pp} per side must also be achieved, resulting in a minimum single-ended gain of 1 kΩ per side or 2 kΩ differential.

This paper describes an InP HBT TIALA with functionality, sensitivity, gain, power dissipation, and integration levels so far unparalleled in 40-Gb/s designs [4]–[6]. Since its input and optimal noise impedance are close to 50 Ω up to 50 GHz, it also operates as a low-noise limiting amplifier (LA) or low-noise broadband voltage preamplifier. Such performance was made possible by a noise- and bandwidth-optimized differential TIA stage with resistive as well as inductive feedback, by the choice of auto-zero dc feedback topology and by employing special on-chip input-to-output isolation techniques. Furthermore, it is demonstrated analytically that, for typical capacitance values encountered in PIN photodiodes operating at 10 Gb/s [3] and 40 Gb/s, it is possible to design the TIA stage such that its input equivalent noise current is minimized when driven by a photodiode, while being concomitantly noise- and input impedance-matched to 50 Ω. The latter allows the TIALA to be operated as a limiting amplifier with better sensitivity and noise than traditional limiting amplifier topologies.

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II. Circuit Design

A. System Architecture

The block diagram, shown in Fig. 1, features a differential TIA stage with 270-Ω transimpedance gain per side, a multistage limiting amplifier, an auto-zero dc feedback amplifier, and an output buffer with an adjustable swing and a gain of 2. The choice of a differential TIA stage was dictated by power-supply-noise rejection and stability considerations. Although the conventional use of this circuit is to drive the DIN input with the photodiode and to ac-ground the other input, it should be noted that it is also possible to employ it in a BPSK application where the inputs are driven by two out-of-phase photodiodes. In the former case, a slicing level adjustment signal can be applied on the ac-grounded input pad. Furthermore, while the main design goal was to optimize the performance of the circuit as a low-noise, high-gain, and high-dynamic-range TIA, it was realized, based on input and noise impedance analysis, that the TIALA could also be operated as a low-noise, 50-Ω-matched, single-ended limiting amplifier. By setting the single-ended power gain of the main path to be 34 dB (40 dB differential), the output signal becomes limited at input signals as low as 120 μA_{pp} or 8 mV_{pp}.

B. TIA Stage

The schematic of the TIA stage is shown in Fig. 2. Low-noise performance is the prime consideration in the design of this stage. First, resistors rather than current sources are employed to bias the transistors in the feedback network. Resistors are known to contribute less noise than current sources and should therefore be preferred. Second, the size, 1 $\mu m \times 5$ μm, and bias current density of the input transistors in the TIA stage are optimized in an effort to reduce the input noise current while ensuring that a small-signal bandwidth of at least 36 GHz is maintained

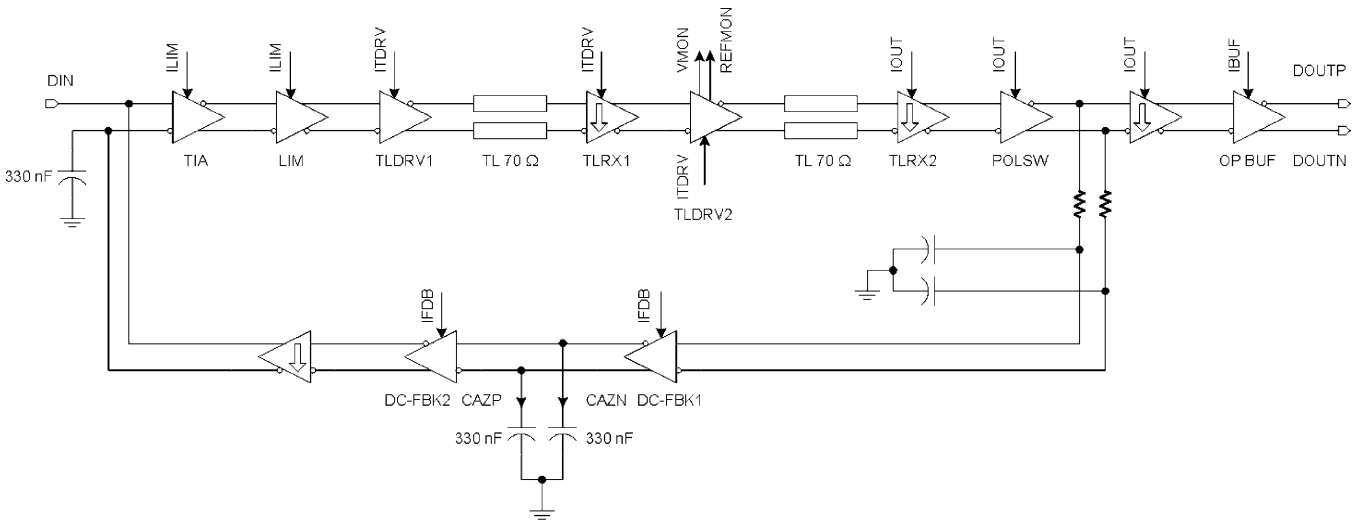

Fig. 1. Block diagram of the TIALA with single photodiode input. The unused TIA input is ac-coupled to ground in order to reduce noise. Emitter-follower stages are identified by a downward pointing arrow.

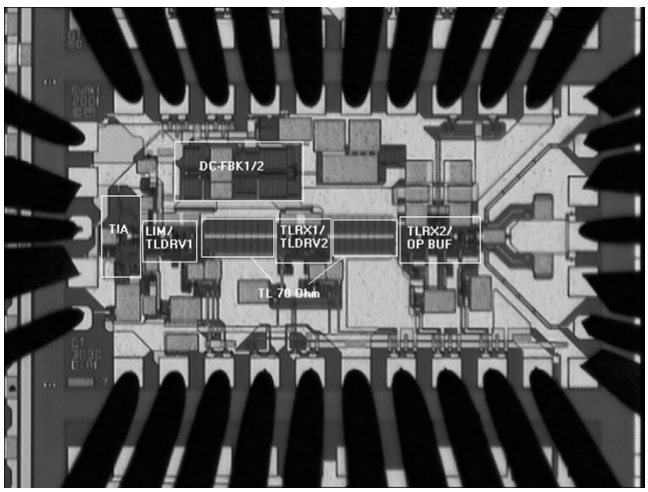

Fig. 2. Differential TIA stage schematic.

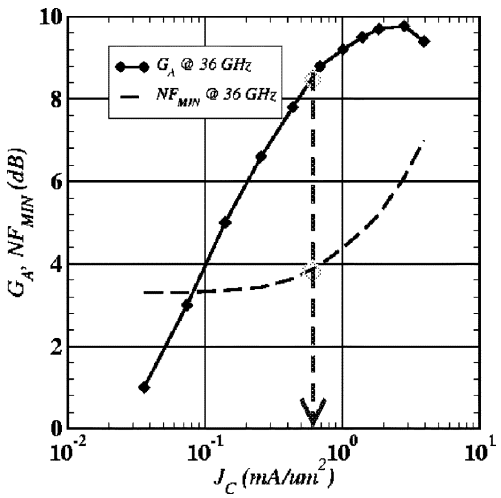

Fig. 3. Simulated $NF_{\rm MIN}$ and G_a versus I_c characteristics of a 1×5 μm^2 InP HBT biased at $V_{\rm CE} = 1$ V.

over process and temperature corners. Third, by placing the inductor L_f in the feedback network, the input-referred noise contribution of the feedback resistor R_f is reduced by a factor of $1 + (\omega L_f R_f)^2$. At the same time, the input return loss and small-signal bandwidth are improved because the inductor also tunes out part of the PIN photodiode capacitance and of the input capacitance of the amplifier. In order to further reduce the equivalent input-referred noise, the transimpedance feedback resistor R_f should be maximized. However, the bandwidth requirement imposes an upper bound of about 300 Ω on its value.

The biasing and sizing of the InP HBTs in the input differential pair is discussed in more detail next. Fig. 3 shows the simulated minimum noise figure $NF_{\rm MIN}$ and the associated power gain G_a at 36 GHz for a 1 μm × 5 μm InP HBT transistor, as a function of the collector current, and illustrates the tradeoff that exists between noise and gain when biasing the input differential pair. Even though the associated gain peaks at the same current density as the cutoff frequency f_T, about 2 mA/μm^2, the optimal noise current density is only 0.1 mA/μm^2, which is significantly lower than in SiGe HBTs or Si MOSFETs. Based on this information, the size of the transistors in the TIA stage was optimized by simulation in order to minimize the input equivalent noise current while maintaining a constant current density of 0.66 mA/μm^2. The simulated input equivalent noise of the entire TIALA and its strong dependence on the input bond wire inductance L_b are depicted in Fig. 4. The impact of the photodiode's 60-fF capacitance and 15-Ω series resistance is included in these simulations. For a 350-pH bond wire, the input noise current remains lower than 27 pA/$\sqrt{\rm Hz}$ up to 40 GHz. These results indicate that, even for OC-768 applications, one can take advantage of the bondwire inductance between the photodiode and the TIALA to improve the overall system sensitivity of the receiver by significantly reducing the input noise current above 20 GHz. While other considerations may drive photodiode–TIA integration, eliminating bondwire inductance should not be one of them.

The methodology described above ensures that the sensitivity of the TIALA is maximized when it is driven by a photodiode. In order to study the sensitivity of the TIALA when operated as

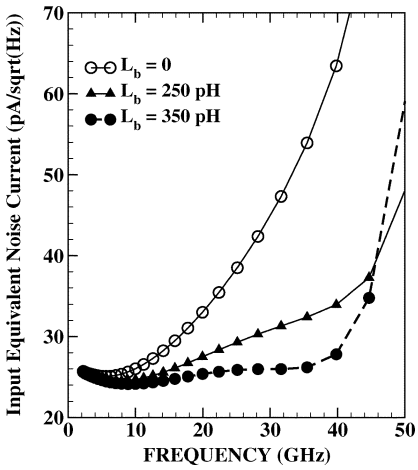

Fig. 4. Equivalent input noise current and gain simulation of the TIALA.

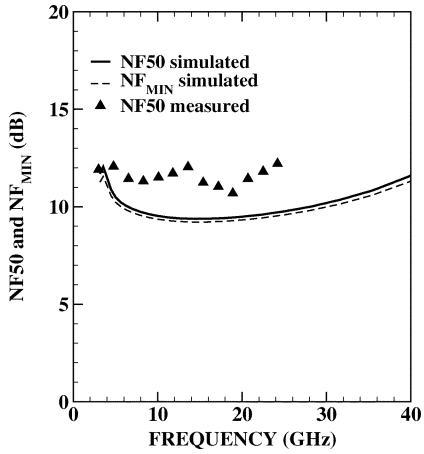

Fig. 5. Simulated and on-wafer measured 50-Ω noise figure, and simulated minimum noise figure of the TIALA. The bondwire inductance is not present in either simulations or measurements.

a limiting amplifier in a 50-Ω environment, one can derive the expression of the noise figure of the TIA half-circuit. By treating the half-circuit as an amplifier with parallel feedback consisting of the the series combination of the feedback resistor R_f and feedback inductor L_f, the expression of the noise factor F as a function of the source impedance Z_0, the minimum noise factor $F_{\rm MIN}$, as well as the optimum noise conductance G_{sop}, of the half-circuit are derived as a function of the feedback elements and of the transistor noise admittance parameters G_{nt}, R_{nt}, and Y_{cort} [7], [8]:

$$F(Z_0) = 1 + R_{nt}Z_0\left|Y_{cort} + \frac{1}{Z_0} + \frac{1}{R_f}\frac{1-j\omega_0}{1+\omega_0^2}\right|^2 + G_{nt}Z_0 + \frac{Z_0}{R_f(1+\omega_0^2)} \quad (1)$$

$$G_{sop} = \sqrt{\left[G_{cort} + \frac{1}{R_f(1+\omega_0^2)}\right]^2 + \frac{G_{nt}}{R_{nt}} + \frac{1}{R_f R_{nt}(1+\omega_0^2)}} \quad (2)$$

$$F_{\min} = 1 + 2R_{nt}\left[G_{cort} + G_{sop} + \frac{1}{R_f(1+\omega_0^2)}\right] \quad (3)$$

where $\omega_0 = \omega L_f/R_f$.

For a given technology and bias point, the transistor noise parameters scale with the emitter length l_E [7]:

$$G_{nt} = G(2\pi f)^2 l_E \qquad R_{nt} = \frac{R}{l_E}$$
$$G_{cort} = 2\pi G_C l_E \qquad B_{cort} = 2\pi f B l_E \quad (4)$$

where G [$\Omega^{-1}*\text{rad}^{-2}*\mu\text{m}^{-1}$], R [$\Omega*\mu$m)], G_C [$\Omega^{-1}*\text{rad}^{-1}*\mu\text{m}^{-1}$], and B [$\Omega^{-1}*\text{rad}^{-1}*\mu\text{m}^{-1}$] are technology constants which depend on the bias current density. By rearranging the terms in (1), the following equation (5) results:

$$\frac{F(Z_0)-1}{Z_0} = R_{nt}\left|Y_{cort} + \frac{1}{Z_0} + \frac{1}{R_f}\frac{1-j\omega_0}{1+\omega_0^2}\right|^2 + G_{nt} + \frac{1}{R_f(1+\omega_0^2)}. \quad (5)$$

By differentiating (5) with respect to the emitter length, one can find the minimum of the right-hand side of (5) as a function of the transistor length at $BW_{3\rm dB}$. The optimal transistor size l_{Eopt} that minimizes the noise figure over a broad band extending up to the 3-dB bandwidth of the amplifier, $BW_{3\rm dB}$, is

$$l_{Eopt} = \frac{1}{2\pi f}\left[\frac{1}{R_f(1+\omega_0^2)} + \frac{1}{Z_0}\right]\sqrt{\frac{R}{\frac{G}{R} + G_C^2 + B^2}}. \quad (6)$$

Similarly, the optimal transistor size, resulting in the lowest input equivalent noise current, can be derived for the case when the TIALA is driven by a photodiode with capacitance C_D

$$l_{Eopt} = \frac{1}{2\pi f}\sqrt{\left[\frac{1}{R_f^2(1+\omega_0^2)^2} + \frac{1}{(2\pi f C_D)^2}\right]} \times \sqrt{\frac{R}{\frac{G}{R} + G_C^2 + B^2}}. \quad (7)$$

Equations (6) and (7) are remarkably similar and indicate that if R_f is significantly larger than Z_0, which is typically the case for TIAs operating at 10 Gb/s and 40 Gb/s, similar values are obtained for the optimum emitter length if $Z_0 = 1/(2\pi f C_D)$. Interestingly, if the 20-fF pad capacitance on the InP substrate is added with the 60-fF diode capacitance, their equivalent impedance at 40 GHz is exactly 50 Ω. The same is roughly true at 10 GHz for photodiodes with 200–300-fF capacitance (including parasitics) and for 50-fF pads on Si substrates.

The preceding analysis and numerical example suggest that it is possible to design 50-Ω noise and input impedance-matched TIALAs that can simultaneously be operated as high-sensitivity TIAs and LAs. In confirmation, Fig. 5 shows the simulated minimum noise figure and the TIALA noise figure when driven by a 50-Ω source. NF and $NF_{\rm MIN}$ are nearly identical up to 40 GHz, demonstrating that the optimum noise impedance of the TIALA is close to 50 Ω, even though only the equivalent input noise current was optimized in the design of the TIA stage. Unlike the equivalent input noise current, the noise figure is negligibly affected by a change in bondwire inductance from 0 to 350 pH. On-wafer measurements of the 50-Ω noise figure, performed up to 24 GHz using an Agilent N8975A NFA Series noise figure analyzer with an NC346E noise source, are also

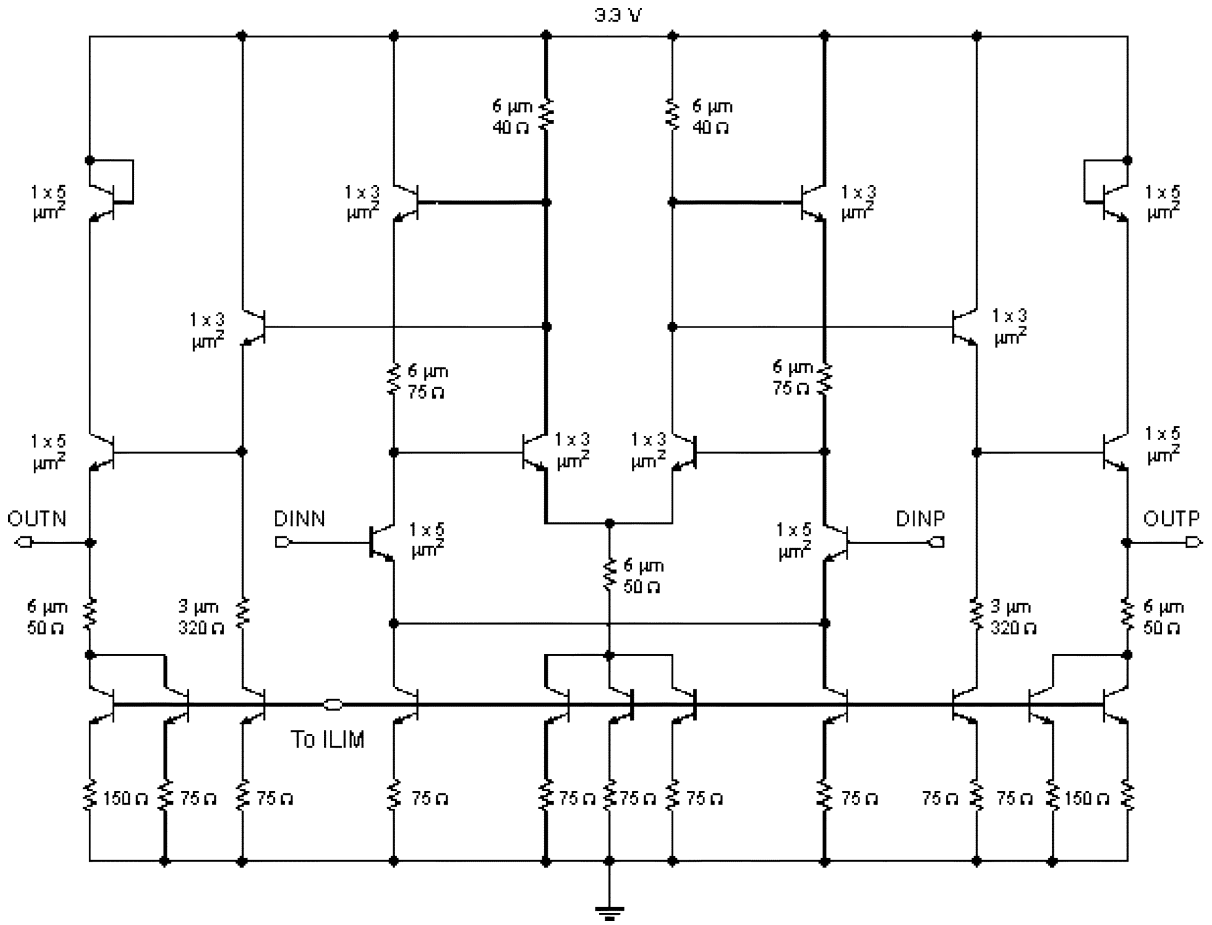

Fig. 6. Differential LA stage schematic.

plotted alongside the simulated noise figure. The measured data, varying between 11 and 12 dB, are 1–2 dB higher than simulation results. The reasons for this discrepancy are currently being investigated.

C. Limiting Amplifier and Output Stage

The limiting amplifier block consists of a Cherry–Hooper stage, shown in Fig. 6, followed by a chain of emitter-follower and inverter stages, as illustrated in the block diagram of Fig. 1. The inverters also act as drivers (TLDRV1/TLDRV2) for two differential transmission line sections that are employed to ensure good isolation between the analog (input) and digital (output) portions of the die. The characteristic impedance of the transmission lines is 70 Ω per side, which represents a compromise between power dissipation and bandwidth. Diode-connected transistors are inserted where appropriate to ensure that the collector-emitter voltage of the InP HBTs remains below 1.5 V. The peak switching current density in the Cherry–Hooper and in each inverter stage is set to 2 $\mathrm{mA}/\mu\mathrm{m}^2$, the lowest value that still allows for the maximum data rate of 45 Gb/s to be achieved for all process, bias, and temperature corners while maintaining excellent reliability.

A signal level peak detector, which operates in linear mode for most of the input current range, is implemented in the second transmission line driver, whose schematic is reproduced in Fig. 7. The peak detector is used for aligning the fiber to the photodiode. It operates on the principle that the common emitter point of the differential pair increases as a function of the applied differential signal level. The common emitter voltage is amplified by the common base transistor on the MON branch, low-pass filtered, and provided externally for fiber alignment as a dc difference voltage between the pads MON and REFMON.

The output stage, shown in Fig. 8, relies on a cascode topology. The output swing is adjustable between 200 $\mathrm{mV_{pp}}$ and 400 $\mathrm{mV_{pp}}$ per side. Since a cascode stage biased with a relatively large current is potentially unstable, resistive padding in the emitters of the common-emitter, and in the base of the common-base transistors, is employed in order to compensate for any negative resistance that might arise in either common mode or differential mode.

D. Auto-Zero DC Feedback Amplifier

The auto-zero dc feedback effectively cancels any systematic or input current-induced dc offset for the entire range of input photodetector currents. It must only be active below the low-frequency cutoff of a SONET system, which is typically 70 kHz. The high gain and the noise contribution of the auto-zero dc feedback amplifier pose a significant design challenge. To increase its effectiveness, the output of the auto-zero feedback is injected differentially in the TIA stage at nodes *FDBP* and *FDBN* (Fig. 2). Its noise contribution to the input of the TIA

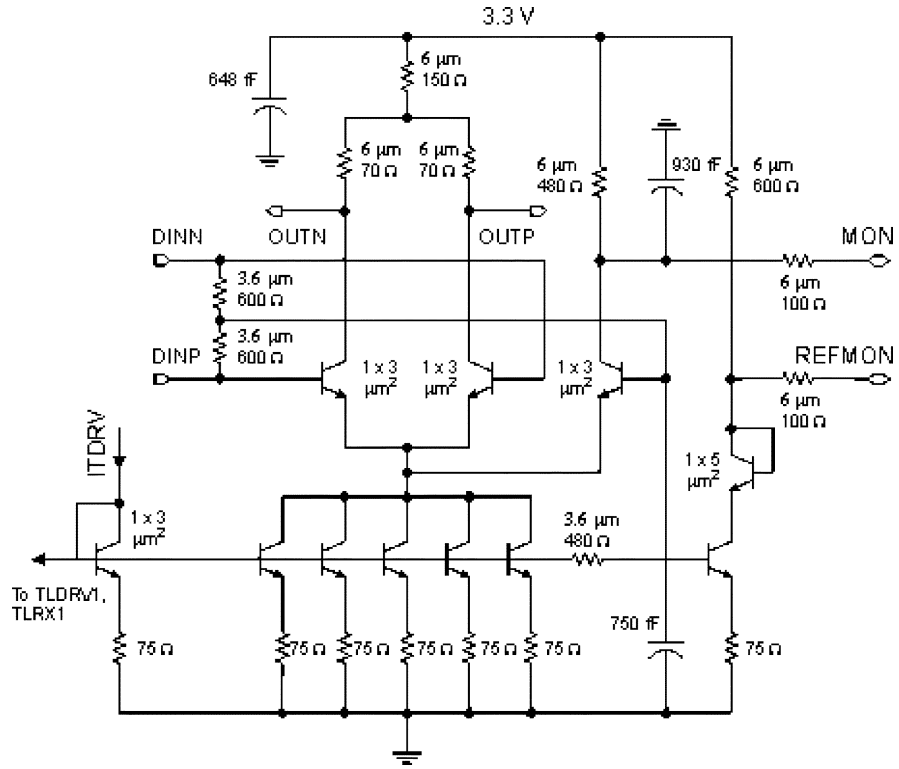

Fig. 7. Peak detector stage schematic and 70 Ω transmission line driver.

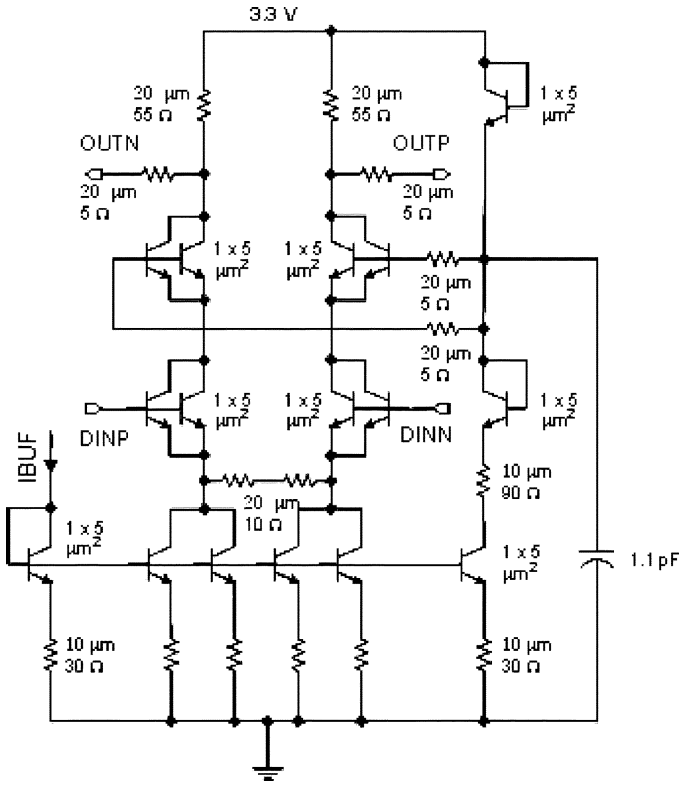

Fig. 8. Differential output stage schematic.

is thus reduced by RC-filtering. The feedback amplifier, shown in Fig. 9, is implemented with two cascaded inverters and two emitter-follower stages. The latter ensure that the appropriate dc level is provided to the differential TIA stage. The gain of the dc feedback amplifier was derived from the duty-cycle-distortion requirement. At the maximum input current level (6 $\mathrm{mA_{pp}}$ or 3 mA average in this case), the differential dc output offset should be lower than ± 60 mV, i.e., 10% of the nominal differential output swing. Over 50 pF of on-chip and 330 nF external capacitors are needed to ensure stability, $1/f$ noise suppression, and the low-frequency bandwidth of 70 kHz.

III. Fabrication

The circuit was fabricated in HRL Laboratories' InP SHBT process with typical f_T and $f_{\max}$ of 160 GHz. The substrate thickness is 100 μm. The process features two metal layers, 50 Ω/sq thin film resistors, and MIM capacitors. The microphotograph of the 1.0×1.8 $\mathrm{mm^2}$ differential TIALA die is shown in Fig. 10. The circuit draws 140 mA from a single 3.3 V supply and has 200 HBTs, two inductors, and 40 MIM capacitors. The latter are employed for bias de-coupling and low-pass filtering in the auto-zero dc feedback circuit. All transmission lines are implemented as uncoupled differential grounded coplanar waveguides.

IV. Measurement Results

The input current range and the output offset were verified by sweeping the input with a dc current up to 3 mA, corresponding to a maximum data current of 6 $\mathrm{mA_{pp}}$. As illustrated in Fig. 11, the measured differential output offset remains less than 40 mV, demonstrating the proper operation of the auto-zero dc feedback.

The high gain and isolation of the amplifier stretch the limits of the dynamic range of the network analyzer when

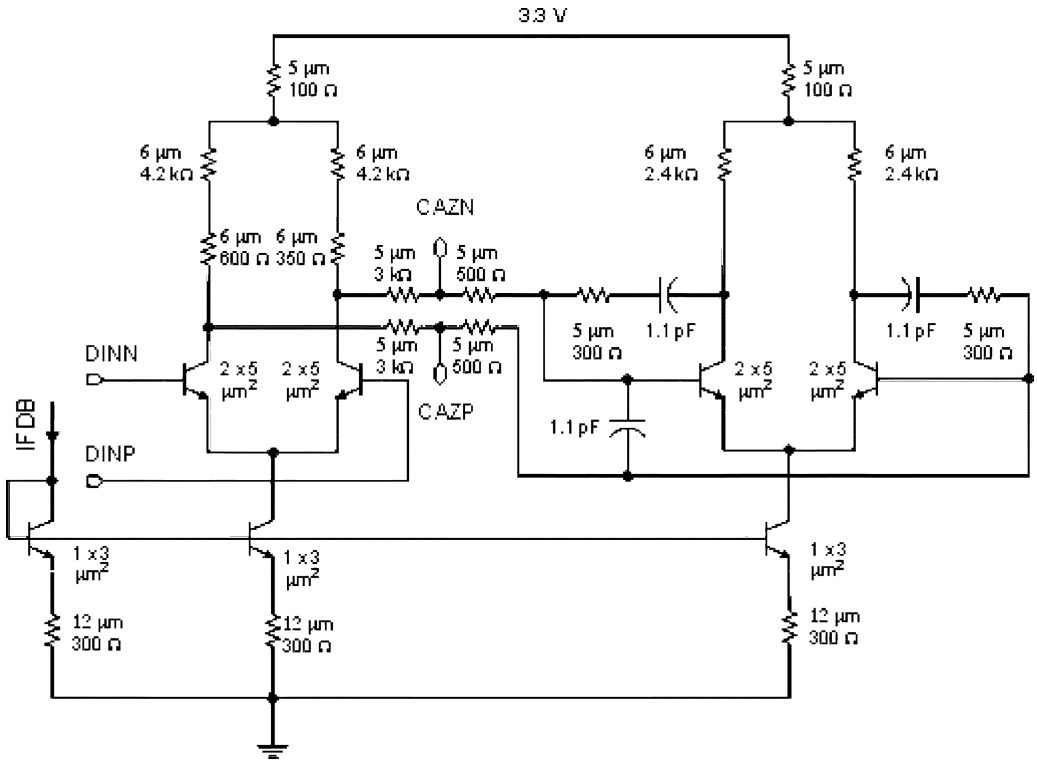

Fig. 9. Differential auto-zero dc feedback amplifier stage schematic.

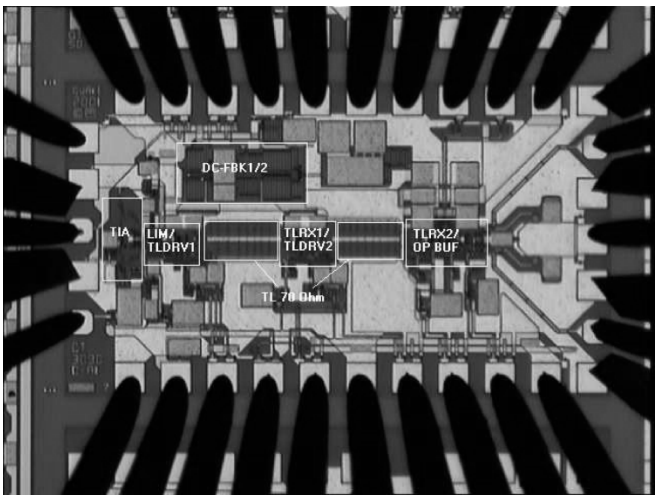

Fig. 10. Microphotograph of the TIALA with HF wafer probes.

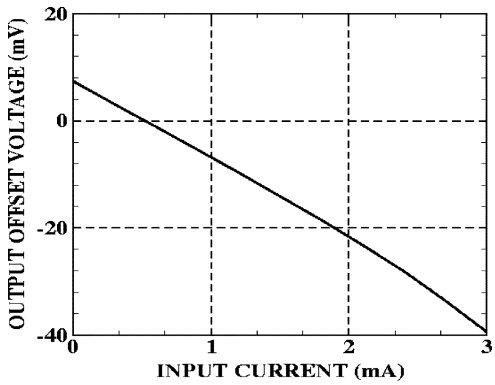

Fig. 11. Measured dc output offset as a function of dc input current.

performing S-parameter measurements. The on-wafer calibration is performed with a −15 dBm input signal. The actual TIALA measurements are next carried out by setting the input attenuator of the network analyzer to the 50 dB level. This technique results in noisier measurements than for lower gain amplifiers but ensures that the TIALA remains in linear mode. Fig. 12 presents the on-wafer measured power gain S_{21}, input and output reflection coefficients S_{11}, S_{22}, as well as the isolation, S_{12}, of the differential TIALA. S_{11}, S_{22}, and S_{12} are lower than −15, −10, and −45 dB, respectively, up to 50 GHz. The small-signal and large-signal power gains, measured with −65 dBm and −25 dBm input power levels, respectively, are also plotted in order to illustrate the 3-dB bandwidth expansion as gain limiting occurs. The small-signal 3-dB bandwidth of the TIALA is larger than 35 GHz while the small-signal power gain exceeds 34 dB per side. The measured input resistance, averaging 65 Ω, and the single-ended Z_{21} (76 dBΩ) are shown in Fig. 13. By accounting for the voltage division due to the on-chip and off-chip 50-Ω resistances at the output of the TIALA, the corresponding small-signal transimpedance gain is 70 dBΩ per side or 76 dBΩ differential.

The unloaded Z_{21} of the TIA stage was measured on a separate test structure and is reproduced with symbols in Fig. 14. The measurements and simulations performed on the TIA test structure provide insight into the impact of the estimated LA loading, PIN photodiode capacitance, and bondwire inductance on the bandwidth of the linear TIA stage. There is good agreement between the simulated (solid line) and measured (symbols) $Z_{21}(f)$ characteristics of the

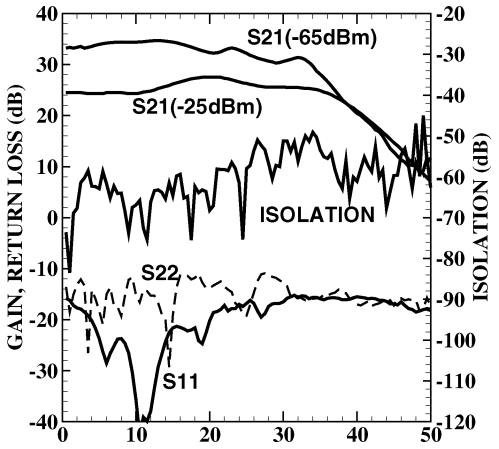

Fig. 12. On-wafer input/output return loss, isolation, small-signal (with −65 dBm input signal) and large-signal (−25-dBm input signal) single-ended TIALA power gain.

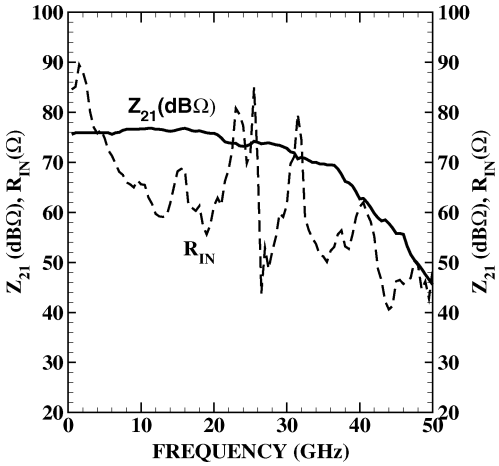

Fig. 13. On-wafer measured small-signal (with −65-dBm input signal) single-ended Z_{21} and input resistance of the TIALA.

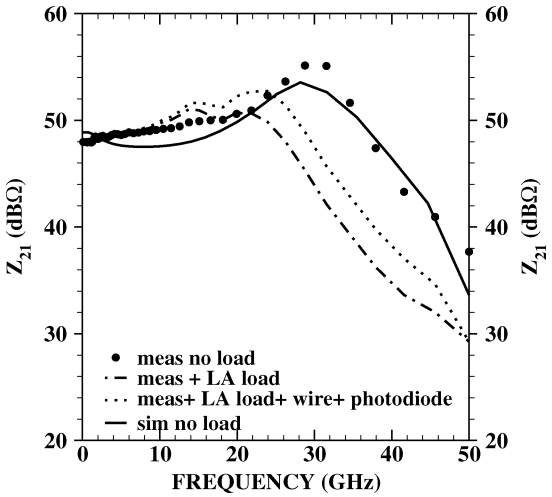

Fig. 14. Measured (symbols) and simulated (solid line) Z_{21} of the unloaded TIA on its own. Simulation results based on the measured unloaded TIA S-parameters and illustrating the impact of the estimated loading due to the LA (dotted-dashed line) and the impact of the photodiode capacitance and bondwire inductance (dotted line) are also included. The input impedance of the LA stage was approximated by a series connection of a 20-Ω resistance and an 80-fF capacitance.

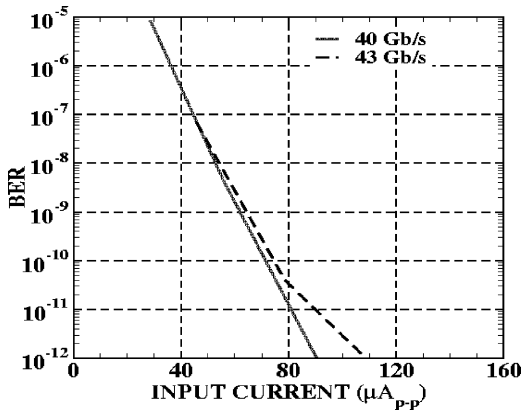

Fig. 15. Measured sensitivity with a $2^{31}-1$ PRBS.

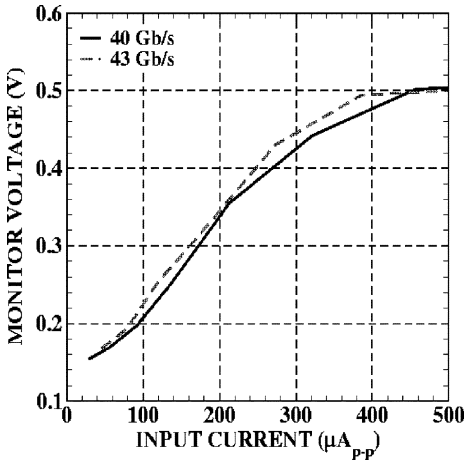

Fig. 16. Measured signal-level monitor output as a function of the $2^{31}-1$ PRBS signal level.

unloaded TIA stage. Its bandwidth is 38 GHz and it features intentional gain peaking to compensate for the input capacitance and base resistance of the following Cherry–Hooper stage, and for the frequency-dependent loss in the two transmission line sections. The simulation results for the latter case are represented with a dotted-dashed line. Additional simulation results (dotted line), using the measured S parameters of the TIA test structure as a "black box" and including the photodiode capacitance and bonwire inductance, indicate that the diode capacitance is fully compensated by the bondwire inductance and that the on-wafer measurements are somewhat pessimistic in terms of bandwidth, sensitivity, and jitter.

The Anritsu MP1801A 43.5-Gb/s multiplexer (MUX) and bit-error ratio tester (BERT), and the Agilent 86 100A DCA with the 86118A 70-GHz dual remote sampling head were used for on-wafer eye diagram and electrical sensitivity measurements, as shown in Fig. 15. The sensitivity is 90 and 110 μA_{pp} at 40 and 43 Gb/s, respectively, defined at a bit-error rate (BER) of 10^{-12} using $2^{31}-1$ pattern and accounting for the 65-Ω input impedance. The corresponding signal level monitor output is reproduced in Fig. 16. Fig. 17 showcases the single-ended output eye diagrams at 40 Gb/s with $2^{31}-1$ pseudorandom bit sequence (PRBS) for current levels of 190 μA_{pp} and 6.2 mA_{pp}, while

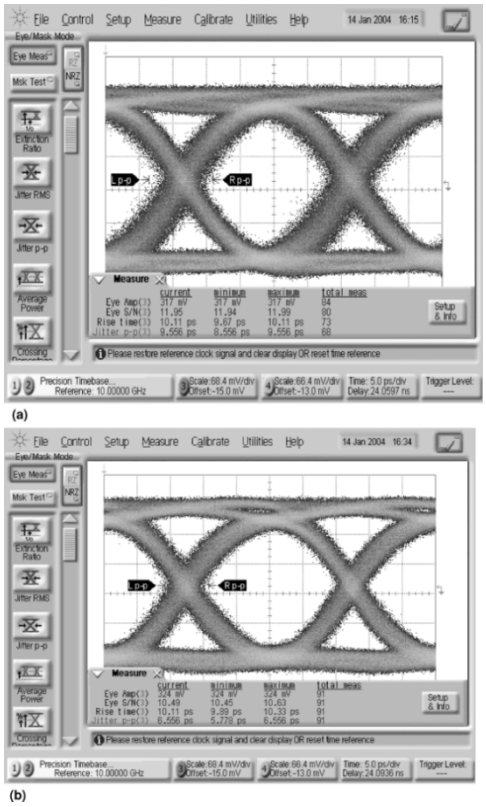

Fig. 17. On-wafer measured 40-Gb/s single-ended output eye diagrams corresponding to (a) 190 μA_{pp} and (b) 6.2 mA_{pp} inputs with $2^{31}-1$ PRBS.

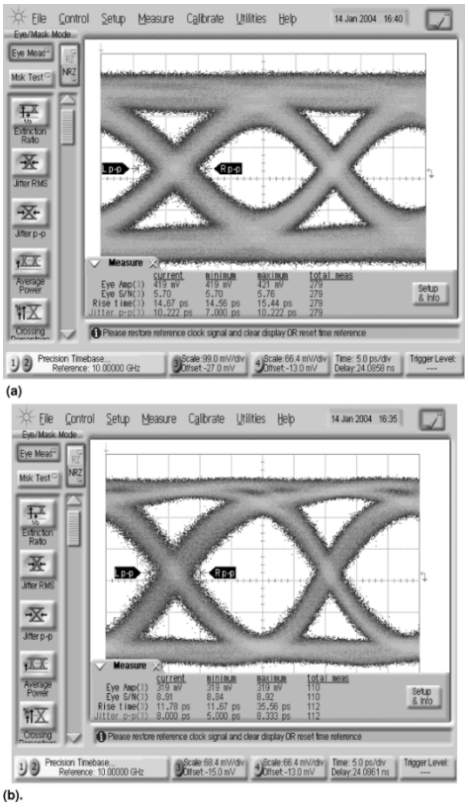

Fig. 18. On-wafer measured 43-Gb/s, single-ended (a) input and (b) output eye diagram corresponding to a 6.2 mA_{pp} input with $2^{31}-1$ PRBS.

Figs. 18–20 summarize the input and output eye diagrams at 43 Gb/s with $2^{31}-1$ pattern for input currents of 6.2 mA_{pp}, 420 μA_{pp}, and 190 μA_{pp}, respectively. The loss of the probes has not been accounted for. In all cases, the output is limited to 320 mV_{pp} per side and the eye Q is larger than 10 over a dynamic range of 15 dB even though the Q of the input eye is very poor. The limiting action of the TIALA improves the jitter, the signal-to-noise-ratio (SNR), and the rise/fall times of the eye diagrams in comparison to those coming out of the 40-Gb/s Anritsu MUX.

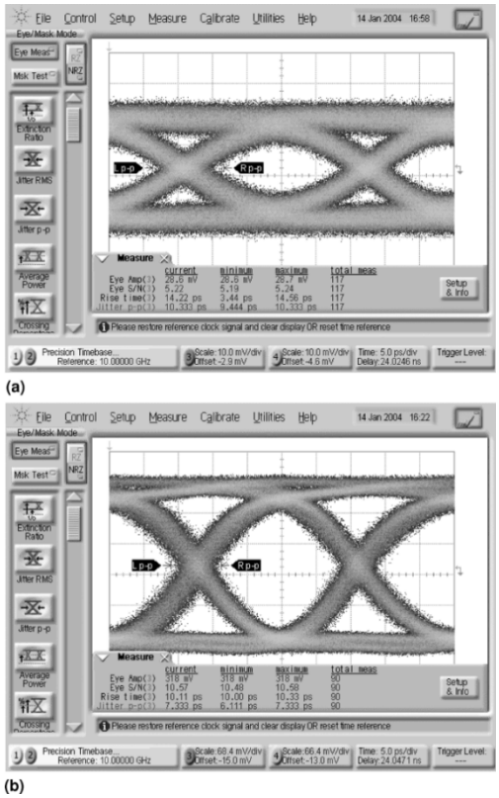

Fig. 19. On-wafer measured 43 Gb/s, single-ended input (a) and output (b) eye diagram corresponding to a 420 μA_{pp} input with $2^{31}-1$ PRBS.

The circuit was next mounted as a limiting amplifier in a customer module and its electrical sensitivity at 43 Gb/s was found to be better than 8 mV_{pp} for a 2^{23}–1 pattern, as illustrated in Fig. 21. The measured jitter of the input and output eye diagrams is 994 fs_{rms} and 1.11 ps_{rms}, respectively, with 0.5 ps_{rms} due to the TIALA. This sensitivity value represents a factor of two improvement over the best sensitivity reported for 40-Gb/s limiting amplifiers (20 mV_{pp} in [9]) or SERDES (31 mV_{pp} single-ended in [10]). It recommends the TIA stage as the lowest noise circuit topology for high-data-rate voltage pre-amplifiers.

V. Conclusion

A high-gain high-dynamic-range 43-Gb/s transimpedance-limiting amplifier has been designed and fabricated in InP/InGaAs HBT technology. An analytical model was developed and employed to derive the optimal transistor size which concomitantly leads to the minimum input equivalent noise current and to the minimum 50-Ω noise figure, when the circuit is operated as a transimpedance amplifier in conjunction with a photodiode, and as a low-noise limiting amplifier, respectively. The TIALA

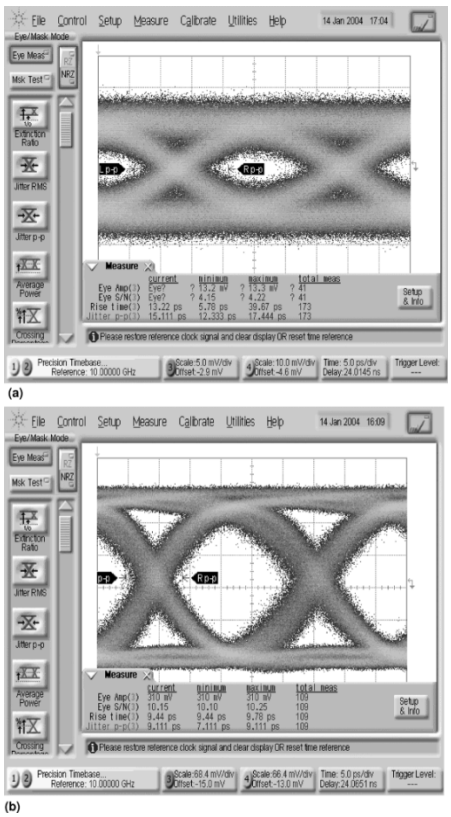

Fig. 20. On-wafer measured 43-Gb/s, single-ended input (a) and output (b) eye diagram corresponding to a 190 μA_{pp} input with $2^{31} - 1$ PRBS.

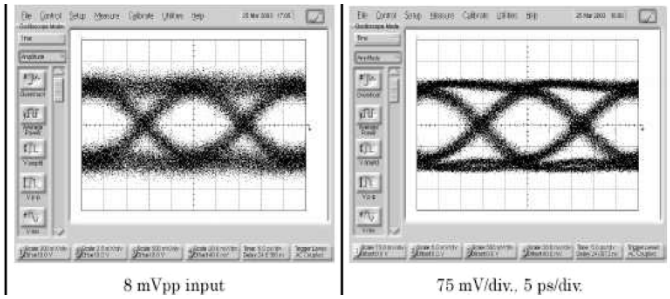

Fig. 21. Measured 43 Gb/s, $2^{23} - 1$ input (8 mV_{pp}) and output (320 mV_{pp}) single-ended eye diagram of the TIALA mounted in a customer module as a limiting amplifier.

exhibits 6-kΩ gain, 100-μA_{pp} sensitivity, 6-mA_{pp} input overload current, and high levels of functional integration. It consumes less than 450 mW from a single 3.3-V supply. When measured as a 43-Gb/s limiting amplifier with a $2^{23}-1$ PRBS, the sensitivity is 8 mV_{pp}, a factor of two improvement over the best data reported to date.

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REFERENCES

[1] H.-M. Rein, "Si and SiGe bipolar IC's for 10 to 40 Gb/s optical-fiber TDM links," *Int. J. High Speed Electron. Syst.*, vol. 9, pp. 1–37, 1998.

[2] J. Mullrich, T. F. Meister, M. Rest, W. Bogner, A. Schöpflin, and H.-M. Rein, "40 Gb/s transimpedance amplifier in SiGe bipolar technology for the receiver in optical-fiber TDM links," *Electron. Lett.*, vol. 34, pp. 452–453, 1998.

[3] S. P. Voinigescu, P. Popescu, P. Banens, M. Copeland, G. Fortier, K. Howlett, M. Herod, D. Marchesan, J. Showell, S. Szilagyi, H. Tran, and J. Weng, "Circuits and technologies for highly integrated optical networking IC's at 10 Gb/s to 40 Gb/s," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, San Diego, CA, May 2001, pp. 331–338.

[4] C. Q. Wu, E. A. Sovero, and B. Massey, "40 GHz transimpedance amplifier with differential outputs using InP/InGaAs heterojunction bipolar transistors," in *IEEE GaAs IC Symp. Tech. Dig.*, Monterey, CA, Nov. 2002, pp. 63–66.

[5] D. Caruth, S. C. Shen, D. Chan, M. Feng, and J. Schutt-Ainé, "A 40 Gb/s integrated differential PIN+TIA with DC offset control using InP SHBT technology," in *IEEE GaAs IC Symp. Tech. Dig.*, Monterey, CA, Nov. 2002, pp. 59–62.

[6] K. W. Kobayashi, "An InP HBT common-base amplifier with tunable transimpedance for 40 Gb/s applications," in *IEEE GaAs IC Symp. Tech. Dig.*, Monterey, CA, Nov. 2002, pp. 155–158.

[7] S. P. Voinigescu, M. C. Maliepaard, J. L. Showell, G. Babcock, D. Marchesan, M. Schroter, P. Schvan, and D. L. Harame, "A scalable high frequency noise model for bipolar transistors with application to optimal transistor sizing for low-noise amplifier design," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1430–1438, Sept. 1997.

[8] G. D. Vendelin, A. M. Pavio, and U. L. Rhode, *Microwave Circuit Design*. New York: Wiley, 1990, ch. 2, pp. 77–83.

[9] K. Krishnamurti, R. Vetury, J. Xu, A. Shou, A. Jaganathan, K. Cheng, J. Chow, D. Mensa, L. Zhang, I. Gontijo, S. Vu, C. Wimczewski, Y. Liu, R. Pullela, and M. Rodwell, "40 Gb/s TDM system using InP HBT IC technology," in *IEEE MTT-S Dig.*, June 2003, pp. 1189–1192.

[10] K. Watanabe, A. Koyama, T. Harada, T. Aida, A. Ito, T. Murata, H. Yoshioka, M. Sonehara, H. Yamashita, K. Ishikawa, M. Ito, N. Shiramizu, T. Nakamura, K. Ohhata, F. Arakawa, T. Kususnoki, H. Chiba, T. Kurihara, and M. Kuraiashi, "A low-jitter 16:1 MUX and a high-sensitivity 1:16 DEMUX with integrated 39.8 to 43 GHz VCO for OC-768 communication systems," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2004, pp. 166–167.

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