Frequency Scaling and Topology Comparison of Millimeter-wave CMOS VCOs

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***Abstract* — This paper presents an algorithmic design methodology and frequency scaling technique for CMOS VCOs. It illustrates the almost ideal scaling of a fundamental 10-GHz, 90-nm CMOS Colpitts VCO with -117 dBc/Hz phase noise and 4 dBm output power to 77 GHz. The 77-GHz VCO features linear 8.3% tuning range and a phase noise of -100.3 dBc/Hz at 1 MHz offset. The first complementary cross-coupled VCO operating at 77 GHz is also reported. In addition, a new figure of merit for CMOS VCO based on the one defined in the 2003 ITRS is proposed to adequately account for the VCO output power and efficiency.**

Keywords – Millimeter-wave, CMOS, VCO, frequency scaling, Colpitts, cross-coupled, figure of merit.

I. INTRODUCTION

SiGe HBT mm-wave VCOs have the advantage of large transistor voltage swings and low phase noise. However, their power dissipation is excessive. At lower frequencies, CMOS VCOs have gained popularity due to their low power dissipation brought about by the significantly lower supply voltages. However, to date, mm-wave CMOS VCOs suffer from inadequate output power levels, reduced tuning range and, until recently [1], from very poor phase noise. Here, a family of 90-nm CMOS VCOs with record tuning range and phase noise performance at 77 GHz are presented.

A systematic design procedure for Colpitts VCOs implemented in SiGe HBT technology was presented in [2]. Similarly, in section II of this paper, an algorithmic design methodology for CMOS Colpitts and cross-coupled VCOs is described. Performance of each topology at RF and at mm-wave frequencies is also discussed. A technique to scale the oscillation frequency f_{osc} of these VCOs is covered in section III, while section IV explains the inadequacy of the VCO FoM as defined in the 2003 ITRS [3] and proposes a new FoM that adequately captures the power efficiency of VCOs in practical applications. Finally, measurement results are summarized in section V.

II. CMOS VCO DESIGN METHODOLOGY

A. Colpitts VCO

The schematic of the 77-GHz Colpitts VCO is shown in Fig. 1. The design methodology for the Colpitts VCO can be summarized as follows.

1) Determine L_{TANK} according to the design constraints [2]. Choose smallest L_{TANK} for minimum phase noise and maximum tuning range, or largest L_{TANK} for minimum power dissipation.

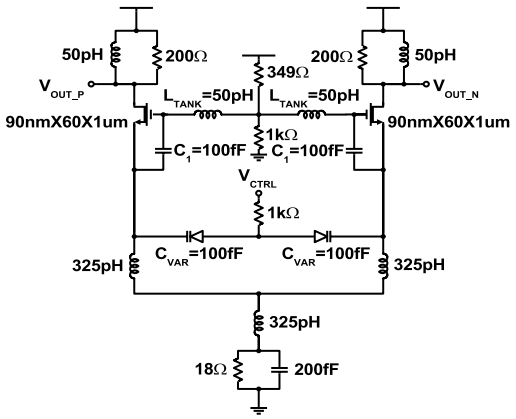

Figure 1. Schematic of 77-GHz Colpitts VCO.

2) For a given f_{osc} (1), the equivalent capacitance (2) is known once L_{TANK} is chosen. Select $C_1 >> C_{VAR}$ for maximum tuning range, or $C_1 = C_{VAR}$ for minimum power dissipation.

$$f_{osc} = \frac{1}{2\pi\sqrt{L_{TANK}C_{eq}}} \tag{1}$$

$$C_{eq} = \frac{(C_1 + C_{GS})(C_{VAR} + C_{SB})}{C_1 + C_{VAR} + C_{GS} + C_{SB}} + C_{GD} \approx \frac{C_1 C_{VAR}}{C_1 + C_{VAR}} \tag{2}$$

3) Bias the transistors at the optimum noise figure current density of 0.15 mA/μm [4] for minimum phase noise. Size transistors (gate width W) to provide enough negative resistance for oscillation (3).

$$G_m \geq \omega_{osc}{}^2 C_1 C_{VAR} R_S \tag{3}$$

$$R_S = \frac{\omega_{osc} L_{TANK}}{Q_L} \tag{4}$$

B. Cross-coupled VCO

The typical schematic of a cross-coupled VCO is shown in Fig. 2. Its design methodology can be summarized as follows.

1) Choose smallest L_{TANK} for maximum tuning range, or largest L_{TANK} for minimum power dissipation.

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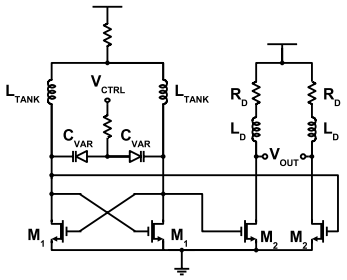

Figure 2. Schematic of cross-coupled VCO.

2) For given oscillation frequency (1), the equivalent capacitance (5) is known once L_{TANK} is chosen. In contrast to the Colpitts topology, C_{eq} is heavily dependent on the parasitic capacitance of the transistor.

$$C_{eq} = C_{VAR} + C_{GS} + 4C_{GD} + C_{DB} + C_{GS\_M_2} + C_{GD\_M_2} \quad (5)$$

3) Bias the transistors at 0.15 mA/μm for minimum phase noise. Determine transistor size from oscillation condition (6).

$$(G_m R_P)^2 \geq 1 \quad (6)$$

$$R_P = \omega_{osc} L_{TANK} Q_L \quad (7)$$

4) Subtract the parasitic capacitances of the transistor from the equivalent capacitance to obtain the varactor size.

In cross-coupled VCOs, as the parasitic capacitances of transistors are directly lumped to the tank capacitance, the tuning range is limited by the transistor size. It is further degraded by the output buffer which is always present in cross-coupled VCOs, either to drive the 50-Ω test equipment or to distribute the VCO signal to mixers and frequency dividers in an IC. At mm-wave frequencies, where a relatively large transistor size has to be used to maintain oscillation, tuning range is sacrificed. At lower frequencies, large tuning range can be realized with small transistor and large varactor sizes which also leads to lower power dissipation, and thus to a superior figure of merit. However, for the same reasons, its output power is generally far below the acceptable range of 0 to 5 dBm. By comparison, the Colpitts VCO requires larger transistor size and current to produce the oscillation, and hence dissipates more power. Nevertheless, since the output buffer is built into the topology, its power efficiency and output power are higher. Moreover, its tuning range is mainly determined by the C_1:C_{VAR} ratio, which is independent of the oscillation frequency. Most importantly, f_{osc} depends primarily on the passive components (L_{TANK}, C_1 and C_{VAR}) which implies that redesigning the VCO to another frequency can be achieved simply by scaling the passive components of the VCO.

III. Frequency Scaling

From eqns. (1) and (2) in the previous section, if L_{TANK}, C_1 and C_{VAR} are all reduced by a factor of k, the oscillation frequency of a Colpitts VCO will be scaled by the same factor:

$$L_{TANK}' = \frac{L_{TANK}}{k}, C_1' = \frac{C_1}{k}, C_{VAR}' = \frac{C_{VAR}}{k} \quad (8)$$

$$f_{osc}' = k f_{osc} \quad (9)$$

If the series resistance of the tank inductor is also scaled down with the tank inductance:

$$R_S' = \frac{R_S}{k} \quad (10)$$

Substituting (10) into (3), we obtain:

$$G_m' = \frac{G_m}{k} \quad (11)$$

which implies that the transistor size and bias current, can be reduced by the same factor. Note that f_{osc} scales exactly even if the parasitic capacitance of the transistor is taken into account. However, R_S does not scale linearly as f_{osc} increases because it includes the parasitic gate and source resistances of the transistor, both of which increase as the total gate width is reduced. As a result, when a VCO design is scaled to a very high frequency, a relatively larger transistor is required to maintain oscillation than that given by (11). Furthermore, it is critical to scale the entire VCO layout, i.e. transistor layout, component orientation, as well as the interconnect routing between components to ensure that layout parasitics also scale.

IV. CMOS VCO Figure of Merit

According to the 2003 ITRS, the FoM for VCOs is defined as:

$$FoM_1 = \left(\frac{f_{osc}}{\Delta f}\right)^2 \frac{1}{L[\Delta f] P_{diss}} \quad (12)$$

However, (12) does not include the output power generated by the VCO. As a result, it artificially rewards designs with low DC power and mediocre phase noise, rather than promoting low phase noise with high power efficiency. It also leads to the misleading conclusion that the cross-coupled topology is superior to the Colpitts one in CMOS technology [5] and that current CMOS mm-wave VCOs actually outperform SiGe HBT VCOs. In practical applications, VCO output power is critical to drive mixers, buffers and power amplifiers. For example, a 77-GHz automotive radar transmitter needs to generate in excess of +16 dBm in a 50-Ω impedance. This means that in a CMOS system implementation, the design burden is simply shifted from the VCO to the PA. Therefore, it is important to include output power in the VCO FoM:

$$FoM_2 = \left(\frac{f_{osc}}{\Delta f}\right)^2 \frac{P_{out}}{L[\Delta f] P_{diss}} \quad (13)$$

V. Measurement Results

To validate the above observations, 12 VCO test structures have been fabricated in TSMC's 180-nm and STM's 90-nm CMOS technologies. Both cross-coupled and Colpitts

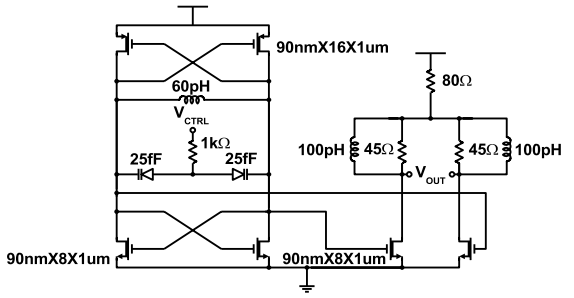

Figure 3. Schematic of 77-GHz cross-coupled VCO.

topologies were fabricated at 10, 20, 40, 50 and 77 GHz. In all cases, the MOSFETs were biased at the optimum noise figure current density. The schematic of the 77-GHz CMOS cross-coupled VCO is shown in Fig. 3. Its measured output power, phase noise and tuning characteristics are shown in Fig. 4. It can be tuned between 76.2 and 78.2 GHz, with a measured phase noise of -84.3 dBc/Hz at 10 MHz offset. The core transistors dissipate between 5 mA and 7.5 mA when the supply varies between 1.5 V and 1.8 V. This marks the first demonstration of a circuit with p-MOSFETs operating at 77 GHz.

As illustrated in Fig. 5, the 77-GHz Colpitts VCO can be tuned between 73.8 and 80 GHz, with a measured phase noise as low as -100.3 dBc/Hz at 1 MHz offset (Fig. 6). It draws 18 to 25 mA from 1.2 V to 1.5 V supply. It is a scaled replica of a 10-GHz Colpitts VCO (L_{TANK} = 435 pH, $C_1 = C_{VAR}$ = 800 fF, 100 x 1 um transistor size). The measured performance of the latter is shown in Fig. 7, with -117 dBc/Hz at 1 MHz offset when biased from 1.2 V. For the purpose of comparison, a 10-GHz NMOS cross-coupled VCO ($M_1 = M_2$ = 24 x 1 um, L_{TANK} = 435 pH, C_{VAR} = 260 fF) was also fabricated, and its performance is shown in Fig. 8. It can be tuned between 9.3 and 10.9 GHz, with a phase noise of -109.2 dBc/Hz at 1 MHz offset. The die photo of the 77-GHz Colpitts VCO is shown in Fig. 9. The VCO core occupies 0.22 mm x 0.l6 mm.

A comparison between W-band CMOS and SiGe HBT VCOs using FoM_1 and FoM_2 is shown in Figs. 10 and 11, respectively. Based on FoM_2, it becomes apparent that SiGe HBT VCOs exhibit superior performance to CMOS VCOs at 77 GHz. Table I summarizes state-of-the-art CMOS and SiGe HBT VCOs in the 60-GHz to 120-GHz range. The FoM of the

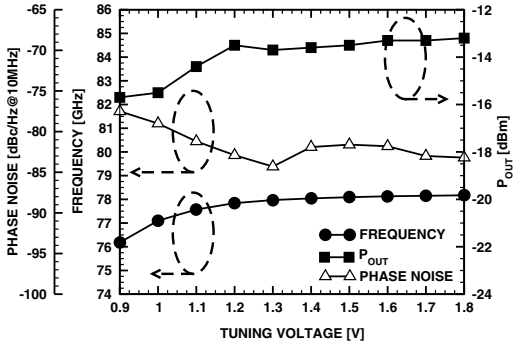

Figure 4. Frequency, output power and phase noise versus tuning voltage of the 77-GHz cross-coupled VCO.

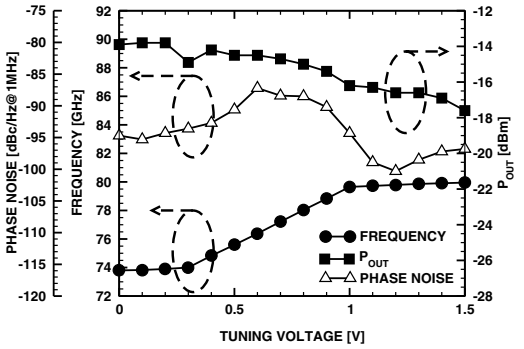

Figure 5. Frequency, output power and phase noise versus tuning voltage of the 77-GHz Colpitts VCO.

77-GHz Colpitts VCO is almost identical to that of its 10-GHz replica, indicating almost perfect scaling of oscillation frequency and phase noise. For the 10-GHz VCOs described in this work, the Colpitts topology achieves better figures of merit than the cross-coupled topology, despite the fact that its power dissipation is four times larger. Furthermore, its FoM_2, output power, and phase noise are comparable to those of the best SiGe HBT VCOs, indicating that CMOS VCOs are capable of delivering similar performance to the SiGe HBT ones at lower frequencies.

VI. Conclusion

An algorithmic design methodology and frequency scaling technique for CMOS VCOs has been presented and validated in measurements. Record phase noise and tuning range have been achieved at 77 GHz using a Colpitts topology, and the first cross-coupled VCO employing p-MOSFETs operating above 50 GHz, has also been demonstrated. Finally, a new figure of merit has been proposed to allow for a realistic comparison between VCO topologies and technologies. While the phase noise of CMOS VCOs at mm-waves is now comparable to that of SiGe HBT ones, they continue to underperform in terms of output power levels.

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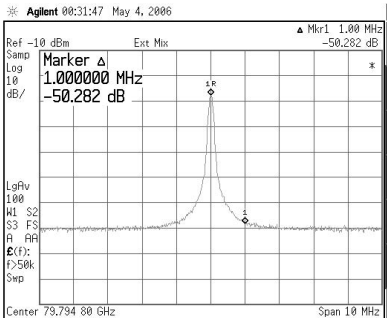

Figure 6. Averaged (100 sweeps) spectral plot of phase noise in 77-GHz Colpitts VCO, showing -100.3dBc/Hz @ 1MHz offset.

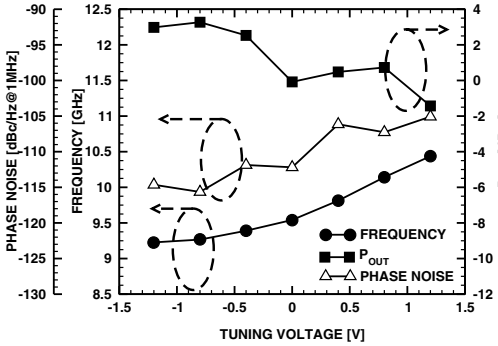

Figure 7. Frequency, output power and phase noise versus tuning voltage of the 10-GHz Colpitts VCO.

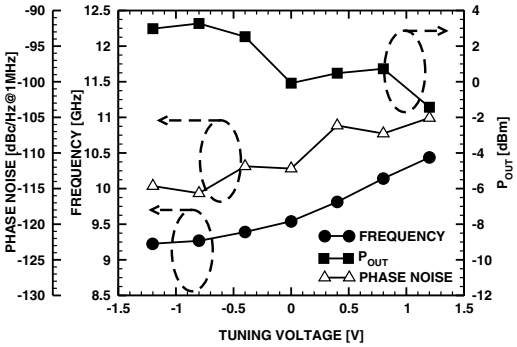

Figure 8. Frequency, output power and phase noise versus tuning voltage of the 10-GHz cross-coupled VCO.

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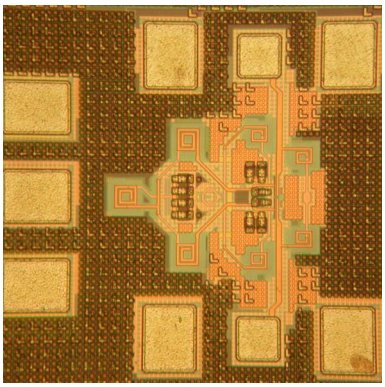

Figure 9. Die photo of 77-GHz Colpitts VCO.

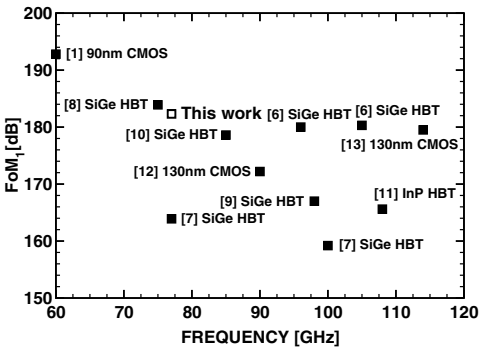

Figure 10. FoM_1 of the state-of-the-art SiGe HBT and CMOS VCOs.

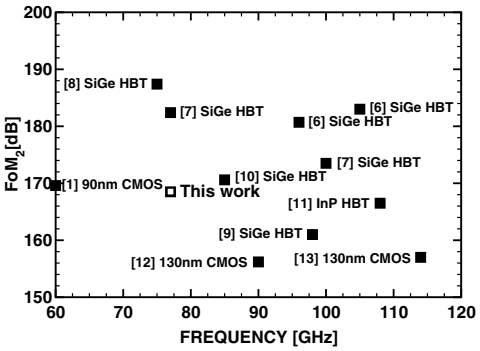

Figure 11. FoM_2 of the state-of-the-art SiGe HBT and CMOS VCOs.

TABLE I. PERFORMANCE SUMMARY OF THIS WORK AND STATE-OF-THE-ART SIGE HBT AND CMOS VCOS.

Reference	Process	f_{osc} [GHz]	Tuning [%]	Phase Noise [dBc/Hz]	P_{out} [dBm]	P_{diss} [mW]	FoM_1 [dB]	FoM_2 [dB]
This work - Colpitts	90nm CMOS	10	12.2	-117.5@1MHz	4.0	36	181.9	185.9
		77	8.1	-100.3@1MHz	-13.8	37.5	182.3	168.5
This work - NMOS cross-coupled	90nm CMOS	10	15.8	-109.2@1MHz	-2.2	7.5	180.4	178.2
This work - CMOS cross-coupled	90nm CMOS	77	2.6	-84.3@10MHz	-13.2	13.5	150.7	137.5
[1]	90nm CMOS	60	0.17	-100@1MHz	-23.2	1.9	192.8	169.6
[6]	SiGe HBT, f_T = 170GHz	96	4.6	-101.6@1MHz	0.7	133	180.0	180.7
	SiGe HBT, f_T = 230GHz	105	4.4	-101.3@1MHz	2.5	133	180.3	183.0
[7]	SiGe HBT, f_T = 175GHz	77	8.7	-97@1MHz	18.5	1200	163.9	182.4
		100	6.2	-90@1MHz	14.3	1200	159.2	173.5
[8]	SiGe HBT, f_T = 200GHz	75	6.1	-105@1MHz	3.5	72	183.9	187.4
[9]	SiGe HBT, f_T = 200GHz	98	3.3	-85@1MHz	-6	60	167.0	161.0
[10]	SiGe HBT, f_T = 200GHz	85	2.7	-94@1MHz	-8	25	178.6	170.6
[11]	InP HBT, f_T = 75GHz	108	2.6	-88@1MHz	0.92	204	165.6	166.5
[12]	130nm CMOS	90	2.4	-105@10MHz	-16	15.5	172.2	156.2
[13]	130nm CMOS	114	2.1	-107.6@10MHz	-22.5	8.4	179.5	157.0