# A Large Swing, 40-Gb/s SiGe BiCMOS Driver with Adjustable Pre-Emphasis for Data Transmission over 75Ω Coaxial Cable

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***Abstract* — A fully differential 40-Gb/s cable driver with adjustable pre-emphasis is presented. Based on a distributed limiting architecture, the circuit can supply up to 3.6V peak-to-peak per side in a 75Ω load with variable pre-emphasis ranging from 0 to 400%. S-parameter measurements show 42dB differential small-signal gain, a bandwidth of 22GHz, gain peaking control up to 25dB at 20GHz and input and output reflection coefficients better than -10dB up to 40GHz. Additional features of the driver include output amplitude control (from $1V_{pp}$ to $3.6V_{pp}$ per side), pulse-width control (35% to 65%) and an adjustable input DC level (1.1V to 1.8V) allowing the circuit to interface with a SiGe BiCMOS or MOS-CML SERDES.**

***Index Terms* — SiGe BiCMOS, cable equalizers, modulator drivers, pre-emphasis, amplitude control, optical fiber communication, high speed data communication.**

## I. Introduction

Increasing consumer demand for HDTV and digital cinema is driving video distribution standards to multi-gigabit per second rates. As bit rates increase, loss (caused by skin effect and dielectric loss) in copper cables causes significant attenuation of the transmitted data at high frequencies. A critical success factor for the serial digital interface (SDI) has been its ability to evolve over time while retaining the use of the installed, bandwidth limited, coaxial cable infrastructure.

To send 40-Gb/s data over large lengths (>50m) of standard 75Ω coaxial cable with a bandwidth of 3-GHz requires approximately 50dB of channel equalization. This prerequisite imposes that the task of equalization be divided between the transmitter and the receiver.

In this paper, the first fully differential 40-Gb/s SiGe BiCMOS cable driver with $3V_{pp}$ swing per side, and adjustable pre-emphasis is presented. Earlier papers have reported 40-Gb/s output swings up to $3V_{pp}$ per side in GaAs p-HEMT [1], $3.5V_{pp}$ in SiGe single-ended [2] and $5.65V_{pp}$ per side in InP [3], without pre-emphasis control.

## II. Large Swing Driver Design

A block diagram of the large swing cable driver is presented in Fig. 1. The circuit architecture consists of a six-stage lumped predriver followed by a seven-stage distributed amplifier (DA). The DA section is similar to that of the 3V GaAs p-HEMT driver in [1]. However, unlike [1], 0 to 400% (~25dB gain peaking) pre-emphasis control is also implemented.

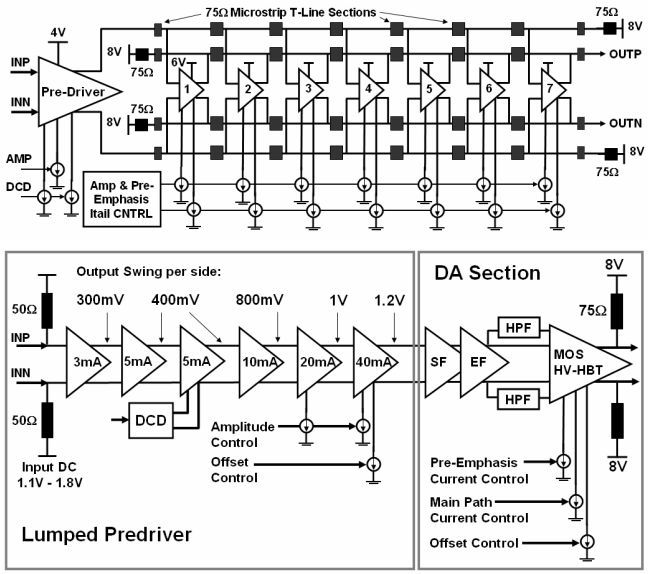


**Fig. 1.** 40-Gb/s driver architecture illustrating the waveshape control functions.

### A. Lumped Predriver

The input stage features on-chip 50Ω resistors and spiral inductors to provide good input match without the use of emitter followers (EF). The lumped predriver is designed to accept a $150mV_{pp}$ per side signal at an input DC level ranging from 1.1V to 1.8V. This signal is amplified and limited to $1.2V_{pp}$ per side, and drives the input of the DA. To maximize the bandwidth of the predriver and save power, duty-cycle distortion (DCD) control is implemented at the low-impedance cascode node of the third inverting stage. To avoid any reflections with the DA, the final limiter is terminated with resistors that are matched to the characteristic impedance of the DA's input transmission lines.

### B. 7-Section Distributed Amplifier

Each DA stage consists of a MOS-HBT differential cascode realized with 0.18μm n-channel MOSFETs and high-breakdown voltage SiGe HBTs (HV-HBT). The MOSFETs and HBTs have $f_T/f_{MAX}$ values of 50GHz/80GHz and 75/100GHz, respectively. Although faster HBTs with $f_T$ and $f_{MAX}$ values of 160GHz are available in this technology

[4], and were employed in 40-Gb/s feed-forward [5] and decision-feedback [6] equalizers, the large output swing requirement exceeds their reliability limit. Furthermore, the use of a 0.18µm n-channel MOSFET in combination with a HV-HBT allows $1.2V_{pp}$ per side to be applied on the gate of the MOSFET, without the need for source degeneration. The $1.2V_{pp}$ input to the DA is imposed by the output voltage swing, which is greater than $3.6V_{pp}$, and the 10dB gain of the DA.

In order to maximize the bandwidth, the output amplitude and pre-emphasis control functions are implemented in each DA cell, as illustrated in Fig. 2. The input signal is applied simultaneously to the MOS-HV-HBT differential pair, whose tail current is varied to control the output amplitude [7], and to a pre-emphasis block. The latter is comprised of a RC-differentiator followed by a differential pair realized with high-speed, low-breakdown voltage HBTs (HS-HBT). The pre-emphasis path and the main path are combined at the low-impedance node between the drain of the MOSFET (and collector of the HS-HBT) and the emitter of the common-base HV-HBT. This scheme results in minimal degradation of the DA bandwidth while maximizing control of the shape of the output waveforms.

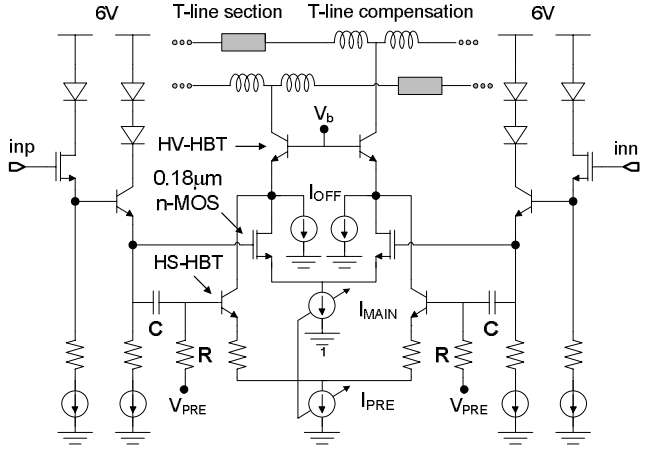


**Fig. 2.** DA section with adjustable amplitude ($I_{main}$), pre-emphasis ($I_{pre}$) and offset ($I_{off}$) control.

## III. Layout and Fabrication

The chip was fabricated in Jazz Semiconductor's SBC18HX, 0.18µm SiGe BiCMOS process and operates from 4V, 6V and 8V supplies. It consumes approximately 3.6W and occupies an area of 1.2mm x 2.5mm. The die photo is reproduced in Fig. 3. The fully differential DA features 75Ω input and output transmission lines realized in the thick top metal of the technology, with "Metal 2" as the ground plane. As in [5], this allows for the routing of bias and control lines below the ground plane. Inductive peaking is distributed along the microstrip T-lines in order to compensate for the periodic loading from each DA stage.

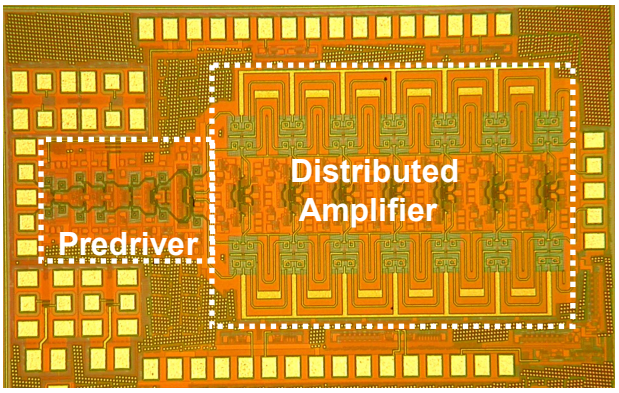


**Fig. 3.** Microphotograph of the cable driver (2.5mm x 1.2mm).

## IV. Experimental Results

All measurements were conducted on wafer in a 50Ω environment. The complete driver exhibits an overall small-signal gain of 36dB per side when DC-coupled to an external 75Ω load.

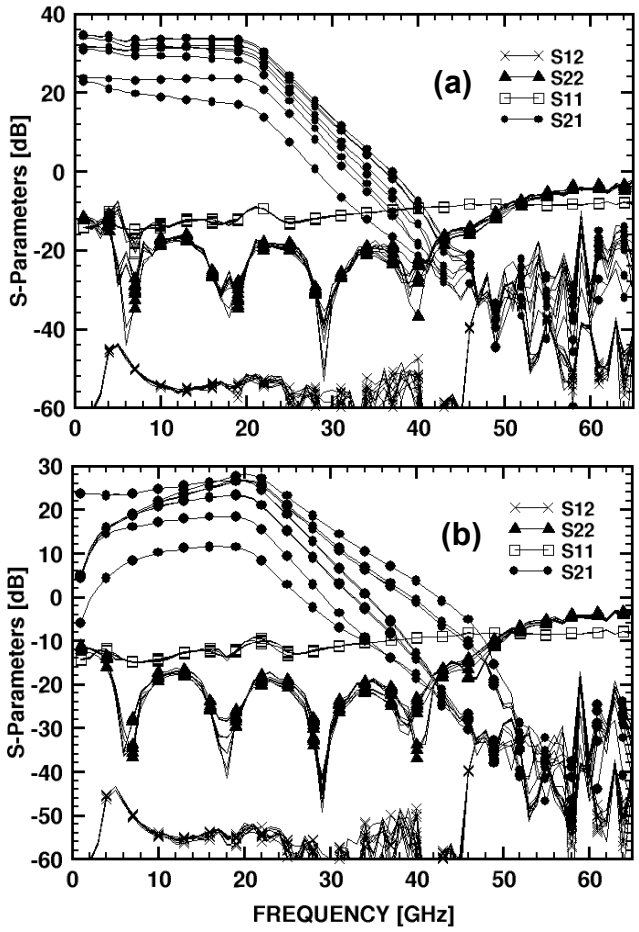


**Fig. 4.** S-Parameters showing **(a)** 10dB amplitude control and 36 dB single-ended gain (42 dB differential) and **(b)** controllable pre-emphasis with up to 25dB of peaking in the range 1 - 20 GHz.

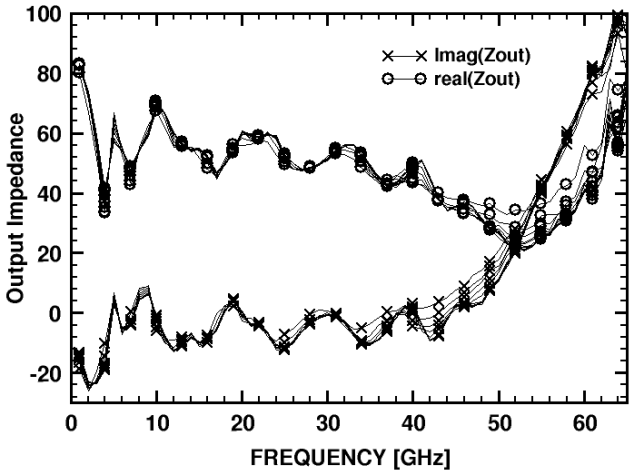


**Fig. 5.** Measured real and imaginary parts of the output impedance of the driver.

S-parameter measurements, shown in Fig. 4, demonstrate 10dB of amplitude control and 25dB of pre-emphasis control with negligible impact on the driver's input and output return loss which are better than -10dB up to 40GHz. The die exhibits 50dB isolation up to 45GHz. Fig. 5 shows that the cable driver's measured DC output impedance of 82Ω is close to the design target of 75Ω.

Time domain measurements were conducted on-wafer in a 50Ω environment using an Agilent 86100DC DCA-J oscilloscope and an Agilent E8257D signal source. Fig. 6 and 7 show 3:1 (~10dB) output amplitude control at 40 Gb/s for a 4 x $2^{31}$-1 PRBS input pattern. The output swings are $3.0V_{pp}$, and $1.0V_{pp}$ per side, respectively, for a single-ended input signal of $300mV_{pp}$. Eye diagrams with 200% and 400% pre-emphasis are shown in Figs. 8 and 9 for the same 40-Gb/s input. A duty cycle control of 35% to 65% is also achieved at 40 Gb/s as illustrated in Fig. 10.

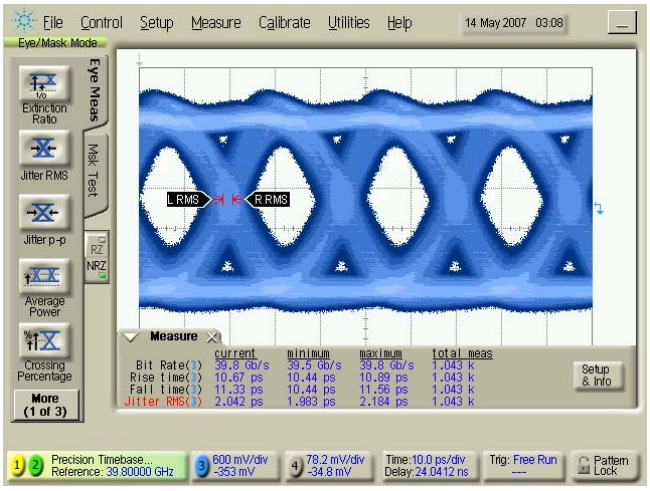


**Fig. 6.** $2^{31}$-1 40-Gb/s output eye diagram with $3V_{pp}$ per side.

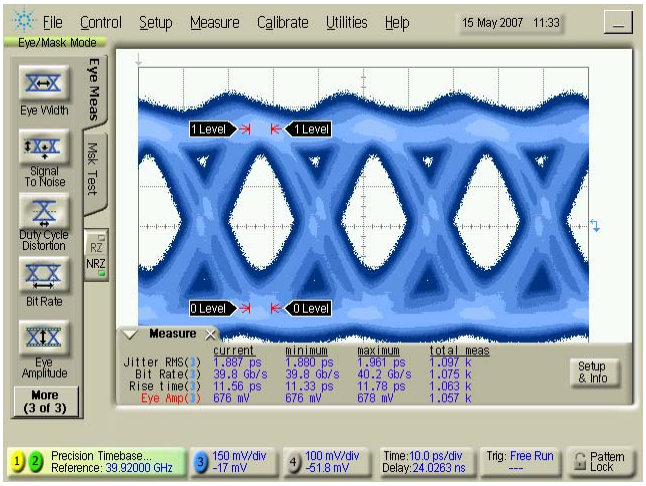


**Fig. 7.** $2^{31}$-1 40-Gb/s output eye diagram with $1V_{pp}$ per side.

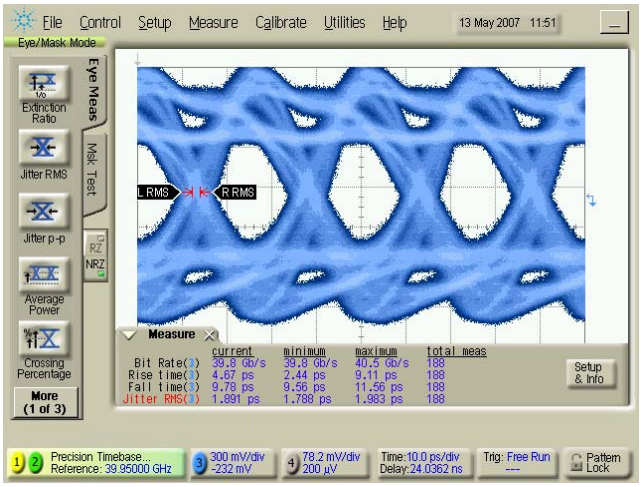


**Fig. 8.** $2^{31}$-1 40-Gb/s output eye diagram with $2V_{pp}$ per side and 200% pre-emphasis.

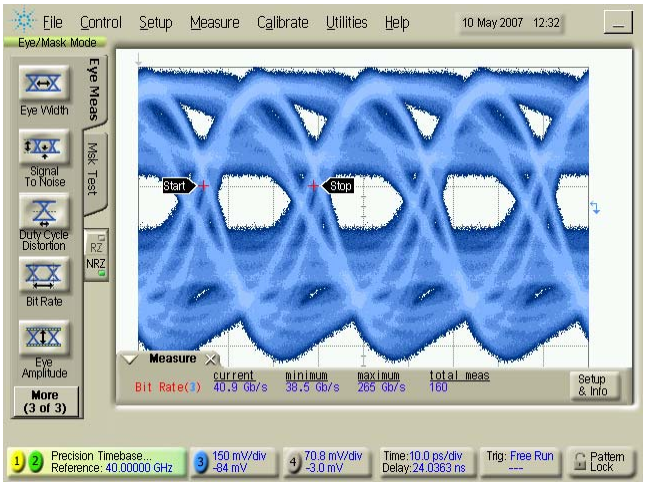


**Fig. 9.** $2^{31}$-1 40-Gb/s output eye diagram with $1V_{pp}$ per side and 400% pre-emphasis.

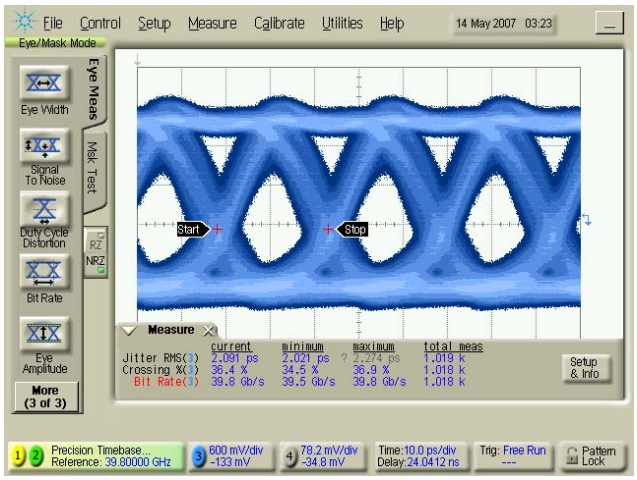


**Fig. 10.** $2^{31}$-1 40-Gb/s output eye diagram with $3V_{pp}$ per side and 35% DCD.

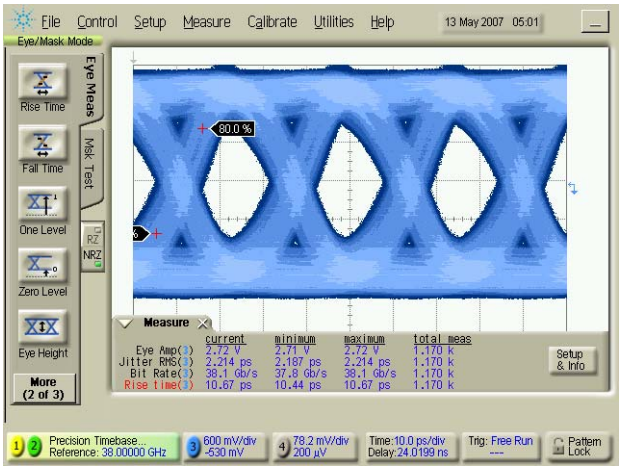


**Fig. 11.** $2^{31}$-1 38-Gb/s output eye diagram with maximum output swing of $3.6V_{pp}$ per side.

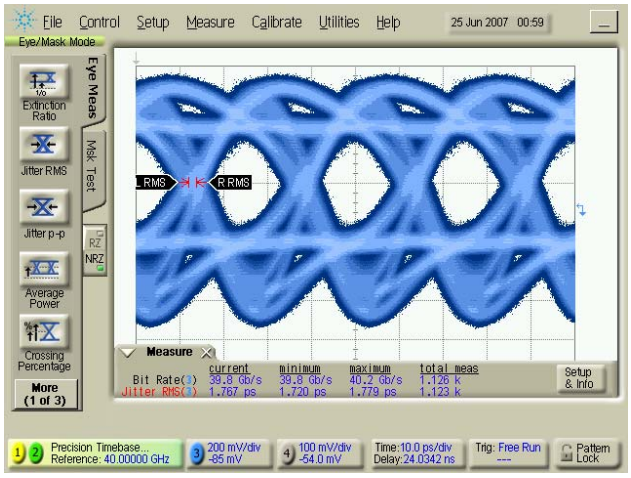


**Fig. 12.** $2^{31}$-1 40-Gb/s output eye diagram with 180% pre-emphasis at 125°C.

The voltage swings in the eye diagram measurements should be multiplied by 1.25 to reflect the values expected with a 75Ω load, as intended for this driver. The maximum output amplitude is at least $3.6V_{pp}$ per side as measured in Fig. 11 at 38 Gb/s. The driver is functional at 40 Gb/s up to 125°C as seen in Fig. 12.

## V. Conclusion

A differential distributed cable driver IC using n-channel MOSFETs and HV-HBTs has been designed and fabricated in a production 0.18µm SiGe BiCMOS process for 40-Gb/s data transmission over standard 75Ω coaxial cable. The IC achieves $3V_{pp}$ per side and features adjustable pre-emphasis, output swing control and DCD control. Measurements indicate that the IC could also be used as a 50Ω EA modulator driver. To the best of the authors' knowledge, this work marks the first 40-Gb/s driver with large output swing and adjustable pre-emphasis. Together with the equalizers in [5] and [6], the driver represents a key milestone towards the single-chip integration of a 40-Gb/s transceiver with equalization aimed at compensating up to 50dB of loss over 75Ω coaxial cable.

## Acknowledgement

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