5GHz SiGe HBT MONOLITHIC RADIO TRANSCEIVER WITH TUNABLE FILTERING

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ABSTRACT

A W-CDMA compliant, fully integrated 5GHz radio transceiver was realized in SiGe technology with on-chip, tunable, VCO-tracking filters. It allows for wide band, up to 20MHz, modulation schemes demonstrating a SSB receiver NF of 5.9dB, 40dB on-chip image rejection, IP1 of -22dBm and larger than 70dB LO-RF isolation. The VCO phase noise is -100dBc/Hz and -128dBc/Hz at 100kHz and 5MHz offset, respectively. The transmitter output compression point is 10dBm. The image rejection in the transmitter is better than 40dB and all spurious signals are 40dB below the carrier.

INTRODUCTION

Based on the proliferation of high speed wireline Internet access at 2-10Mb/s, one can envision future demand for wireless access at comparable rates. Unlike the crowded 2GHz band, the 5GHz bands, with more than 300MHz available, appear extremely attractive for high-speed applications such as wireless ATM and wideband fixed-radio access, allowing several HDTV channels and Internet services, as a potential low-cost alternative to 28GHz LMDS. A 5GHz radio transceiver has recently been reported in Si BiCMOS technology [1]. The VCO and the image reject filters were not included on chip. This paper describes a SiGe HBT 5GHz radio transceiver with superior performance and a higher level of integration, including the VCO and tunable VCO-tracking image reject filters. In addition, in order to minimize on-chip cross-talk and reduce the impact of package inductance, a fully differential architecture was employed.

CHIP ARCHITECTURE

Fig. 1 shows a block diagram of the new SiGe HBT radio transceiver. The chip contains an LC-tuned, 1GHz-to-5GHz transmitter and 5GHz-to-1GHz receiver, as well as a shared 4GHz varactor-tuned LC VCO. Varactor-tuned 3GHz image reject filters are integrated into both the transmitter and the receiver. The image rejection filters remove the image signal by notch rejection [2]. The notch frequency tuning is designed to track the on-chip VCO over 350MHz with 1GHz separation, allowing for a fixed IF of 1GHz. The VCO has a differential varactor-tuned LC architecture with two inductors[3]. IF sampling with a bandpass ΔΣ ADC [4], allowing for further integration, or a more conventional 2nd IF scheme can be used to process the 1GHz data signals coming on and off this chip.

The transmitter features 17 on-chip inductors and a fully differential architecture with a double-balanced 1GHz-to-5GHz upconverter, followed by a 5GHz driver amplifier with built-in 3GHz image-rejection, and a linear power amplifier stage. The outputs of the upconverter, driver and power amplifier are LC tuned at 5GHz.

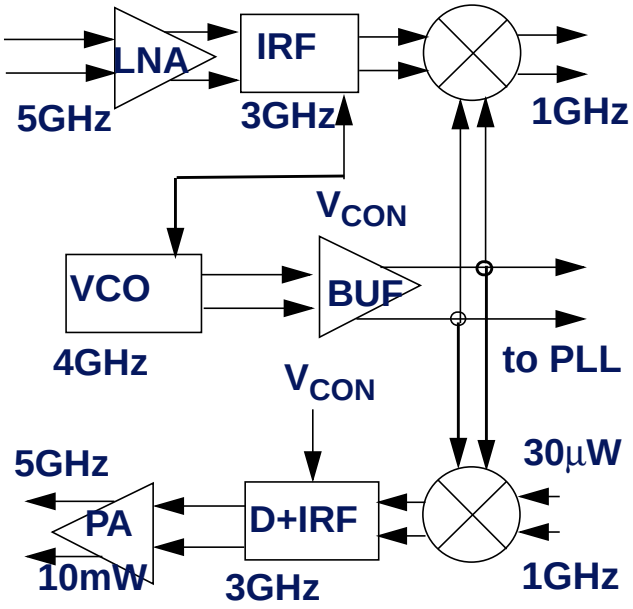

Figure 1: Block diagram of the single chip 5GHz transceiver.

The fully differential receiver has 14 on-chip inductors and contains a 5GHz tuned LNA which drives an RF- and IF-tuned double-balanced mixer. The low noise design of the mixer and LNA allows for the optimal partitioning of gain across receiver blocks in order to maximize receiver linearity without degrading the overall noise figure [5]. On-chip inter-stage conjugate matching is used throughout and impedance levels are maximized to reduce power dissipation. Transistor sizing and lossless on-chip inductive feedback are employed

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for simultaneous noise and input-impedance matching in both the LNA and the mixer [5]. No external matching components are required at the chip boundaries since the matching is entirely provided by on-chip and bondwire inductances.

FABRICATION AND LAYOUT

The radio transceiver was fabricated in IBM's SiGe HBT technology. All 33 inductors, multistripe varactors, MIM capacitors and most multistripe transistors were custom designed for this particular chip. No prior device models or measured data were available. Fig.2 shows f_T and f_{MAX} characteristics as a function of collector current, as measured in our lab on a "fast" wafer. The appropriate number of base and collector contacts for multistripe transistors ensures that, as the collector current scales with transistor size, both f_T and f_{MAX} remain constant.

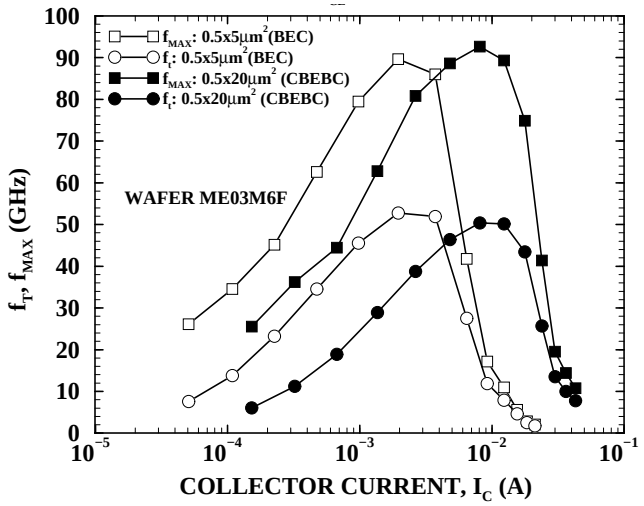

Figure 2: Measured f_T and f_{MAX} as a function of collector current for 0.5x5μm^2 and 0.5x20μm^2 transistors at V_{CE}=1V. BEC stands for 1 base, 1 emitter and 1 collector contact geometry. Similarly CBEBC stands for collector-base-emitter-base-collector geometry.

Substrate tiedowns were used in conjunction with trenched n-wells and ample first metal ground planes to reduce cross coupling through the substrate. Each circuit block was surrounded by a sufficiently wide guard-ring made of the above combination. Wide, low-inductance top metal lines over first metal planes were used to provide bias supply. Appropriate resonance-free MIM-capacitor based de-coupling was provided on each supply line. Such isolation and bias de-coupling techniques are critical for achieving spurious-free and stable operation of the single chip radio. The chip was statistically simulated over process variations after layout extraction, including parasitic distributed interconnect [6]. The chip worked at first pass with performance within 10% of nominal simulation. The discrepancies are in the resonant frequency of the LC tanks, measured inductance and varactor capacitances being 5-10%, and 15-20%, respectively above nominal.

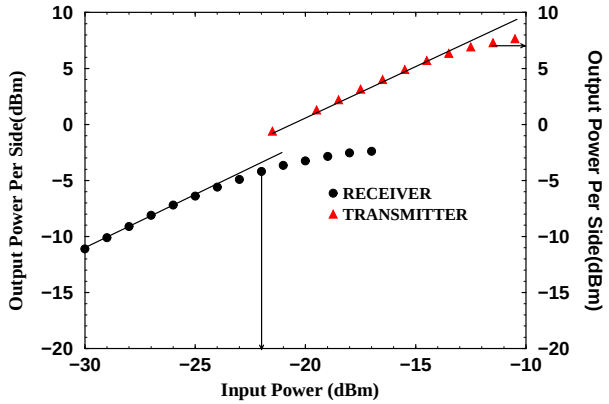

Figure 3: Transceiver 1dB compression point measurement with on-chip VCO. The signal is applied and extracted single-ended. The unused input and output are terminated in 50Ω.

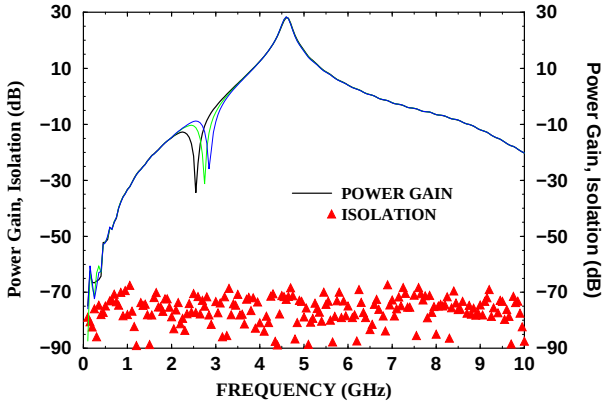

Figure 4: Transmitter single-sided small signal gain and isolation. The image reject filter control has been set at 1.5V, 2.5V and 3.5V. The LO inputs to the upconverter have 0.4V differential bias.

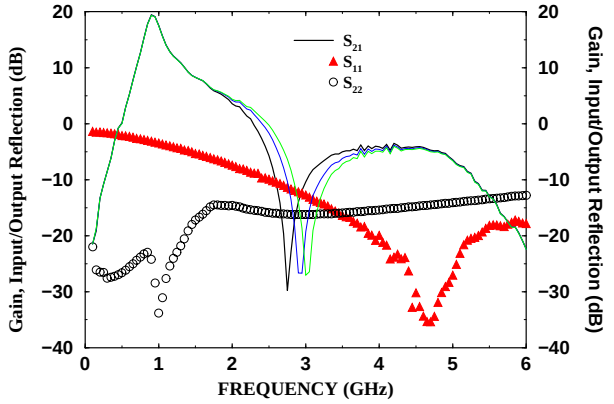

Figure 5: Receiver single-ended S parameters. The image reject filter control has been swept as in Fig.4 to demonstrate tunability. The LO inputs to the mixer have 0.4V dc differential bias.

EXPERIMENTAL RESULTS

Fig.3 shows a transmitter output compression point of +7dBm per side. The resultant differential conversion gain is 26dB. The measured small-signal gain of the transmit path

when the upconverter is biased as an amplifier is given in Fig.4. On-chip image rejection is better than 40dB throughout the 350MHz VCO tracking range, as shown in Fig.7. RF-IF isolation is higher than 75dB up to 10GHz, the measurement being limited by the dynamic range of the network analyzer. In addition to the image suppression, all other spurs are more than 40dB below the carrier, even with single-ended output.

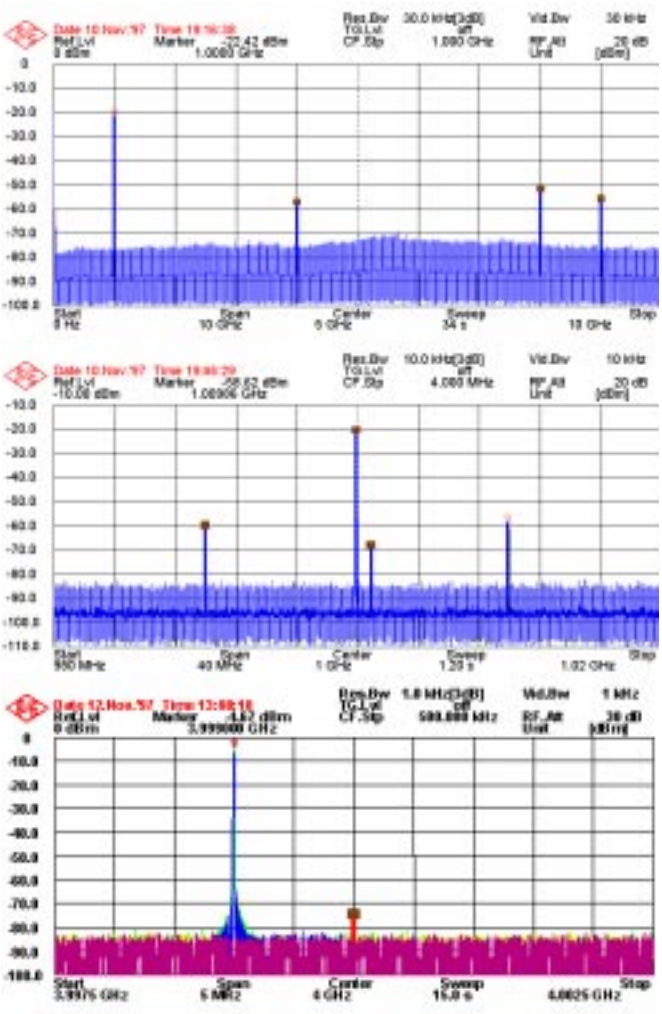

Figure 6: Top: Receiver single-ended IF spectrum showing the 4GHz LO, 1GHz IF, 8GHz and 9GHz spurs. Middle: Receiver IF output showing 40dB image rejection over a 20MHz channel bandwidth obtained by sweeping the frequency of an image signal applied around 3GHz. Bottom: Receiver LO-to-RF leakage with two superimposed traces: i) output spectrum of the external LO set at 3.999GHz and -4.67dBm, ii) RF leaking signal of -76dBm at a single-ended RF input with the LO tuned to 4GHz.

The receiver has 19dB single-ended gain, 25dB differential conversion gain, input and output return loss better than 20dB (Fig.5), and an input compression point of -22dBm, Fig.3. More than 40dB image rejection, tunable over 350MHz, is achieved on chip over a 20MHz-wide channel and is better than 50dB for narrower channels, Fig.6. The measured single-ended receiver noise figure is 5.9dB SSB. The differential receiver noise figure is expected to be 4.5dB based on simulated and measured single-ended noise figure of half-circuit (2.5dB) and differential (4.2dB) stand-alone LNAs. The single-ended and differential S-parameters of the LNA were measured using an SPTS-4 system from ATN Microwave.

The VCO tuning range is larger than 350MHz for the nominal control voltage range of 1.5V to 3.5V, as illustrated in Fig.7. Fig.8 shows the phase noise of a stand-alone buffered version of the VCO as -100 and -128dBc/Hz at 100kHz and 5MHz, respectively, from a 3.91GHz carrier. The buffered output power is adjustable up to -6dBm and draws 20mA from a 3.5V supply. The VCO core itself requires 5mA.

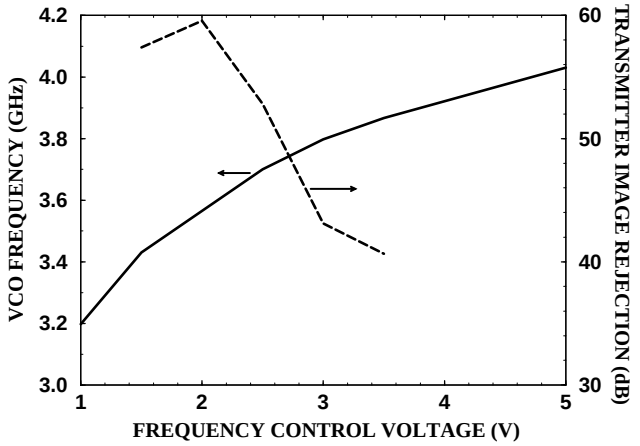

Figure 7: VCO frequency and transmitter image rejection as a function of the frequency control voltage applied to the VCO and tracking image reject filter. Typical control range is 1.5V to 3.5V.

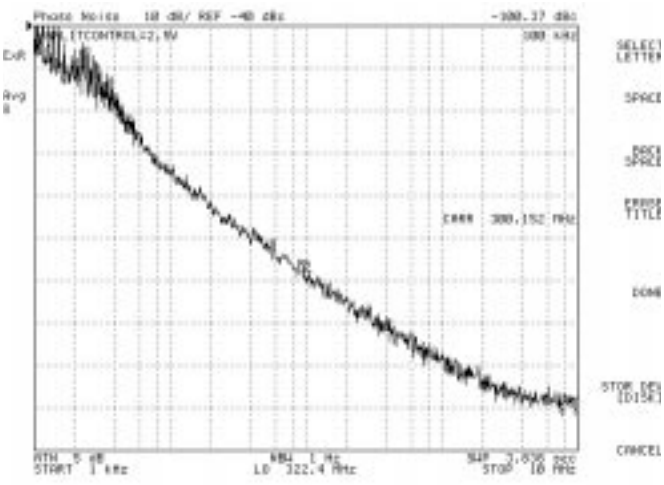

Figure 8: Measured VCO phase noise at 100KHz offset from the 3.91GHz carrier. A double-conversion scheme was used in the measurement with an HP4352B phase meter and an HP70427A downconverter having an IF of 300MHz, as displayed.

The transceiver operates from a 3.5V supply and, with the buffered VCO on, draws 125mA in transmit mode and 45mA in receive mode. The total transceiver area is 4.2x2.6

mm^2, Fig.9. All measurements reported here have been performed on wafer using multiple wedge probes. Separate, packageable versions of the transmitter and of the receiver have also been fabricated to be used in applications where VCO phase noise requirements are more stringent.

SUMMARY

These results, including VCO noise, demonstrate that W-CDMA compliance is achievable at 5GHz with a fully integrated transceiver in cost-competitive Si-based technology. Measured on-chip isolation is better than 75dB up to 10GHz and remains above 60dB up to 26GHz, suggesting that integrating the low-frequency part of a complete radio is feasible without crosstalk problems. The linearity, image rejection and noise figure of the transceiver make it versatile enough to permit various types of modulation and coding schemes such as GMSK, QPSK and CDMA. For applications requiring higher output power, an external power amplifier must be provided.

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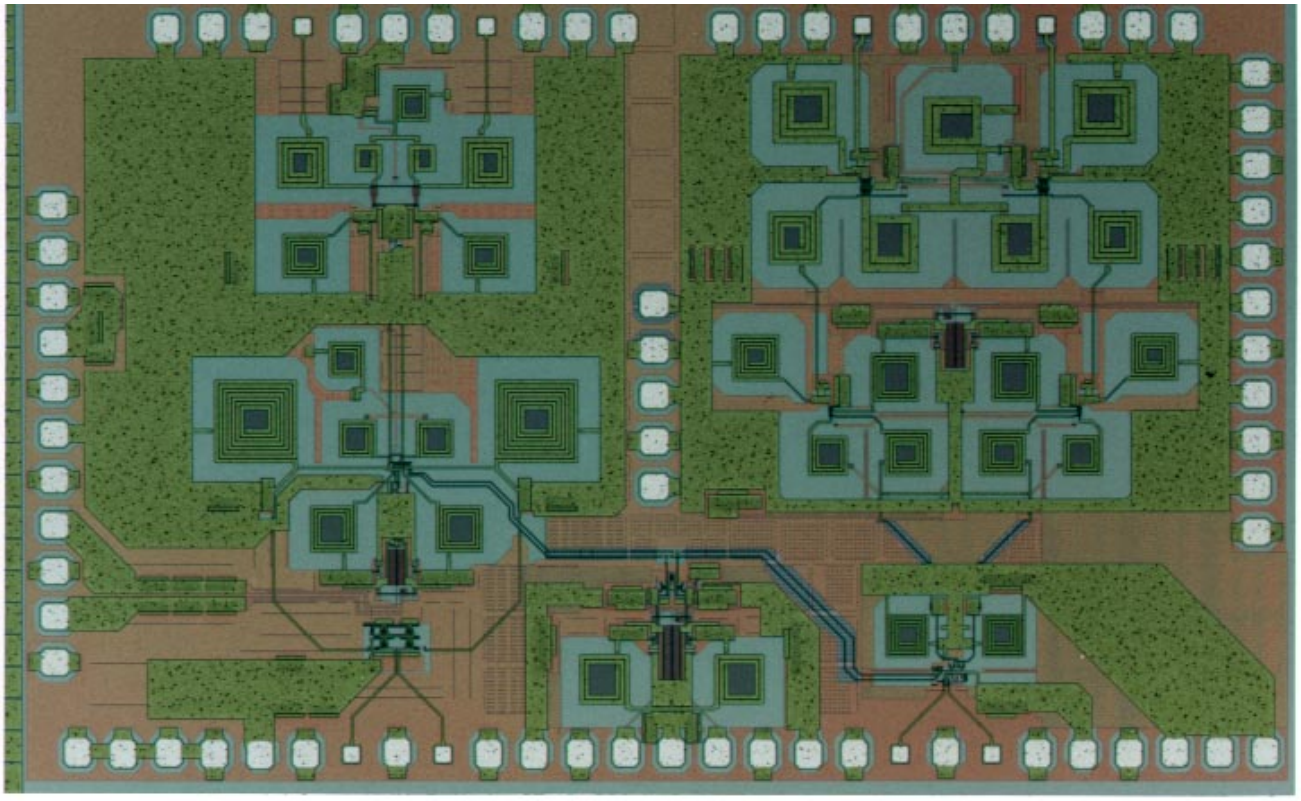

Figure 9: Transceiver micrograph showing the receiver at the left, transmitter at the right, and VCO at the bottom. The 5GHz differential RF ports are at the top while the 1GHz IF ports are at the bottom.