A Low-Noise 40-GS/s Continuous-Time Bandpass $\Delta\Sigma$ ADC Centered at 2GHz

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***Abstract*— A 2-GHz, Continuous-Time Bandpass $\Delta\Sigma$ Analog-to-Digital Converter sampled with a 40-GHz clock was implemented in a 130-nm SiGe BiCMOS technology. It achieves an SNDR of 55 dB and 52 dB over 60 MHz and 120 MHz, respectively, and an SFDR of 61 dB with a single-ended IIP3 of +4 dBm. The center frequency is tunable from 1.8-2 GHz. It employs a G_m-LC_{VAR} filter based on a MOS-HBT cascode transconductor with an NF_{MIN} of 2.3 dB. The ADC dissipates 1.6 W from a 2.5-V supply with a figure of merit of 18 pJ/sampled bit, including the contribution of the 40-GHz clock distribution network.**

***Index Terms*— Analog-to-digital converter, continuous-time, delta-sigma, direct RF sampling, SiGe BiCMOS.**

I. Introduction

Continuous-Time (CT) $\Delta\Sigma$ modulators ($\Delta\Sigma$M) are commonly used in high-speed Analog-to-Digital Converters (ADCs) due to their high resolution, low complexity and inherent anti-alias filtering. Such an ADC may potentially replace the analog blocks (excepting the VCO and, perhaps, the LNA) of a wireless receiver and directly digitize the RF signal. To process the entire system bandwidth (BW), as required in a base station receiver, a large oversampling ratio (OSR) is needed. With the advent of deep submicron silicon technologies with f_T larger than 150 GHz, it is now possible to increase the sampling rate of the ADC to the mm-wave range and further improve performance. Compared to other bandpass (BP) ADC designs with GHz clocks [1]–[4] and operating from 3.3 V or higher supplies, this work employs a new, highly linear and low-noise BiCMOS cascode filter topology, which is biased from a 2.5-V supply. The 40-GHz clock frequency is two times larger than in any previously reported $\Delta\Sigma$ ADCs, opening the path for mm-wave sampling ADCs.

II. System Level Architecture

Figure 1 shows the system level architecture of the $\Delta\Sigma$ ADC. It is based on a classical feedback topology with 2 resonators and feedback paths. The BP loop filter consists of two G_m-LC stages. A Master-Slave-Master (MSM) D-type flip-flop (DFF) with 5 ps rise and fall times [5] is used as a comparator and quantizer. Feedback is applied through two current steering RZ DACs. While the MSM topology compensates for metastability, it introduces an additional half-clock cycle delay in comparison to a simple MS implementation. To ensure that the ADC is stable in the presence of excess loop delay [1], the tail currents of the feedback DACs were set to 15 mA and 45 mA, respectively. A second technique that helps mitigate the delay is the choice of a RZ instead of NRZ pulse. A loop with RZ pulse can tolerate delays of up to half a clock cycle without SNDR loss. This becomes important as clock frequencies exceed 1/5 of the transisor f_T [1]. Since the output digital stream has 40-Gb/s content, a 50-Ω driver with 50-GHz BW [5] was employed to drive the signal off-chip.

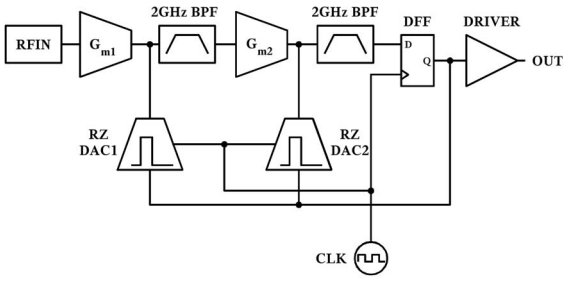

Fig. 1. System level ADC model.

III. Loop Filter

A. Filter Design

The circuit schematic of the 4th order loop filter is shown in Fig. 2. The filter tank consists of a LC-C_{VAR} combination, with L_C = 3.8 nH and C_C = 2.3 pF. The varactor was added to provide a means of adjusting the center frequency against process variations. Its capacitance C_{VAR} varies between 0.4 and 0.8 pF. It is significantly smaller than C_C in order to maintain a high Q while still providing $> 10\%$ tunability at 2 GHz. The transconductance of each stage is found from system level simulations to be g_{m1} = 22 mS and g_{m2} = 10 mS respectively. The combination of n-MOSFET and HBT transistors in the cascode amplifier provides maximum linearity and isolation allowing for lower power supply than it is otherwise possible with an HBT-only implementation. Since the design goal for the filter is linearity rather than gain, we make use of the intrinsic linearity of n-MOSFETs when biased at the peak-g_m current density of 0.4 mA/μm (Fig. 3). Under peak-g_m bias, the n-MOSFET does not require inductive or resistive source degeneration for improved linearity ($>$ 0.5 Vpp linear swing on the gate) and the noise figure (NF) is only slightly degraded from its minimum value at 0.15 mA/μm. A degenerated HBT-HBT cascode would increase the NF of the circuit for the same linearity. The linearity is further improved by the higher output voltage swing and output resistance of the HBT in the MOS-HBT cascode. The degeneration inductor L_E is used

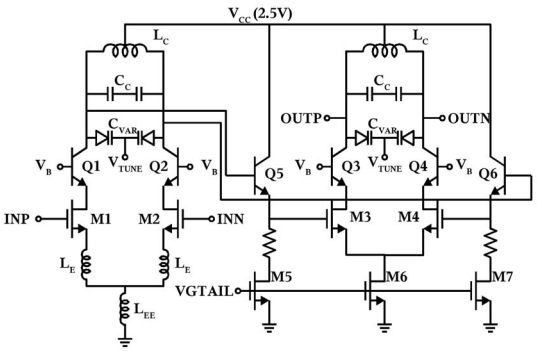

Fig. 2. Circuit schematic of 2-stage loop filter.

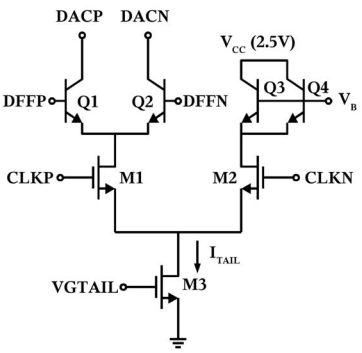

Fig. 4. Circuit schematic of RZ DAC.

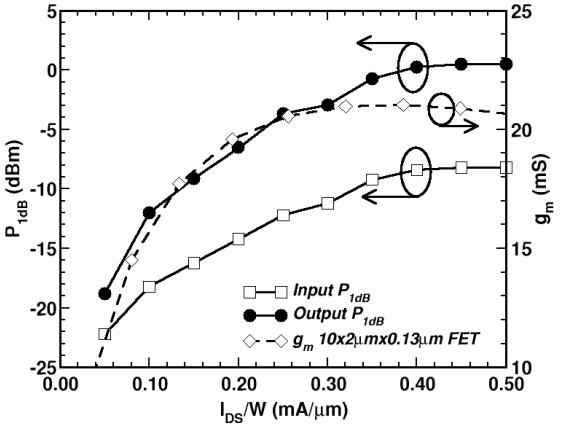

Fig. 3. Measured filter linearity and g_m of n-MOSFET vs current density.

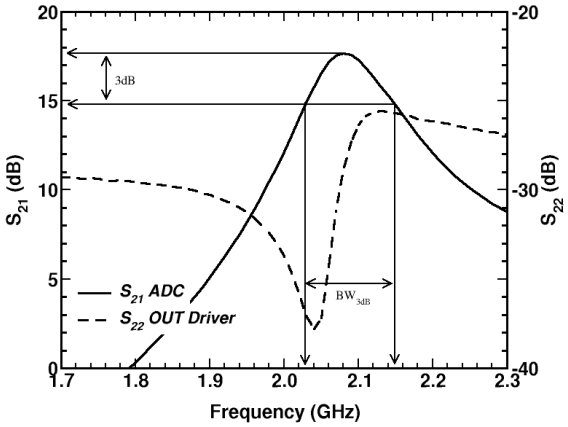

Fig. 5. Measured ADC single-ended S-parameters.

for matching purposes to make the real part of the input impedance equal to 50 Ω. The common mode inductor L_{EE} suppresses the even order harmonics of the first transconductor with minimal noise contribution. Both filter stages are biased at the peak-g_m current density.

B. Filter Characterization

Single-ended S-parameter, NF and differential P_{1dB} and IP3 measurements were performed on wafer on a separate filter test structure, identical to the one used in the ADC. The measured NF_{MIN} is 2.29 dB at 2 GHz. As can be seen in Fig. 3, the maximum value of $P_{1dB,out}$ = 0.5 dBm occurs at 0.4 mA/μm current density, which coincides with the flat region of the transistor g_m-I_{DS} transfer characteristic. The differential IIP3 and OIP3 of the filter are -0.5 dBm and 9 dBm, respectively.

IV. Feedback DACs

Figure 4 shows the DAC topology, similar to the one in [6] but implemented using MOS-HBT cascodes. When both M1 and one of Q1-Q2 turn on, I_{TAIL} is subtracted from the feedback node at the resonator tank. The clock signal switches the differential pair M1-M2 and generates the RZ current waveform. Transistors Q3-Q4 act as dummy loads to ensure the symmetry of the waveform. The external clock signal is distributed to the 3 latches and 2 DACs by a broadband clock tree. The latter comprises a cascade of MOS-HBT cascode inverters with series and shunt inductive peaking to extend its bandwidth beyond 40 GHz.

V. Measurement Results

The ADC was tested on wafer using 65-GHz GGB probes. S-parameter, eye diagram and power spectrum measurements were performed. Figure 5 illustrates the measured S_{21} and S_{22} in the passband of the ADC with the clock tree turned off. The filter Q is 17.5 and the 3-dB BW is 120 MHz. Large signal measurements were conducted by directly connecting the output of the circuit to a 50-GHz Agilent E4448A spectrum analyzer (PSA) and the other output to an Agilent Infiniium DCA-86100C oscilloscope with 70-GHz remote heads. The clock signal was provided from a low phase noise Agilent E8257D PSG signal source and the RF input signals were obtained from Agilent E4422B and 83650B signal sources. The 40-Gb/s output eye diagram is depicted in Fig. 6 for a 2-GHz input, when the feedback loop is turned off and the analog input is sampled by the quantizer at 40 GS/s. The eye jitter is less than 0.4 ps rms, posing no problem to the ADC resolution. The simulated spectrum is illustrated in Fig. 7 for an input power of P_{IN} = -10 dBm and 32768 FFT points. The simulated SNDR = 51 dB is calculated over a bandwidth of 60 MHz. Figure 8 shows the measured $\Delta\Sigma$ ADC output

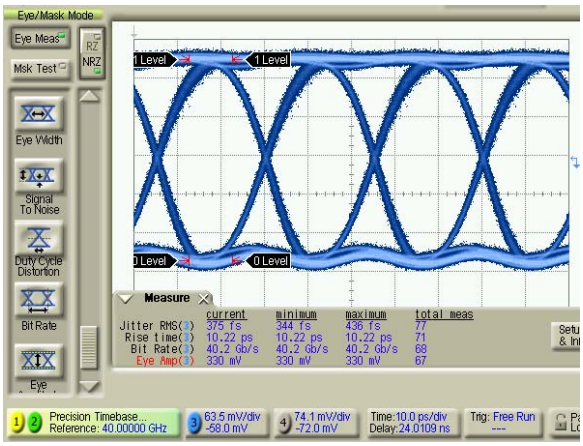

Fig. 6. Output eye diagram at 40Gbps.

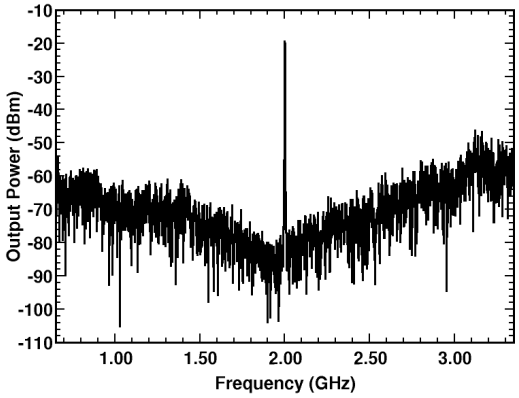

Fig. 7. Simulated ADC spectrum (NFFT=32K).

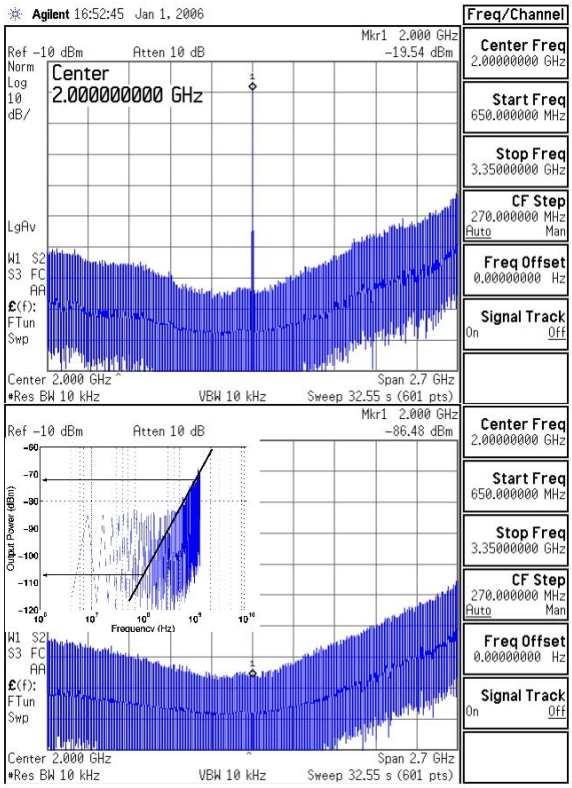

Fig. 8. Measured ADC spectrum for 2-GHz input and no input.

spectrum with and without an input sinusoidal signal at 2 GHz. Losses in the test setup have not been de-embedded. The loop remains stable in the absence of input signal and maintains its noise shaping, despite the finite Q of the resonators. The noise shaping in the lower part of the spectrum is $>$ 35 dB/decade, as displayed in the inset. The inset is obtained by shifting the spectrum to 0 GHz and plotting on a log scale. The single-ended IIP3 = +4 dBm, P_{1dB} = -4 dBm, and SFDR = 61 dB of the ADC were obtained from two-tone measurements with 10-MHz spacing, as shown in Fig. 9. The ADC linearity is better than that of the filter test structure reported in Section IIIB due to the application of feedback. The single-ended SNDR is plotted as a function of input power for 10-MHz, 60-MHz and 120-MHz bandwidths in Fig. 10. The SNDR was calculated from the power spectrum by integrating the noise around the input signal over the bandwidth of interest using the built-in integration function of the PSA. To accurately measure the SNDR, the resolution BW of the PSA was lowered until the noise floor remained constant. The noise floor obtained in this manner represents the quantization noise and the thermal noise contribution from the circuit itself. The ADC achieves an SNDR of 63 dB, 55 dB and 52 dB over 10 MHz, 60 MHz and 120 MHz, respectively, for a single tone at 2 GHz. The peak SNDR vs bandwidth plot can be found in Fig. 11. The simulated SNDR is pessimistic because the FFT has only 32K samples, corresponding to an FFT bin of 1.22 MHz, 100 times larger than the PSA resolution BW. This raises the noise levels of the simulated spectrum. A larger FFT size, however, would make the simulation time prohibitive at 40-GHz sampling rates. As can be seen in Fig. 8, the ADC passband has an approximately flat noise distribution. The SNDR can be further improved by adding cross-coupled negative resistance cells across the filter tanks to increase their Q [1].

The circuit was implemented in a 130-nm SiGe BiCMOS process and occupies 1.52$\times$1.58 mm^2. It dissipates 1.6 W from a 2.5-V power supply. Half the power (0.8W) is consumed by the clock path and output driver with the rest being dissipated by the DACs, filter, and quantizer. The chip microphotograph is shown in Fig. 12. Table I summarizes the performance of recently-published ADCs. The ADC in this work achieves the lowest $FOM = P_{DC}/(2^{ENOB} \times 2BW)$ among the BP designs and comparable performance to the low-pass ADC of [6], which was implemented in a 205-GHz f_T InP technology.

VI. Conclusion

A 4th order Continuous-Time BP $\Delta\Sigma$ ADC, clocked at 40 GHz, has been demonstrated at 2 GHz. The loop filter employs two G_m-LC stages with MOS-HBT cascode transconductors for high linearity, low-noise and lower supply voltage when compared with an all-HBT implementation. The ADC achieves an SNDR of 52 dB over a 120 MHz bandwidth with an ENOB of 8.5 and tunable center frequency between 1.8 and

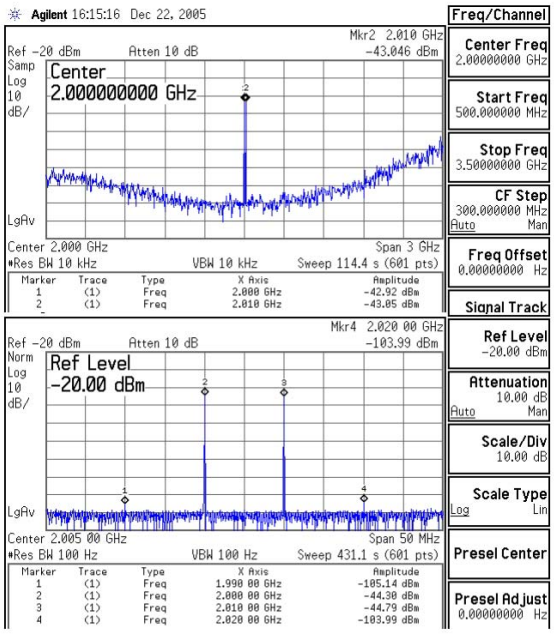

Fig. 9. ADC two-tone spectra at 2 GHz with P_{in}=-30 dBm.

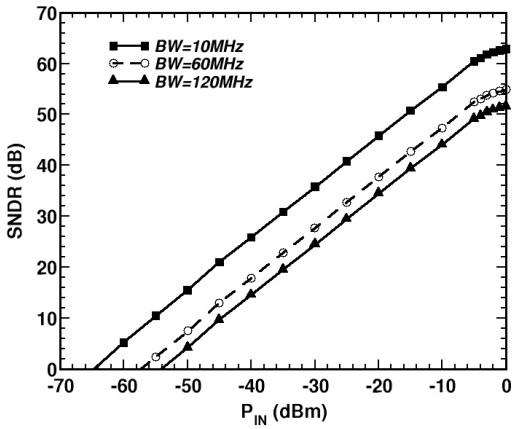

Fig. 10. Dynamic range for a 2-GHz single tone input.

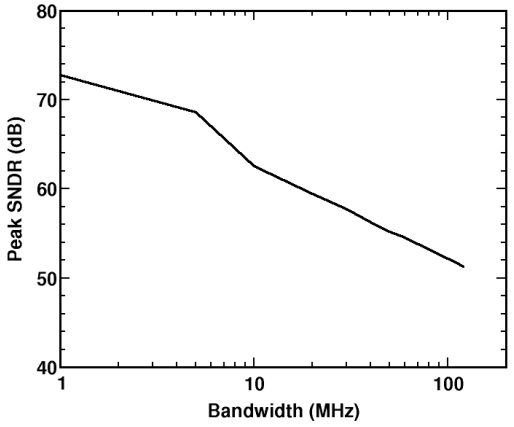

Fig. 11. Peak-SNDR vs bandwidth for a 2-GHz single tone input.

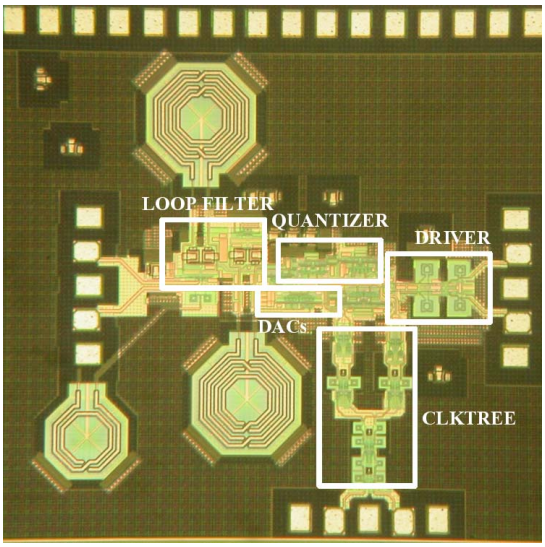

Fig. 12. Chip microphotograph.

TABLE I
COMPARISON OF MM-WAVE ΔΣ ADCS

Ref	Process	f_S (GHz)	f_C (GHz)	BW (MHz)	$SNDR$ (dB)	FOM (pJ/bit)
[2] (BP)	Si	3.8	0.95	0.2	49	1473
[3] (BP)	InP	3.2	0.8	25	41	400
[4] (BP)	InP	4	1	60	47.4	135
[6] (LP)	InP	8	-	62.5	57.4	24
This work	SiGe	40	2	60	55	26
	BiCMOS	40	2	120	52	18

2 GHz. The SFDR is 61 dB and the FOM is 18 pJ per sampled bit. These results demonstrate for the first time that mm-wave sampling can be applied to BP ΔΣ ADCs in silicon.

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