60-GHz PA and LNA in 90-nm RF-CMOS

Terry Yao[1], Michael Gordon[1], Kenneth Yau[1], M.T. Yang[2], and Sorin P. Voinigescu[1]

[1]Edward S. Rogers Sr. Department of Electrical and Computer Engineering, University of Toronto, 10 King's College Rd, Toronto, ON Canada M5S 3G4, e-mail: tyao@eecg.toronto.edu

[2]TSMC, 9 Creation Rd. I, Science-Based Industrial Park, Hsin-Chu, Taiwan 300-77, R.O.C.

***Abstract* — 60-GHz power (PA) and low-noise (LNA) amplifiers implemented in a 90-nm RF-CMOS process with thick 9-metal layer copper backend and transistor f_T/f_{MAX} of 140GHz/170GHz are reported. The PA operates from a 1.5V supply with 5.2dB power gain, a 3-dB bandwidth >13GHz, a P_{1dB} of +6.4dBm with 7% PAE and a saturated output power of +9.3dBm at 60GHz. The LNA features 14.6dB gain, an IIP3 of –6.8dBm, and a simulated NF of 4.5dB, while drawing 16mA from a 1.5V supply. Both circuits employ inductors which reduce the total PA and LNA die sizes to 0.35 x 0.43 mm^2 and 0.35 x 0.40 mm^2, respectively.**

***Index Terms* — CMOS millimeter-wave integrated circuits, characteristic current densities, f_{MAX}, f_T, inductors, low-noise amplifiers, noise figure, power amplifiers, transformers.**

I. Introduction

As CMOS technology is scaled into the nanometer range, the transistor I_D-V_{GS} characteristics in the saturation region become linear while the transconductance, minimum noise figure (NF_{MIN}), f_T, and f_{MAX} improve. Additionally, when biased at current densities between 0.15mA/μm and 0.4mA/μm, these figures of merit (FOMs) become almost insensitive to I_D and V_{GS} variation. In this paper, the potential of 90-nm RF-CMOS for 60-GHz transceiver front-ends is explored in the implementation of two critical building blocks – the power amplifier, demonstrated here for the first time at 60GHz in CMOS, and the low-noise amplifier.

The LNA is a CMOS replica of a noise and impedance-matched, 2-stage cascode SiGe BiCMOS LNA [1]. It employs matching inductors between the CS and CG transistors [2, 3] to compensate for the reduced f_T of the MOSFET cascode stage (Fig. 1). While earlier 60-GHz LNA implementations in 0.13μm CMOS [4, 5] have shown the potential of mainstream CMOS technology for mm-wave circuits, this work proves the benefits of technology scaling and demonstrates FOMs comparable to those of SiGe-HBT LNAs [1, 6]. By relying solely on inductors as matching elements, the LNA and PA exhibit smaller area and lower power consumption than similar 60-GHz circuits.

II. 90-nm RF-CMOS Technology

A. Transistor Performance and Millimeter-Wave Modeling Approach

The measured power gain of 90-nm n-MOSFETs is larger than 8dB at 60GHz and is comparable to that of SiGe HBTs. More importantly, the peak f_T current density remains constant at 0.3mA/μm for different finger widths and for both the CS and cascode configurations (Fig. 1). The optimal NF_{MIN} bias occurs at 0.15mA/μm, close to the peak f_{MAX} current density of 0.2mA/μm and is independent of frequency. Thus, CMOS amplifiers can be optimized simultaneously for low noise and power gain, unlike SiGe HBT ones where the peak f_{MAX} and NF_{MIN} biases are significantly different. Furthermore, as seen in Fig. 2, f_{MAX}, which is directly extrapolated from power gain, changes by less than 11% (corresponding to the 1-dB compression point) for bias current density swings of 0.4mA$_{pp}$/μm, irrespective of the technology node and, in the 90-nm node, for gate voltage swings of 0.5V$_{pp}$. The latter property, in conjunction with a drain voltage swing larger than 2.4V as evident in the experimental output characteristics and load line shown in Fig. 3, can be applied in the design of highly linear power amplifiers. In PAs the transistor must be biased for optimal linearity at 0.3mA/μm.

The gate-source, gate-drain, and parasitic source/drain-bulk capacitance per unit gate width of p/n-MOSFETs remain constant across technology nodes [7] at approximately 1fF/μm, 0.5fF/μm, and 1.5fF/μm, respectively. Similarly, the gate resistance can be easily calculated based on layout geometry, contact resistance and salicided gate poly resistance data. The intrinsic peak transconductance of 90-nm n-MOSFETS biased in saturation is approximately 1.2mS/μm, and the measured noise parameters for a cascode stage biased at 0.15mA/μm are R_n=1880Ω*μm, R_{SOP}=1200Ω*μm and X_{SOP}=50000Ω *GHz*μm. These properties, along with the invariance of the f_T, f_{MAX} and NF_{MIN} characteristic current densities across technology nodes, allow for simple hand design equations of tuned LNAs and PAs, with better than 15% accuracy even at 60GHz and even in the absence of RF models.

B. Millimeter-Wave Passives

A direct benefit of designing at mm-waves is the reduced form factor of on-chip passives. In this work, significant area savings result from the exclusive use of spiral inductors, rather than transmission lines, in the impedance matching networks. Although the inductors are small enough to be implemented as microstrip lines over metal-1 ground planes [8], test structure measurements have indicated that the spiral inductor implementation systematically leads to higher Q while minimizing area. All inductors are designed using the ASITIC software [9], whose accuracy at mm-waves has been repeatedly confirmed through previously fabricated inductor test structures in three different CMOS and SiGe BiCMOS technologies from three different foundries [1, 8, 10]. Inductor 2-π models are used in the circuit schematics to capture the skin effect at high frequencies.

Transformers provide the most compact way for realizing single-ended to differential conversion up to 100GHz [10]. Taking advantage of the multi-level interconnect layers in the 90-nm RF-CMOS process, a vertically-stacked 32x32μm^2 transformer, shown in Fig. 7, has also been implemented. The measured S_{21}, better than –2dB in the 60-94GHz range (Fig. 4), is comparable to an earlier implementation in a 180-nm SiGe BiCMOS process with a thick top Al layer [1].

III. 60-GHz Power Amplifier

A. PA Design

The PA consists of three single-ended, common-source stages biased in class A. Although the cascode topology has higher gain, larger output impedance and flat I_{DS}-V_{DS} characteristic, the single-transistor CS configuration is advantageous in terms of the lower supply voltage required, leading to higher efficiency and good linearity. The tail currents in the three stages are scaled to maximize linearity and are selected based on the required input and output P_{1dB} for that stage. The first stage is biased at the peak f_{MAX} bias of 0.2mA/μm to maximize gain while its source degeneration inductance is set to $L_S = Z_0/2\pi f_T$ for 50-Ω matching. The second and third stages are biased at the optimum linearity current density of 0.28 mA/μm. The transistor width and bias current of the last stage are chosen based on (1) derived from load-line theory. The value of $V_{DS,sat}$ corresponding to 0.28mA/μm is about 0.3V, I_{DC}= W*(0.28mA/μm) and I_{swing} per width is 0.4mA$_{pp}$/μm .

$$P_{1dB} = \frac{I_{swing} \times (V_{DD} - V_{DS,sat})}{4} \qquad (1)$$

A finger width of 1μm was chosen for all transistors as a good compromise between f_T degradation due to the gate-bulk overlap capacitance, C_{GBO}, and reduced gate resistance R_G, thereby increasing f_{MAX}. The input matching network consists of the inductor L_S, which matches the real part of the input impedance to 50Ω, and L_G which cancels the imaginary part of Z_{in}, at 60GHz, as in an LNA. At the output, a 1-stage L-match network consisting of the load inductor L_D and capacitor C_C performs the impedance transformation to 50Ω. Simplicity in the matching networks is critical in minimizing series parasitics, whose effects are more pronounced at 60GHz. Inter-stage matching maximizes power transfer between stages, and improves linearity through the degeneration inductor, L_S. The schematic and chip micrograph of the PA are shown in Figs. 5 and 8. The chip occupies only 0.35x0.43mm^2 and is essentially pad-limited in the vertical direction.

B. PA Measurement Results

The measured PA gain and return loss are shown in Fig. 10 for 3 different dice. With a 1.5V supply, the amplifier has a peak gain of 5.2dB at 61GHz, a 3-dB BW exceeding 13GHz (52-65GHz), with the upper frequency limit being imposed by the operating range of the VNA. Broadband matching is achieved at the output, with S_{22} < -10dB over the 51-65GHz band, while S_{11} is < -10dB in the 60-65GHz range. The isolation (S_{12}) is better than 30dB in the entire measurement range (1-65GHz). Fig. 11 shows the large-signal performance of the PA, where an output P_{1dB} of +6.4dBm and a saturated output power of +9.3dBm were measured at 60GHz, with a 1.5V supply and total current of 26.5mA. The linearity and gain dependence on the bias current of the final stage are shown in Fig. 12. As expected, maximum gain and linearity occur when the final stage is biased at 0.28mA/μm. The output P_{1dB} variation with supply voltage is shown in Fig. 13. A maximum *PAE* of 7.4% and a maximum efficiency of 21.4% are achieved. The gain, and hence *PAE*, can be further improved by replacing the first CS stage with a cascode stage, while maintaining the same power supply. Despite the better linearity of MOSFETs, SiGe HBTs still have a performance advantage in PAs and VCOs due to the larger voltage swings that can be supported.

IV. 60-GHz Low-Noise Amplifier

A. LNA Design

Compared to the CG [5] or CS topologies, the cascode topology [4] exhibits better isolation and higher gain. It also features similar input linearity and simultaneous noise and input impedance matching as the CS stage. For these reasons, the 60-GHz LNA (Fig. 6) in this work employs a 2-stage cascode topology. Series inductors (LM1, LM2) are placed between the CS and CG transistors in each stage to tune out the middle pole of the cascode and to compensate for its lower f_T (Fig. 1). This technique has been successfully applied to low-GHz LNA designs [2] and high-speed HEMT-CML circuits [3]. It is also

proving to be useful now at mm-waves. The input stage transistors are biased at 0.2mA/μm and are sized such that the real part of the optimum noise impedance is about 40Ω. This is a good compromise between noise impedance matching (requiring a device gate width of 24μm), gain, linearity (requiring large current) and insensitivity to impedance mismatch and process variation which calls for low R_n (requiring large current and g_m). The LNA chip micrograph is shown in Fig. 9.

B. LNA Measurement Results

The measured S-parameters of 3 different LNA dice are shown in Fig. 14. The LNA achieves a peak gain of 14.6dB at 58GHz and isolation of better than 32dB. Linearity measurements show an output P_{1dB} of -0.5dBm and an IIP3 of –6.8dBm at 58GHz, with a 50-MHz tone spacing used in the IIP3 measurement (Fig. 15). The LNA noise figure could not be measured at 60GHz due to lack of a downconvert mixer at this frequency. Instead, the noise parameters of a 90-nm n-MOSFET cascode test structure were measured in the 10-26GHz range using a Focus Microwaves system (Fig. 16). The extrapolated NF_{MIN} of the cascode stage at 60GHz is between 2.8dB and 3.6dB, after allowing for measurement scatter. These measurements were found to be in good agreement with simulation results (Fig. 16) and indicate that the simulated 4.5dB LNA noise figure at 60GHz is realistic. Finally, Table 1 shows a comparison of mm-wave LNAs in silicon using the FOM (in units of GHz) as defined by the ITRS [11]. The LNA presented in this paper achieves the highest FOM among all previous implementations in technologies with lower or comparable f_T, f_{MAX} performance.

V. Conclusion

The higher f_T, f_{MAX} and lower NF_{MIN} resulting from CMOS technology scaling directly translates to improved performance in mm-wave radio ICs. This work has shown that lower frequency design techniques can be successfully applied to 60-GHz CMOS radio circuits while the reduced form factors of on-chip passives at mm-waves also lead to significantly lower area consumption than that of similar 5-GHz or 10-GHz circuits.

Acknowledgments

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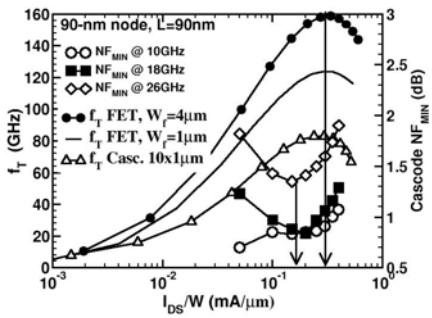

Fig. 1. Measured cascode f_T, NF_{MIN} vs. bias.

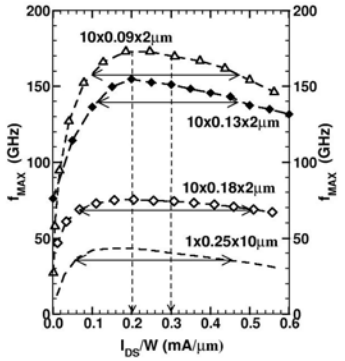

Fig. 2. Measured f_{MAX} across nodes.

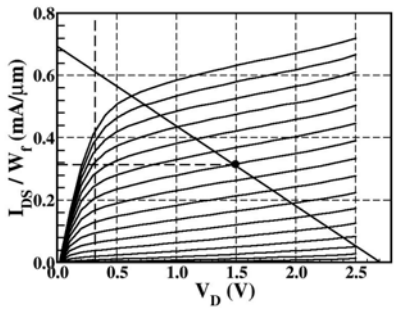

Fig. 3. Optimal load line for 90-nm CS n-MOSFET stage on measured I-V characteristic. The breakdown voltage is larger than 3V.

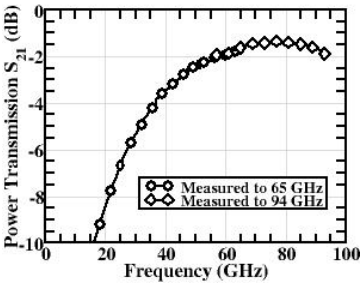

Fig. 4. Measured transformer S_{21}.

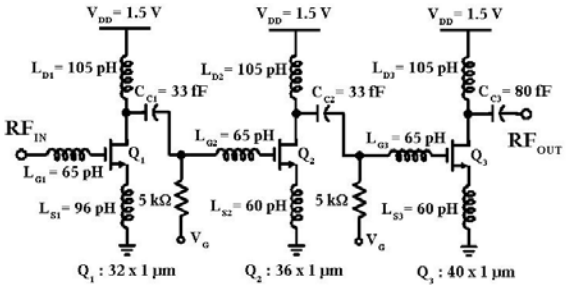

Fig. 5. 60-GHz PA schematic.

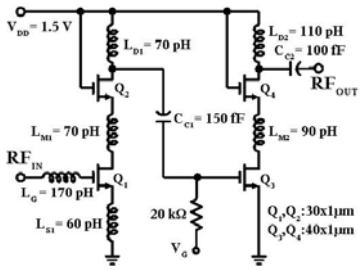

Fig. 6. 60-GHz LNA schematic.

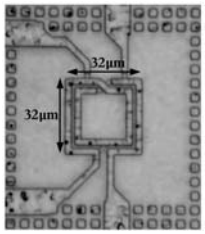

Fig. 7. Stacked 32μm x 32μm transformer in 90-nm RF-CMOS.

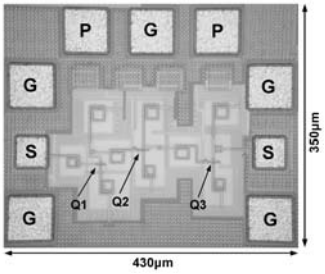

Fig. 8. Die photo of PA (350μm x 430μm).

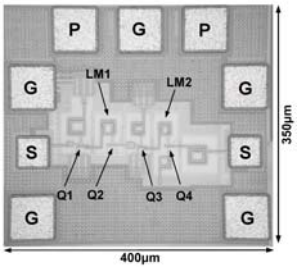

Fig. 9. Die photo of LNA (350μm x 400μm).

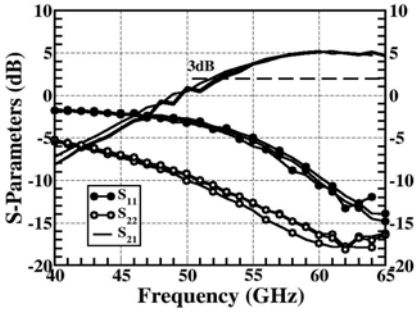

Fig. 10. Measured PA S-parameters across 3 different dice.

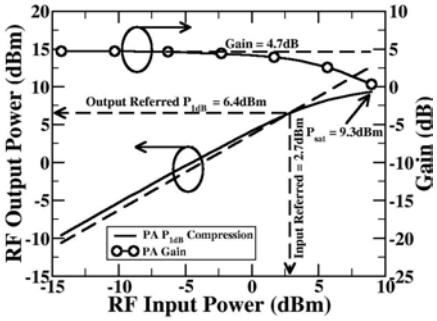

Fig. 11. Measured PA P_{1dB} at 60GHz.

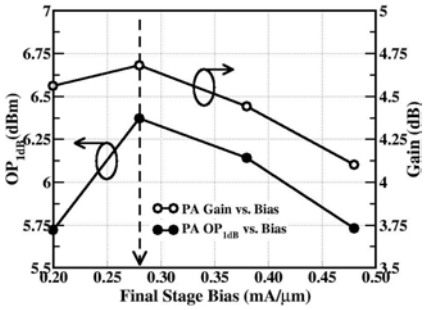

Fig. 12. Measured PA P_{1dB}, gain vs. final stage bias at 60GHz.

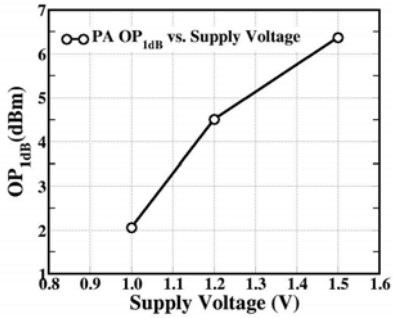

Fig. 13. Measured PA P_{1dB} vs. supply at 60GHz.

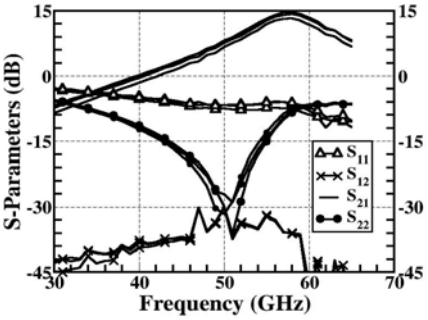

Fig. 14. Measured LNA S-parameters across 3 different dice.

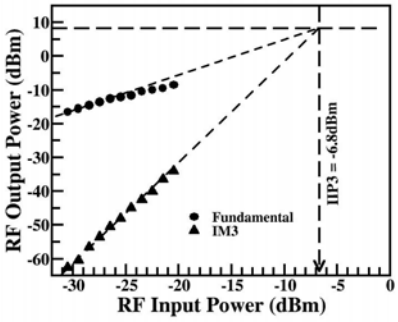

Fig. 15. Measured LNA IIP3 with 50-MHz tone spacing.

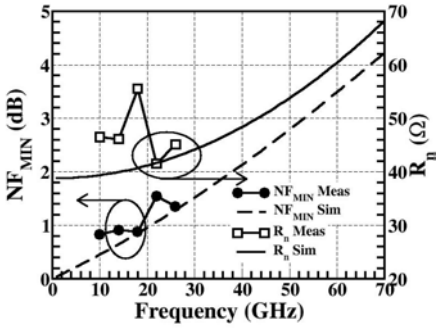

Fig. 16. Meas. vs. sim. $NF_{MIN,}$ R_n for a 40 x 90nm x 1μm n-MOS cascode.

LNA Technology	*f*	*G*	*NF*	*IIP3*	*Pdiss*	*Area*	*FOM*
160/160 GHz f_T /f_{MAX} SiGe HBT [1]	65GHz	14dB	10.5dB (sim)	-6dBm	34mW @ 2.5V	0.3 x 0.4 mm^2	1.2
200/290GHz f_T /f_{MAX} SiGe HBT [6]	61.5GHz	15dB	4.5dB	-8.5dBm	10.8mW @ 1.8V	0.6 x 0.9 mm^2	13.8
90/130GHz f_T /f_{MAX} 130nm CMOS [4]	60GHz	12dB	8.8dB	-0.5dBm (sim)	54mW @ 1.5V	1.3 x 1.0 mm^2	2.1
140/170GHz f_T /f_{MAX} 90nm CMOS (this work)	**58GHz**	**14.6dB**	**4.5dB (sim)**	**-6.8dBm**	**24mW @ 1.5V**	**0.35 x 0.4 mm^2**	**8.1**

Table 1. Comparison of state-of-the-art mm-wave LNAs in silicon.