80/160-GHz Transceiver and 140-GHz Amplifier in SiGe Technology

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***Abstract* — A dual-band mm-wave imaging transceiver, transmitting and receiving simultaneously in the 80-GHz and 160-GHz bands, is fabricated in SiGe HBT technology. The circuit features an 80-GHz quadrature Colpitts oscillator with differential outputs at 160 GHz, a double-balanced Gilbert-cell mixer, and two broadband 70-270 GHz vertically stacked transformers for single-ended to differential conversion. The differential down-conversion gain is -20.5 dB for RF inputs between 70 GHz and 94 GHz and -23.5 dB for inputs in the 150-170 GHz band. The oscillator generates a total of +5.5 dBm at 80 GHz and -5 dBm differentially at 160 GHz. The transceiver with pads occupies 650μm×700μm, is biased from 3.3 V, and consumes 280 mW. A 5-stage amplifier with 17 dB gain and -1 dBm output compression power at 140 GHz is also fabricated and characterized over temperature up to 125 °C and over 14 different wafer splits. These results demonstrate for the first time the feasibility of SiGe BiCMOS technology for products in the 100-160 GHz range.**

***Index Terms* — 140-GHz SiGe amplifier, quadrature oscillator, mm-wave imaging, 160-GHz transceiver, 160-GHz transformer.**

I. Introduction

Mm-wave VCOs operating above 140 GHz have been previously realized in CMOS [1], SiGe [2], and InP [3] technologies. Amplification and integration at the receiver or transmitter level have only been achieved in silicon at frequencies below 80 GHz. This paper reports the first dual-band 80/160-GHz transceiver and the first 140-GHz amplifier implemented in silicon with comparable performance to InP HEMT circuits [4]. Furthermore, the oscillator at the core of the transceiver is the first capable of generating differential signals at 160 GHz, while simultaneously providing quadrature signals at 80 GHz.

II. Transceiver Architecture

In active imaging applications it is customary to use several receivers and transmitters in an array configuration, to increase the resolution of an imager [5]. Integrating such an array at frequencies above 100 GHz poses a significant challenge in terms of LO clock distribution, power, and area. One possible system architecture relies on generating four quadrature signals at the fundamental frequency (80 GHz) together with a differential signal at the second harmonic (160 GHz). Since only one VCO is involved, all its six outputs can be locked to a single 80-GHz PLL, thus saving power and area.

A simplified version of that system was implemented in this paper as the single-chip transceiver whose schematic is illustrated in Fig. 1. In the receiver, the RF signal is converted through an on-chip transformer to a differential signal that drives the down-convert mixer. The 160-GHz LO signal is generated on chip using a quadrature oscillator. One of the 160-GHz signals drives the mixer differentially through another on-chip transformer. The second 160-GHz oscillator signal provides the 160-GHz transmitter output, while two of the 80-GHz quadrature signals form the 80 GHz differential output of the transmitter. The remaining two 80-GHz outputs of the oscillator can be used to drive a divider chain [6] as part of a PLL, but in this version of the transceiver they were terminated on-chip. Thus, simultaneous 80- and 160-GHz transmitter and receiver operation is achieved. The differential IF output of the mixer is matched on-chip over a 10 GHz band. No IF buffer was incorporated in this version of the transceiver.

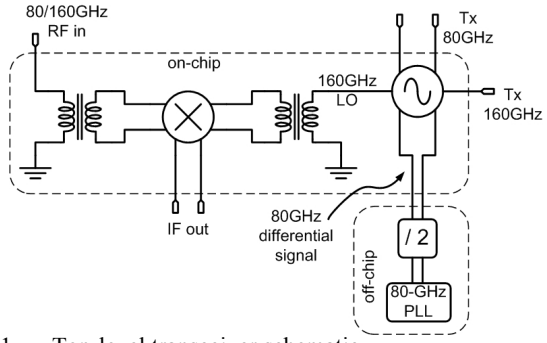

Fig. 1. Top-level transceiver schematic.

III. Circuit Building Blocks

A. Quadrature Oscillator

The oscillator relies on a novel Colpitts topology with 4-fold symmetry, and a star connection of the four tank inductors, as shown in Fig.2. By appropriately terminating the common-mode nodes on the second and fourth harmonics, it effectively couples two differential oscillations such that a fourth harmonic signal is produced at the common nodes. Due to the built-in symmetry, the four 80-GHz fundamental frequency signals operate in quadrature while the two second harmonic signals at 160 GHz are 180° out of phase. Cascode transistors are employed to adequately isolate the outputs from the tank, and to allow for the differential collection of the 160 GHz signals. All transistors are biased at peak-f_T current density to obtain the maximum output swing. Particular attention

was paid to making the oscillator layout symmetric, both for differential and for quadrature signals. The oscillator operates from 3.3 V, and consumes a total of 70 mA. To our knowledge, this is the first quadrature oscillator at 80 GHz and the first differential oscillator at 160 GHz.

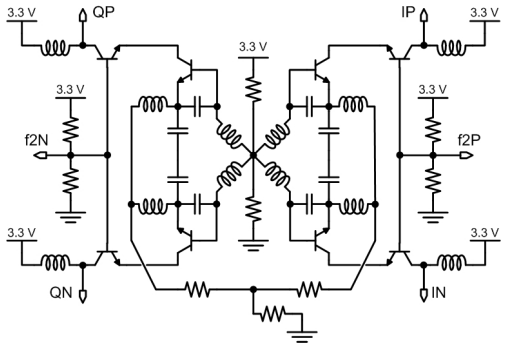

Fig. 2. Schematic of the quadrature oscillator.

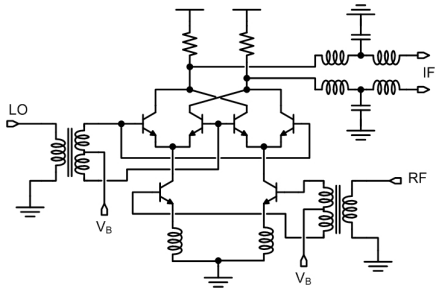

Fig. 3. Down-convert mixer schematic.

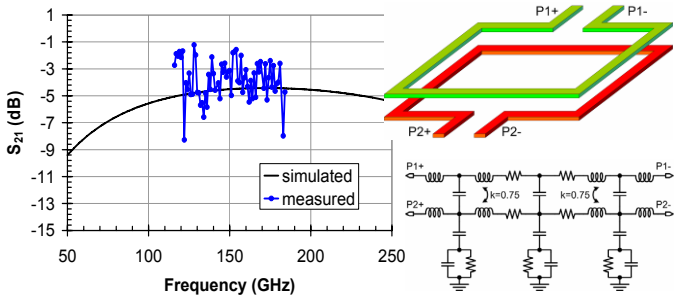

Fig. 4. Left: measured and simulated transformer S_{21}. Right: transformer layout and the 2-π model obtained from ASITIC.

B. Down-convert Mixer with Transformers

A double-balanced Gilbert cell topology with on-chip RF and LO baluns is employed in the receiver, as shown in Fig. 3. The bias for the RF diff-pair and for the LO quad is applied to the center tap of the secondary coil of each transformer. The differential IF output is matched to 50 Ω per side over a broad bandwidth (DC-10 GHz) with the help of a network of inductors and on-chip 50 Ω resistors. The mixer operates from 3.3 V and consumes 15 mA. All transistors have the same size ($l_E = 4$ µm, $w_E = 0.13$ µm) and are biased at peak-f_T current density.

Identical transformers were employed at the RF and LO inputs of the mixer for single-ended to differential mode conversion. Fig. 4 compares the ASITIC-simulated S_{21} of the transformer with measurements, showing excellent agreement. The transformer was optimized for maximum coupling and lowest loss around 160 GHz. The primary and the secondary coils consist of one square turn with a diameter of 20 µm and with 2.5 µm metal width.

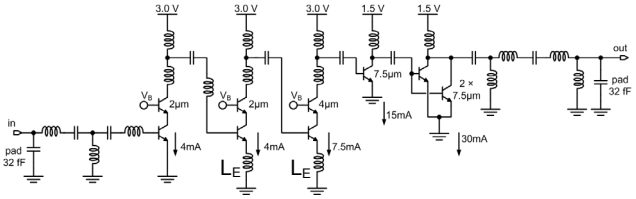

Fig. 5. 140-GHz, 5-stage amplifier schematic.

C. 140-GHz Amplifier

A tuned 5-stage amplifier, illustrated in Fig.5, was also designed and fabricated, but was not integrated in this version of the transceiver to minimize the risks of malfunction. A split inductive load is employed in each cascode stage. The last stage consists of a CE transistor biased at 30mA to obtain a +2dBm ($0.8V_{PP}$) signal in a 50-Ω load. The bias current and emitter length of each preceding stage are scaled by a factor of 0.5 from the output towards the input. All transistors are biased at the peak-f_T current density. This choice of biasing and transistor sizing help maximize the power transfer between stages because the real part of Z_{IN} of each stage (1) is approximately equal to the Z_{OUT} of the previous stage. At the same time, the imaginary part (which is much smaller than the real part) is cancelled using inter-stage series capacitors. In a similar way, the first stage is matched to $50\ \Omega \approx R_B + R_E$, without requiring inductive degeneration. To minimize gain variability, all inductors were implemented with identical geometry and ratio-ed sizes.

$$Z_{IN} = R_B + R_E + \omega_T L_E - j\, f_T / g_m f \qquad (1)$$

IV. Fabrication

The circuits were fabricated in a SiGe HBT technology with f_{MAX} of 300 GHz and f_T of 230 GHz [7]. The process features a digital CMOS backend with 6 copper layers and a regular thickness, top aluminum layer. Die photos of the transceiver and amplifier are reproduced in Fig. 6.

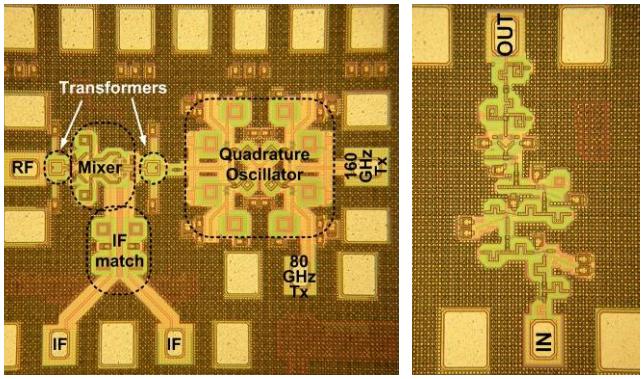

Fig. 6. Left: Transceiver die photo occupying an area of 650µm×700µm, including pads. Right: Amplifier die photo, with an area of 200µm×400µm.

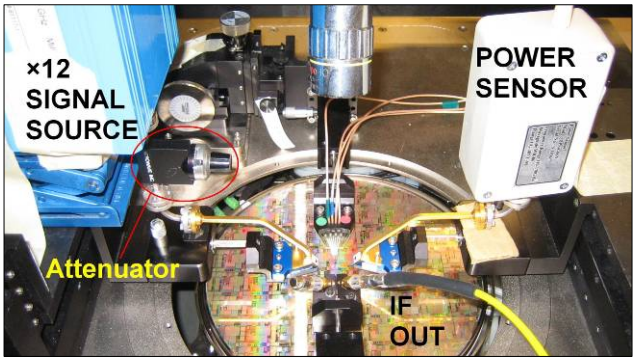

Fig. 7. 160 GHz on-wafer test setup showing the signal source on the left, applied at the receiver input through 110-170 GHz waveguide probes. The 110-170 GHz power sensor is at the right, for transmitter output power measurements. The IF output is collected at the bottom with differential probes.

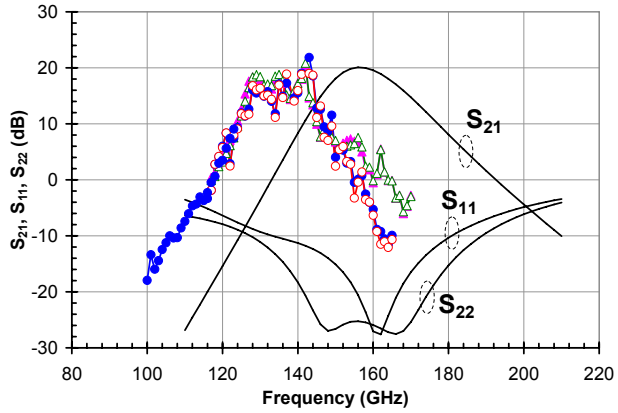

Fig. 8. Simulated S-parameters (lines) and measured S_{21} at 25°C for amplifiers on 2 nominal wafers (circles – using PSA; triangles – using power sensor).

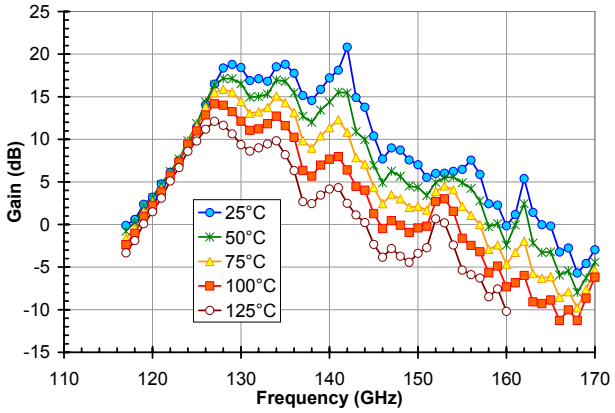

Fig. 9. Amplifier gain over temperature measured using a D-band power sensor.

V. Measurement Results

Measurements were conducted on wafer using 110-170 GHz and 140-220 GHz waveguide probes. A 110-170 GHz OLM signal source, an Agilent E4448A PSA in conjunction with a Farran 140-220 GHz down-convert mixer, and an ELVA 110-170 GHz power sensor were employed for signal generation, spectral, and power measurements. The set-up with power sensor is illustrated in Fig.7. Since the signal source generates multiple tones in the 110-170 GHz band, the power and gain measurements where conducted twice, once with the power sensor and once with the PSA and Farran mixer (Fig. 8). A 0-30 dB variable attenuator was used in the linearity measurements.

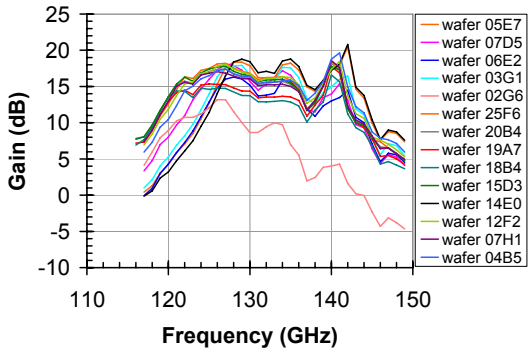

Fig. 10. Amplifier gain curves measured on 14 wafers.

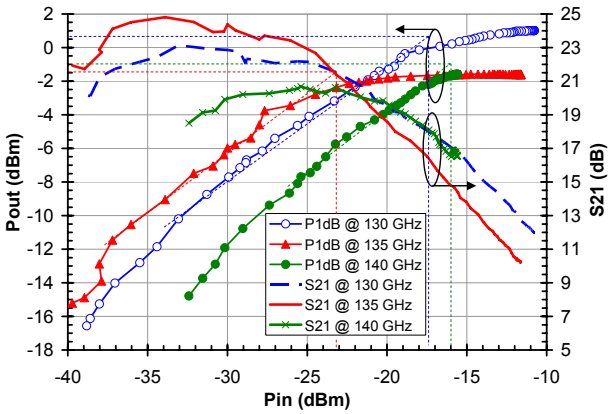

Fig. 11. Amplifier linearity measurements at 3 frequencies.

A. Amplifier

The gain of the amplifier was measured at 25 °C on several dies from two "nominal" wafers from two different runs. The gain remains above 15 dB from 126 GHz to 144 GHz with less than 1 dB variation between the two wafers (Fig. 8). There is a 15% reduction in the center frequency between measurements and simulation which may be explained by the fact that the models were extracted on 2-year old silicon [7] and from S-parameter measurements below 110 GHz. Fig. 9 reproduces the measured gain as a function of temperature. At 140 GHz, the gain decreases from 17 dB at 25°C to 4 dB at 125°C while in the 125-135 GHz range it remains above 10 dB for all temperatures. Finally, the amplifier gain was measured across 14 different process wafer splits in order to identify the best HBT profile for circuits operating above 100 GHz (Fig. 10). The wafer splits differ in the SiGe HBT f_T/f_{MAX} values which vary in a correlated manner between 230/290 GHz and 290/260 GHz. Similar to the temperature behavior, the

gain variation is small at the lower end and increases at the upper end of the bandwidth, with the gain tracking closely the f_{MAX} of the SiGe HBT. This behavior is similar to that of tuned SiGe HBT and CMOS amplifiers at 80 GHz and 60 GHz, where the gain at the higher frequencies depends on transistor f_{MAX} and load Q and rapidly degrades with temperature, whereas, at the lower end of the amplifier bandwidth, the gain is primarily controlled by the ratio of the collector load and emitter degeneration inductors.

Linearity measurements, conducted using the ×12 multiplier source, the attenuator, and the D-band power sensor are illustrated in Fig. 11. The output P1dB is -1 dBm at 140 GHz and +1dBm at 130 GHz.

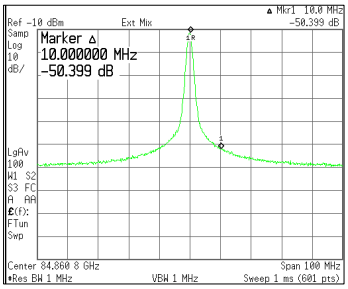

Fig. 12. Measured phase noise of the single-ended 84-GHz output of the transmitter.

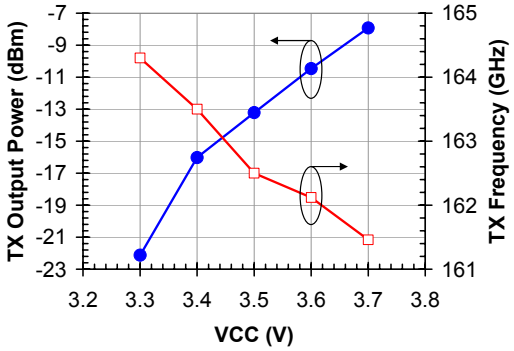

Fig. 13. Single-ended power and frequency of the 160-GHz output of the transmitter vs. the oscillator power supply voltage.

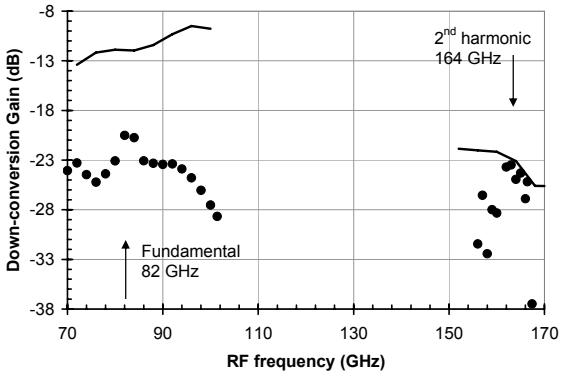

Fig. 14. Differential down-conversion gain of the receiver. Bullets: measured points, lines: simulation. Losses at IF were not de-embedded.

B. Transceiver

The output spectrum of the transmitter at 80 GHz is shown in Fig.12, with phase noise less than -110 dBc/Hz at 10 MHz offset. The TX output signal at 160 GHz is plotted in Fig. 13. After de-embedding losses, the single-ended transmitted power at 161.5 GHz is -8 dBm.

The measured differential down-conversion gain of the receiver is shown in Fig. 14. The RF bandwidth is 10 GHz for receiver operation at 80 GHz, and 8 GHz for operation at 160 GHz. The RF bandwidth of the receiver at 160 GHz is limited by the available power from the RF signal source and by the noise floor of the test setup.

The transceiver and amplifier performance is summarized in Table 1.

Table 1	**Measured**	**Simulated**
Transceiver DC power	295 mW	280 mW
Tx power at 80GHz (single-ended)	-0.5 dBm	+6 dBm
Tx power at 160GHz (single-ended)	-8 dBm	-3.9 dBm
Down-conversion gain at 80GHz*	-20.5 dBm	-11.9 dBm
Down-conversion gain at 160GHz*	-23.5 dBm	-22 dBm
Phase noise at 160 GHz, 10 MHz off.	-110dBc/Hz	
Amplifier DC power	112 mW	112 mW
Amplifier gain (at 140 / 156 GHz)	17 dB	20 dB

* - differential

VI. Conclusion

A dual frequency 80/160GHz transceiver and a 140 GHz amplifier with 17 dB gain were fabricated and characterized. To the best of our knowledge, these are the first such circuits operating at 160 GHz in SiGe HBT technology. They pave the way for higher levels of integration at frequencies above 100 GHz by making it feasible to integrate mm-wave imaging arrays in silicon.

Acknowledgement

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