Design and Scaling of W-Band SiGe BiCMOS VCOs

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***Abstract*—This paper discusses the design of 77–106 GHz Colpitts VCOs fabricated in two generations of SiGe BiCMOS technology, with MOS and HBT varactors, and with integrated inductors. Based on a study of the optimal biasing conditions for minimum phase noise, it is shown that VCOs can be used to monitor the mm-wave noise performance of SiGe HBTs. Measurements show a 106 GHz VCO operating from 2.5 V with phase noise of −101.3 dBc/Hz at 1 MHz offset, which delivers +2.5 dBm of differential output power at 25 °C, with operation verified up to 125 °C. A BiCMOS VCO with a differential MOS-HBT cascode output buffer using 130 nm MOSFETs delivers +10.5 dBm of output power at 87 GHz.**

***Index Terms*—Millimeter-wave integrated circuits, phase noise, process monitor, SiGe BiCMOS technology, voltage-controlled oscillators, W-band voltage-controlled oscillators.**

I. Introduction

MILLIMETER-WAVE applications in the W-band (75–100 GHz), particularly automotive and weather radar at 77 GHz and 94 GHz, have typically been the territory of III-V technology. However, the latest SiGe processes with f_T/f_{MAX} above 150 GHz [1]–[6] allow them to compete directly with III-V technologies for applications in the W-band. W-band radar and radio transceivers require a phase-locked loop, in which the VCO and the frequency divider are the most critical components. Fig. 1 compares the phase noise of state-of-the-art W-band SiGe and CMOS VCOs [8]–[13] along with those presented in this paper [24].

As the level of integration in W-band circuits increases, high yield processes must be developed, and circuit scaling between successive SiGe technology generations must be understood. Key process monitor circuits are required to investigate both issues. Given the complexity and variability of noise parameter measurements above 50 GHz, Colpitts oscillators can be employed to monitor the W-band noise performance of SiGe HBTs, just as ring oscillators are used as CMOS process speed monitors. While such a monitoring technique does not allow the direct determination of SiGe HBT noise parameters, nor the f_T and f_{MAX} of the HBTs, comparing the phase noise and output power of a VCO fabricated on several wafer splits allows the relative performance of the HBTs to be deduced. In this fashion, the profile of the HBT can be optimized for mm-wave performance.

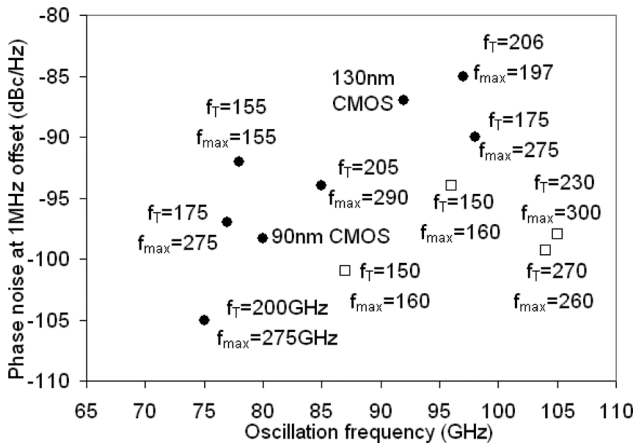

Fig. 1. Phase noise of state-of-the-art SiGe HBT and CMOS W-band oscillators (with process f_T/f_{MAX}) (*this work shown with open symbols* [24]).

This paper, which is based on the work in [24], presents a Colpitts oscillator topology with compact layout, suitable for low voltage, low phase noise applications in the W-band, and explores the impact of technology scaling on VCO performance. Also presented is a low voltage SiGe BiCMOS output buffer using 0.13 μm MOSFETs, suitable for W-band applications. The design and layout methodologies for the circuits are discussed in detail, and measurement results are presented which verify the accuracy of the design methodologies.

II. Overview of VCO and Output Buffer Topology

A. VCO Topology

The differential Colpitts topology [7] is a common choice for low phase noise, mm-wave VCOs [8]–[11], [13], [14], [20], [24]. Fig. 2 reproduces the schematic of our SiGe BiCMOS implementation of this topology. Not all of the passive components shown are strictly necessary to achieve oscillation. However, many of them, particularly the output network consisting of L_{PAD}, C_{PAD}, T_1, and C_4, arise out of layout and measurement considerations, which are critical at 100 GHz.

In an effort to minimize the supply voltage and phase noise, and to simplify layout, a single transistor topology is employed. A MiM capacitor (C_1) in parallel with C_{BE} improves supply induced pushing and reduces phase noise by shunting the base resistance, also illustrated in Fig. 2. Negative Miller capacitors (C_3) are placed at the base–collector junctions to cancel the effect of C_{BC}, thereby increasing the oscillation frequency. Finally, fully differential tuning with MOS varactors is employed for better supply noise rejection. Differential tuning also

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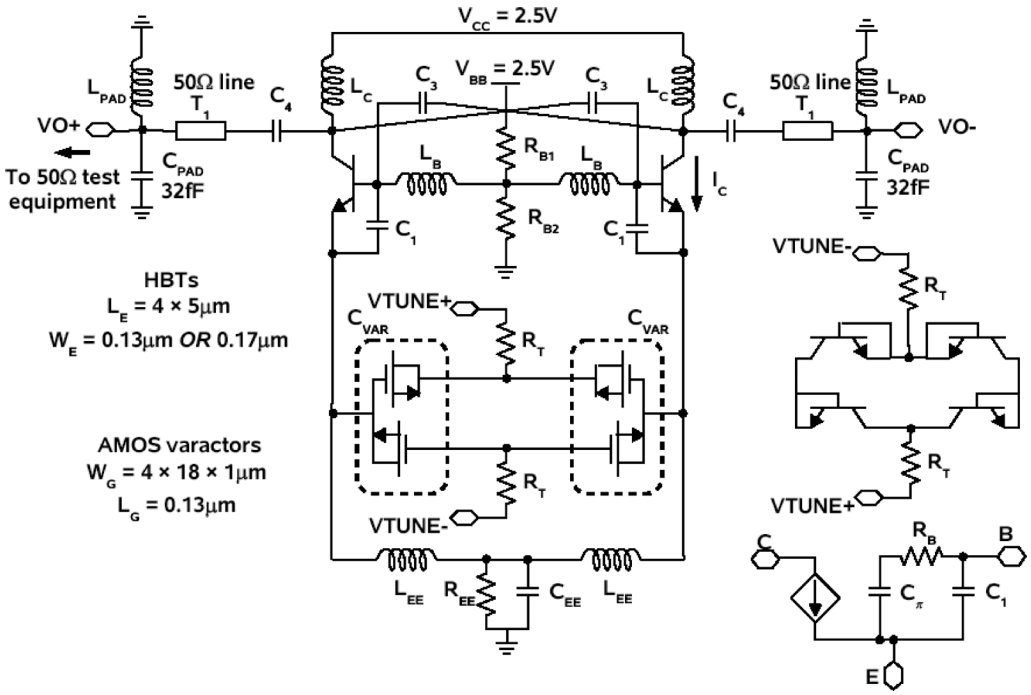


Fig. 2. Colpitts oscillator schematic.

reduces the modulation of the varactor capacitance $(C_{\rm VAR})$ by the tank voltage, which helps to suppress the maximum in phase noise seen at the center of the tuning range in some other VCOs [13]. The varactor layouts are optimized for high Q as in [13]. Where appropriate, spiral inductors are used in place of transmission lines to achieve a compact layout. When MOSFETs are not available to implement Accumulation Mode MOSFET (AMOS) varactors, HBT varactors, also shown in Fig. 2, can be employed instead.

B. Output Buffer Topology

To obtain larger output power, and to further isolate the VCO tank from external noise sources, an output buffer can be added to the VCO. Circuit topologies for a powerful output buffer include the HBT cascode [8], and the common source amplifier [21]. Another possible topology is the MOS-HBT BiCMOS cascode [14], shown in Fig. 3, which is more stable and can operate at lower supply voltage, than the HBT cascode. Additionally, the 130 nm MOSFET has greater linearity at high input voltage swings and a lower input time constant than the SiGe HBT [14]. The tail current source is eliminated, and the MOSFETs require less voltage headroom, allowing the supply voltage of the buffer to be reduced from 5.5 V for the HBT cascode amplifier in [8], to 2.5 V. To maximize the gain of the cascode stage and prevent instability, capacitors C_B must be placed as close as possible to the bases of Q_1 and Q_2 in Fig. 3 to minimize the parasitic inductance and resistance L_{PB} and R_{PB}.

All transistors in the output buffer (schematic shown in Fig. 3) are biased at peak $f_T/f_{\rm MAX}$ current density for maximum speed and linearity [17]. The transistor sizes and bias currents are chosen such that the buffer delivers $+10$ dBm of output power per side into a 50 Ω load. The cascode bias voltage (1.8–1.9 V) is chosen to set the drain–source voltage of $\rm M_1$ equal to 0.9 V when the supply voltage is 2.5 V. L_{G2} resonates with C_{GS1} at the design frequency, maximizing the buffer input impedance, which is otherwise very low because of the large transistor sizes needed to carry the bias current. T_2 is added to maximize the f_T of the cascode [19], whereas L_S improves linearity and stability, and also acts to increase the real part of the buffer input impedance.

III. Circuit Design Methodology

The VCOs presented here (all with the topology illustrated in Fig. 2) are designed for use in W-band transceivers for mm-wave imaging, automotive radar, and high data-rate communications. In these applications, aside from the well-known requirement for low phase noise, the VCO must drive the power amplifier, frequency divider (for the PLL), and down-convert mixer which together represent a significant capacitive load. To simultaneously meet the phase noise and loading requirements, the VCO will have high power consumption, and may need buffering stages capable of providing well over 0 dBm output power.

A. VCO Design: Obtaining High Tank Q

To achieve minimum phase noise in an LC-VCO, the quality factor (Q) of the resonant tank must be as high as possible. The dominant influence on the tank Q in W-band VCOs is the varactor Q which is 5–10 for 0.13 μm MOSFETs at 80 GHz [13]. Nonetheless, the series resistance of the tank inductor, as well as the base and emitter resistances of Q_1 and Q_2, also play important roles. Table I lists the values of the various parasitic resistances in our 100 GHz VCO implementation illustrated in Fig. 2, and clearly demonstrates the importance of the varactor series

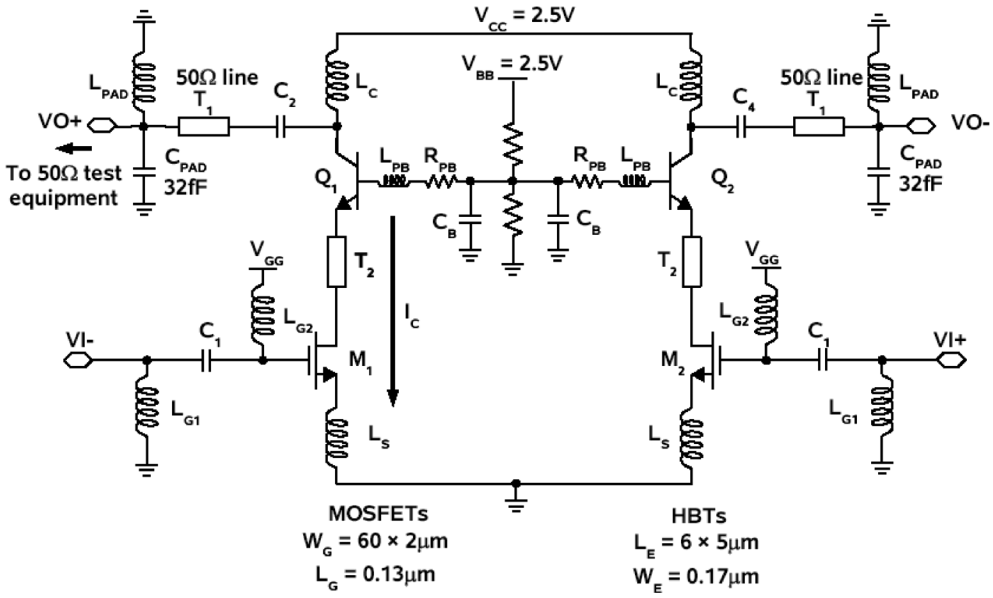


Fig. 3. MOS-HBT cascode output buffer for W-band VCOs.

TABLE I
PARASITIC RESISTANCES IN THE RESONANT TANK OF 0.13 μm AND 0.17 μm SiGe VCOs

Parameter	Value (for 4 × L_E = 5μm)
R_B' = 75Ωμm	3.75Ω
R_E' = 5Ωμm^2	1.5Ω when W_E = 0.17μm 1.9Ω when W_E = 0.13μm
Series resistance of L_B (L_B = 25pH, Q = 10)	< 1.5Ω
MOSFET varactor series resistance	12Ω if C_{VAR} = 25fF (Q=5) 6Ω if C_{VAR} = 25fF (Q=10) 3Ω if C_{VAR} = 50fF (Q=10)

resistance. Note that increasing the size of the varactor actually increases the tank Q, even if the varactor Q remains constant.

The varactor Q itself is determined by the gate, source-access, drain-access, and channel resistances of the MOSFETs used. The gate resistances for multi-finger MOSFETs with single-sided and double-sided contacts are given by

$$R_G = \frac{\frac{R_{\rm cont}}{N_{\rm cont}} + \frac{R_{G-SQ}}{L_{\rm phys}}\left[W_{\rm ext} + \frac{W_f}{3}\right]}{N_f} \quad (1)$$

$$R_G = \frac{\frac{R_{\rm cont}}{N_{\rm cont}} + \frac{R_{G-SQ}}{L_{\rm phys}}\left[W_{\rm ext} + \frac{W_f}{6}\right]}{2N_f} \quad (2)$$

respectively, where $R_{\rm cont}$ is the contact resistance, $N_{\rm cont}$ is the number of contacts per gate finger, R_{G-SQ} is the gate poly sheet resistance per square, $W_{\rm ext}$ is the gate extension beyond the active region, W_f is the finger width, N_f is the number of gate fingers connected in parallel, and $L_{\rm phys}$ is the physical channel length [19]. Comparing (1) and (2), clearly double-sided gate contacts should be used. Furthermore, W_f should be minimized (1 μm or less in sub-130-μm CMOS), and a large number of fingers (N_f) used in parallel to obtain the desired capacitance [19], [20].

The overall channel resistance (R_{ch}) is given by

$$R_{ch} = \frac{R_{CH-SQ}}{12}\frac{L_{\rm phys}}{W_f N_f} \quad (3)$$

where R_{CH-SQ} is the sheet resistance of the channel material. The channel resistance is minimized using fingers with minimum gate length ($L_{\rm phys}$). Because the total gate width ($W_f N_f$) influences the channel resistance, and not the finger width (W_f) independently, choosing small W_f to minimize R_G does not degrade R_{ch} if the total gate width is held constant.

The source and drain access resistances can be up to 200 $\Omega\mu$m in 130 nm CMOS. Once again, this resistance is minimized using many parallel gate fingers. To minimize any layout parasitic resistances, as many contacts and vias as possible should be stacked on the drain and source of the varactor, and the varactor nodes should be routed in as many metals as possible. In VCOs using HBT varactors, the HBT varactor layout should have multiple base stripes to minimize the base resistance. Note that the layouts exhibit considerable parasitic capacitance which further improves the quality factor, albeit at the expense of tuning range.

In addition to maximizing the varactor Q, close attention must be paid to the inductance and quality factor of the tank inductor. To obtain low phase noise, the tank inductance must be as small as possible without allowing the quality factor of the tank inductance to degrade the tank Q. Choosing the smallest possible L_B allows the largest possible values for C_1 and $C_{\rm VAR}$ for a given $f_{\rm osc}$, which can be seen by studying the formulae for the frequency of oscillation

$$f_{\rm osc} = \frac{1}{2\pi\sqrt{L_B C_{\rm EFF}}} \quad \text{where}$$
$$C_{\rm EFF} = C_{BC} + \frac{C_{\rm VAR}(C_1 + C_{BE})}{C_{\rm VAR} + C_1 + C_{BE}} \quad (4)$$

and phase noise

$$S_{\Delta\rm out} = 2\frac{\langle |I_n|^2\rangle}{|V_{\rm tank}|^2}\frac{1}{(C_1 + C_\pi)^2\left(\frac{C_1 + C_\pi}{C_{\rm var}} + 1\right)}\frac{1}{\Delta\omega^2} \quad (5)$$

for a Colpitts oscillator [18]. In (5) $V_{\rm tank}$ is the peak-to-peak tank swing in volts, I_n is the noise current representing all noise sources of the amplifying HBT, and $C_{\rm VAR}$ includes both the varactor capacitance and parasitic capacitance at the emitters of Q_1 or Q_2. Because C_1 is in the denominator of (5), having a large C_1 improves phase noise, and as seen in Table I, larger $C_{\rm VAR}$ also improves the tank Q. In a given technology, the minimum value for L_B with reasonable Q can be found using ASITIC (the complete design methodology for all inductive interconnect is described in [23]). In W-band VCOs, an inductance of about 25 pH, and corresponding quality factor of 20, is acceptable to ensure that the varactor, and not the tank inductance, dominates the overall resonant tank quality factor.

B. VCO Design: Tank Swing, Temperature Sensitivity, and Supply Pushing

Obtaining high tank swing, and minimizing temperature and supply induced changes in center frequency are related because they can all be achieved using large transistors (Q_1 and Q_2 in Fig. 2). High tank swing is desirable because it minimizes phase noise, which can be understood from (5). Critical in obtaining high tank swing is having high bias current, and if necessary, biasing at the peak $f_T/f_{\rm MAX}$ current density of Q_1 and Q_2. Care must be taken not to exceed the breakdown voltage of Q_1 and Q_2.

When Q_1 and Q_2 are large and C_3 is added to cancel C_{BC}, $f_{\rm osc}$ reduces to

$$f_{\rm osc} = \frac{1}{2\pi\sqrt{L_B C_{\rm VAR}}}. \tag{6}$$

The required size of C_3 is found by extracting the value of C_{BC} from S-parameter simulations, as outlined in [25]. Using this extraction method, C'_{BC} was found to be approximately 15 fF/μm^2, yielding a total C_{BC} of 40 fF for the device used. To avoid generating negative capacitance, 30 fF was chosen for C_3, which was implemented using a minimum size MiM capacitor. The use of large transistors, the addition of C_1 to C_{BE}, and the addition of C_3 to cancel C_{BC} reduce supply pushing simply through minimizing the dependence of $f_{\rm osc}$ on transistor parameters. Differential tuning also helps to reduce supply pushing.

Even without C_1, large HBTs (and therefore large C_{BE}) minimize the temperature and supply dependence. For example, consider a VCO where $C_1 = 0$. In this case, the effective tank capacitance is approximately given by

$$C_{\rm EFF} = C_{BC} + \frac{C_{\rm VAR}C_{BE}}{C_{\rm VAR} + C_{BE}}. \tag{7}$$

Taking the derivative of (7) with respect to temperature yields (8). Under the condition that C_{BE} is much greater than $C_{\rm VAR}$, (8) simplifies to (9), where the temperature dependence on C_{BE} is negligible. [See (8)–(9) shown at the bottom of the page.]

The variation of C_{BC} over temperature is approximately given by

$$\frac{\partial C_{BC}}{\partial T} \approx \frac{\partial}{\partial T}\sqrt{\frac{q\varepsilon_{Si}}{2\left[\frac{1}{N_A}+\frac{1}{N_D}\right]V_A}} \tag{10}$$

where N_a is the density of acceptors in the base, N_d is the density of donors in the collector, and V_A is the reverse bias voltage of the base–collector junction. The temperature range 0 °C to 100 °C is high enough that all of the donors and acceptors are ionized, but low enough that the intrinsic carrier concentrations in the base and collector are less than N_a and N_d. Therefore, in this temperature range variations in C_{BC} will remain low [27]. In this situation, the temperature dependence of $f_{\rm osc}$ is dominated by temperature variations in $C_{\rm VAR}$, which are caused primarily by changes in the bias voltage at the emitters of Q_1 and Q_2. Differential tuning and intrinsic series feedback minimize these variations.

C. Series Feedback

Series feedback plays an important role in reducing temperature and supply voltage variation in $f_{\rm osc}$. The emitter resistance in the 0.13 μm HBTs used here is 5 $\Omega\mu$m^2, which reduces the transconductance of the HBT biased at peak $f_T/f_{\rm MAX}$ current density (shown to be 15 mA/μm^2 in Section IV) by a factor of 4. Equation (11) demonstrates the calculation for an HBT with $L_E = 1$ μm and $W_E = 0.13$ μm. In common mode, R_{EE} also generates considerable series feedback.

$$g_{m\rm eff} = \frac{g_m}{1+g_m R_E} = \frac{g_m}{1+\frac{15\ \text{mA}/\mu\text{m}^2\times 5\ \Omega\mu\text{m}^2}{25\ mV}} = \frac{g_m}{4}. \tag{11}$$

D. Negative Resistance and Current Density

The negative resistance provided by Q_1 is approximated by

$$R_{\rm NEG} = R_E + R_B + \frac{\omega_{\rm osc}L_B}{Q_{LB}} + \frac{1}{\omega_{\rm osc}Q_{\rm CVAR}C_{\rm VAR}} - \frac{g_m/k}{\omega_{\rm osc}^2(C_\pi/k + C_1)C_{\rm VAR}} \tag{12}$$

where R_B is the base resistance, R_E is the emitter resistance, Q_{LB} is the quality factor of the base inductance, $Q_{\rm CVAR}$ is the quality factor of the varactor, g_m is the transconductance of the HBT, and k is the intrinsic feedback factor caused by the emitter

$$\frac{\partial C_{\rm EFF}}{\partial T} = \frac{\partial C_{BC}}{\partial T} + \frac{(C_{BE}+C_{\rm VAR})\left(\frac{\partial C_{BE}}{\partial T}C_{\rm VAR} + \frac{\partial C_{\rm VAR}}{\partial T}C_{BE}\right) - (C_{BE}C_{\rm VAR})\left(\frac{\partial C_{BE}}{\partial T} + \frac{\partial C_{\rm VAR}}{\partial T}\right)}{(C_{BE}+C_{\rm VAR})^2} \tag{8}$$

$$\frac{\partial C_{\rm EFF}}{\partial T} = \frac{\partial C_{BC}}{\partial T} + \frac{\partial C_{\rm VAR}}{\partial T} + \frac{C_{\rm VAR}^2}{C_{BE}^2}\frac{\partial C_{BE}}{\partial T} \tag{9}$$

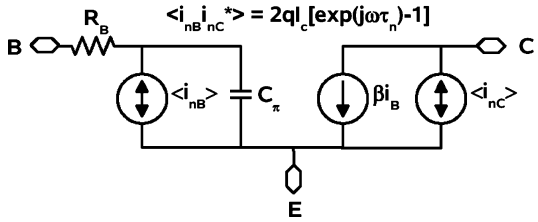


Fig. 4. Correlation of base and collector shot noise currents where τ_n is the noise transit time [26].

resistance. $R_{\rm NEG}$ must be large enough to overcome the transistor series resistances and other tank losses. Ultimately, negative resistance will limit the size of C_1 and $C_{\rm VAR}$ which are used to minimize phase noise. Alternatively, (12) can be recast as

$$R_{\rm NEG} = (\text{Tank loss resistance}) - \frac{I_C/kV_T}{\omega_{\rm osc}^2(\tau_F I_C/kV_T + C_1)C_{\rm VAR}} \tag{13}$$

where τ_F is the transit time through the base and collector regions of the HBT. From (13), biasing at peak f_T current density (equivalent to minimum τ_F and high I_C) maximizes $R_{\rm NEG}$, and therefore allows the largest values of C_1 and $C_{\rm VAR}$, given $\omega_{\rm osc}$. To minimize phase noise in 40 GHz VCOs, in [13] and [14] it was shown that Q_1 should be biased at the $\rm NF_{MIN}$ current density, which minimizes I_n. In the W-band, the correlation between base and collector noise currents (illustrated in Fig. 4) pushes the optimum $\rm NF_{MIN}$ current density closer to the peak $f_{\rm MAX}$ current density [15]. Furthermore, biasing at peak $f_{\rm MAX}$ current density increases the tank swing, and enables larger values of C_1 to meet the oscillation condition in (7). Because $|V_{\rm tank}|$ and C_1 both appear in the denominator of (5), the optimum phase noise bias current density of W-band VCOs shifts toward peak f_T current density.

E. VCO Output Network and Biasing Networks

The output network, consisting of L_C, C_4, T_1, $L_{\rm PAD}$, and $C_{\rm PAD}$, is designed to provide maximum output power, and isolate the tank from the bias supply. The size of C_4 is designed to provide effective DC blocking while having high Q at the oscillation frequency. L_C is chosen to resonate C_{CS} and the bottom plate parasitic capacitance of C_4. Finally, $L_{\rm PAD}$ is chosen to resonate $C_{\rm PAD}$, and T_1 is 50 Ω microstrip line, maintaining a 50 Ω environment from the test equipment up to the VCO output.

The biasing network consists of R_{B1}, R_{B2}, R_{EE}, L_{EE}, and C_{EE}, and should be designed to isolate the tank, minimize the noise contribution of R_{EE}, and allow the full tuning range of the VCO to be exercised without requiring negative voltages at $V_{\rm TUNE^+}$ or $V_{\rm TUNE^-}$. To isolate the tank, L_{EE} should be large. The noise contribution of R_{EE} can be reduced by selecting C_{EE} in accordance with

$$\frac{1}{2\pi R_{EE}C_{EE}} < \frac{f_{\rm osc}}{5} \tag{14}$$

which attenuates the noise of R_{EE} by 20 dB at $2f_{\rm osc}$. The full tuning range can be exercised by selecting R_{EE} in accordance with

$$V_{GS\rm MAX} = 2I_C R_{EE} \tag{15}$$

TABLE II
VCO DESIGN PARAMETERS

f_{osc}	77GHz	87GHz	100GHz
L_B	35pH	28pH	23pH
L_C	55pH	35pH	35pH
L_{EE}	200pH	200pH	200pH
C_{VAR}	2×3μm×0.13μm HBT varactor (double bases)	2×10×1μm×130nm NMOS varactor	2×9×1μm×130nm NMOS varactor *OR* 1×6μm×0.13μm HBT varactor (double base)
added C_1	75fF	55fF	55fF
C_3	30fF	27fF	27fF
L_{PAD}	80pH	80pH	80pH
I_C	24mA	24mA	24mA
A_E	4×5×0.13μm	4×5×0.17μm or 4×5×0.13μm	4×5×0.17μm or 4×5×0.13μm
R_{EE}	40Ω	40Ω	40Ω
C_{EE}	250fF	250fF	250fF

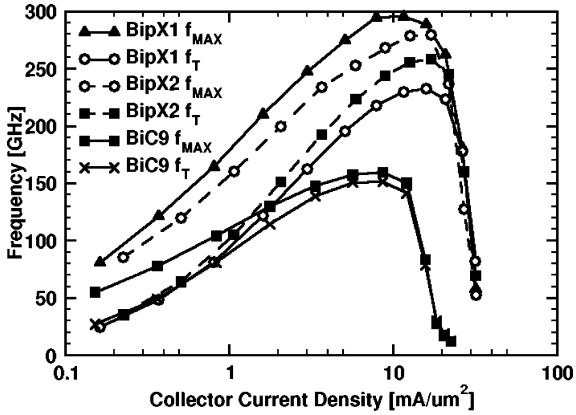


Fig. 5. High frequency performance of two generations of SiGe technology.

where I_C is the collector current of Q_1. Finally, R_{B1} and R_{B2} should be small enough to provide the base current for Q_1 and Q_2 without causing large voltage fluctuations at their center node.

F. Design Parameter Summary

Table II summarizes the design parameters for 77 GHz, 87 GHz, and 100 GHz VCOs designed for low phase noise and biased at peak f_T current density. The different emitter sizes will be discussed in Section IV.

IV. FABRICATION AND LAYOUT

VCOs with center frequencies of 77, 87, and 100 GHz, with the architecture shown in Fig. 2, were designed and fabricated in a SiGe BiCMOS process with $f_T/f_{\rm MAX}$ of 150/160 GHz (referred to as "BiC9" [1]), and two SiGe HBT process splits with $f_T/f_{\rm MAX}$ of 230/300 GHz and 260/270 GHz, referred to as BipX1 and BipX2, respectively [2]. The measured $f_T/f_{\rm MAX}$ of the three HBTs are illustrated in Fig. 5 and summarized in Table III. The two BipX HBTs have the same $f_T f_{\rm MAX}$ product. The three processes are identical except for the HBTs (also MOSFETs are not available in BipX). This allows investigation of: 1) the impact of SiGe HBT scaling on mm-wave VCO

TABLE III
SiGe TECHNOLOGY f_T AND f_{MAX}

Technology Name	Emitter width (μm)	f_T (GHz)	f_{MAX} (GHz)
BiC9	0.17	150	160
	0.13	170	210
BipX1	0.13	230	300
BipX2	0.13	260	270

TABLE IV
SUMMARY OF FABRICATED CIRCUITS

Designed Center Frequency	**Circuits Fabricated**
100GHz	VCO in BipX1, with HBT varactors VCO in BipX2, with HBT varactors VCO in BiC9, with HBT varactors VCO in BiC9, with MOS varactors
87GHz	VCO in BiC9, with MOS varactors MOS-HBT cascode output buffer, in BiC9 VCO with MOS-HBT cascode output buffer, in BiC9
77GHz	VCO in BiC9, but with 0.13μm emitter width

performance; 2) the relative importance of f_T and f_{MAX} on VCO performance; and 3) the VCO as a process monitor for mm-wave HBT noise performance. The HBTs in all three processes are directly substitutable in the layout view, and therefore the VCO layout need not be modified when porting designs between the technologies. Consequently, measurement results from all 100 GHz VCOs can be compared directly.

Because MOSFETs are not yet available in BipX1 and BipX2, two versions of the 100 GHz VCO were designed, one with differential MOS varactor tuning as illustrated in Fig. 2, and another with single-ended HBT varactors. The 87 GHz VCO with output buffer was fabricated in the BiC9 process only because the output buffer requires MOSFETs. Separate structures of the 87 GHz VCO and the buffer were also fabricated to allow determination of the buffer and VCO performance individually. The 77 GHz VCO, with the differential HBT varactor tuning illustrated in Fig. 2(b), was fabricated in BiC9 only, but with 0.13 μm emitter width for Q_1 and Q_2, which lends improvements in f_T and f_{MAX}. For clarity, Table IV lists all of the circuits that were fabricated.

A microphotograph of the 100 GHz VCO layout is shown in Fig. 6, and the 87 GHz VCO with buffer is illustrated in Fig. 7. All VCOs occupy 300 μm $\times$ 400 μm each, including all pads (not shown), while the VCO core is only 100 μm $\times$ 100 μm. The VCO with output buffer occupies 550 μm $\times$ 500 μm including all pads. The die areas are smaller than other W-band SiGe VCOs [8], [9], [11] because inductors are used in place of transmission lines.

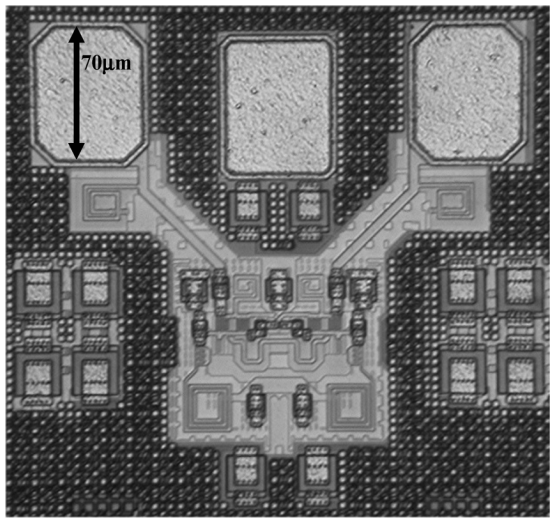


Fig. 6. 100 GHz VCO microphotograph.

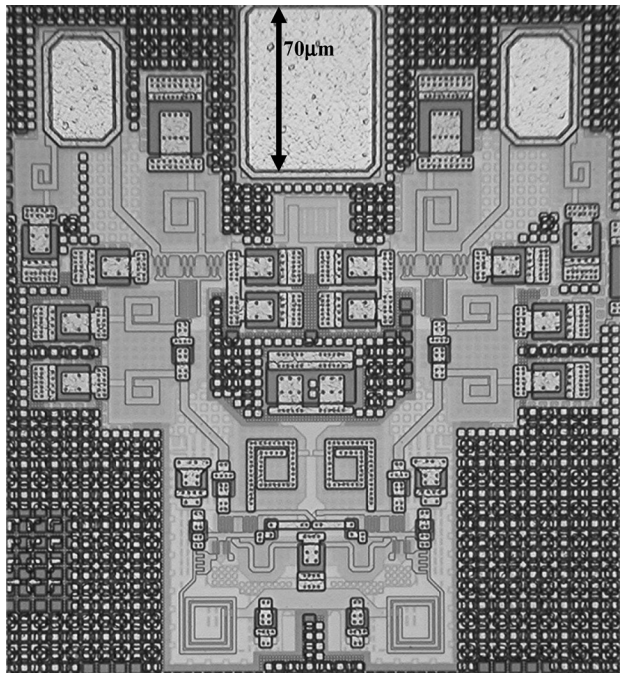


Fig. 7. 87 GHz VCO with output buffer.

V. EXPERIMENTAL RESULTS

A. VCO Performance Summary

All VCOs consume 135 mW from a 2.5 V supply. Tables V and VI summarize the measurement results (5 dB $\pm$ 1 dB measured probe and cable losses de-embedded) for the 100 GHz and 77–87 GHz VCOs, respectively. The differential output powers listed in Tables V and VI were measured using the Agilent E4419B power meter and W8486A waveguide power sensor. Note that the measured center frequencies of the VCOs designed for 100 GHz vary from 96 GHz to 106 GHz, depending on the technology. Post-layout simulations performed using HiCUM models show similar variation in the oscillation frequency.

B. Technology Comparison

The change in center frequency between the 100 GHz VCOs in Table V is $\pm$5%, whereas the improvements in phase noise and output power between the BiC9 MOS varactor VCO and the BipX1 HBT varactor VCO are 2.8 dB (or 90%), and 2.0 dB (or 58%), respectively. If the BiC9 VCO with HBT varactor is used as a basis for the same comparison, the improvements are even greater. This clearly demonstrates that phase noise and

TABLE V
SUMMARY OF 100 GHz VCO PERFORMANCE

	BiC9 MOS var.	BiC9 HBT var.	BipX1 HBT var.	BipX2 HBT var.
Process f_T/f_{MAX} (GHz)	150/160	150/160	230/300	260/270
Differential Output Power (dBm)	+0.5 sim. +5.5	-0.5 sim. -1.15	+2.7 sim. +6.5	+2.5
SSB Phase Noise @ 1MHz offset (dBc/Hz)	-96.0	-80	-96.6	-98.8
Center Frequency (GHz)	96 sim. 96	100 sim. 100	106 sim. 108	104
Tuning Range (GHz) 25ºC	5	3.8	2.3	2.2
KVCO (GHz/V),25ºC	2.08	2.11	1.15	1.1
Pushing: $\Delta f_{osc}/\Delta V_{DD}$, (GHz/V)	0.27	Not measured	3.0	Not measured

TABLE VI
SUMMARY OF 87 GHz AND 77 GHz VCO PERFORMANCE

	BiC9, MOS var. w/o buffer	BiC9 MOS var. w buffer	BiC9 w $W_E = 0.13\mu m$ HBT var. w/o buffer
Process f_T/f_{MAX} (GHz)	150/160	150/160	170/210
Differential Output Power (dBm)	+0.5 sim. +2	+7 (2.5V) +10.5 (3.3V) sim. +10	+2.5 sim. +3
SSB Phase Noise @ 1MHz offset (dBc/Hz)	-98.3	not measured	-99.1
Center Frequency (GHz)	87 sim. 87	87 sim.87	77 sim. 79
Tuning Range (GHz) 25ºC	3.7	3.7	1
KVCO (GHz/V) 25ºC	1.54	1.54	0.42
Pushing: $\Delta f_{osc}/\Delta V_{DD}$, (GHz/V)	0.065	0.065	Not measured

output power are improved by migrating to a new technology node, even without design changes. Conversely, oscillation frequency remains relatively constant, despite the 50%–70% increase in f_T and 69%–88% increase in f_{MAX}. This is not surprising since the oscillation frequency depends primarily on the accurate modeling of the passive components (in particular C_{VAR} and L_B, but also all other interconnect). So long as the back-end-of-line (BEOL) remains unchanged, mm-wave circuits can be ported directly between successive generations of SiGe technology with improvements in phase noise and output power, obtaining benefits but mitigating costs of moving to the next node.

Another observation from Table V is the direct correspondence between process f_{MAX}, center frequency, and output power. However, the relationship between f_{MAX} and phase noise is not so straightforward, as the BipX2 VCO actually has lower phase noise than the BipX1 VCO. Nonetheless, the improvement in phase noise and output power, and increase in center frequency of the BipX 100 GHz VCOs over the BiC9 ones indicates that 1) migrating to a new technology without design changes will improve VCO performance and 2) Colpitts VCOs can be used to monitor the mm-wave performance of HBTs. Any confounding influence of the varactors could be removed by using MiM capacitors in their place.

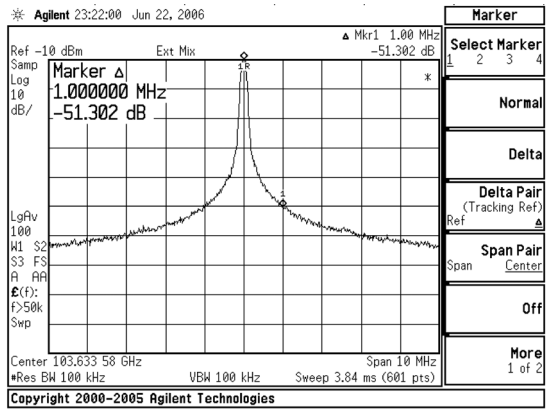
Comparing the BiC9 VCOs with MOS and HBT varactors (columns 2 and 3 of Table V), the MOS varactors probably offer a higher quality factor than the HBT varactors. The BipX VCOs would likely perform even better if MOS varactors were available at the time of manufacture.

C. Phase Noise

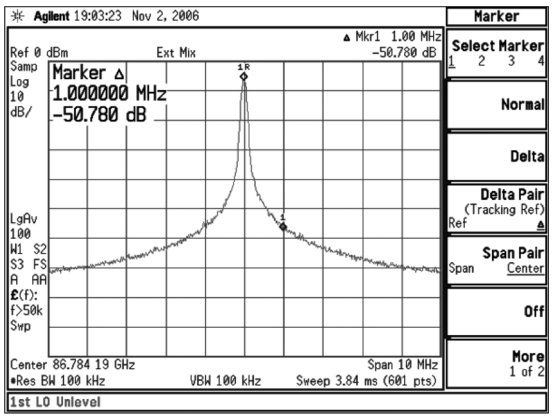
Fig. 8 illustrates averaged spectral plots of phase noise at 1 MHz offset for the 104 GHz BipX2 VCO (a), and the 87 GHz BiC9 VCO (b) to verify the phase noise results given in Tables V and VI, respectively. All phase noise measurements were made using the Agilent E4448A Power Spectrum Analyzer and the Agilent 11970W waveguide harmonic mixer, and are averaged over 100 sweeps to ensure that these record results for SiGe VCOs over 80 GHz have not occurred by chance. Because video averaging was used, the phase noise values shown in the plots are about 2.5 dB optimistic; the worst case corrected values are listed in Table V and Table VI. The phase noise measurements were performed using a low noise power supply capable of providing 62 mA, and a voltage regulator powered using standard 9 V batteries was employed to adjust the tuning voltage inputs. The phase noise of the BiC9 VCO with output buffer cannot be measured because the low noise power supply cannot provide the current necessary to bias both the VCO and output buffer.

D. Performance Over Temperature

Shown in Fig. 9 are measured tuning characteristics of the VCOs with HBT varactors over temperature. The BipX1 VCO displays 2 GHz of overlapping tuning range from 27 °C to 100 °C; the center frequency changes by only 1% over the



(a)



(b)

Fig. 8. Averaged spectral plots of phase noise in (a) the 104 GHz VCO with HBT varactor (BipX2), and (b) the 87 GHz VCO with MOS varactor (BiC9).

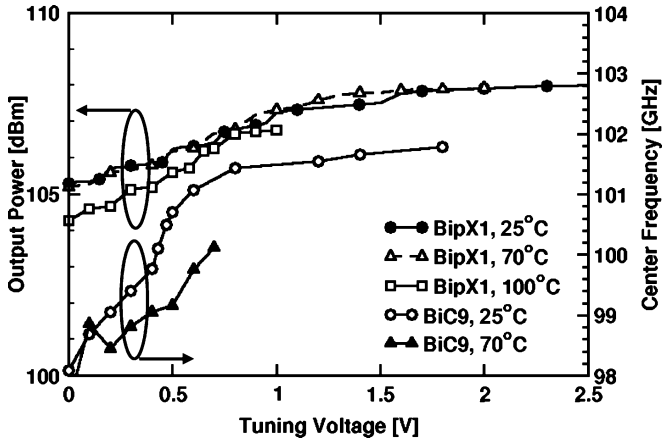


Fig. 9. Tuning characteristics across temperature for HBT varactor VCOs.

same temperature range. These measurements verify the design methodology used to achieve insensitivity to temperature.

Fig. 10 compiles the measured output power across the tuning range at 25 °C, 70 °C, and 125 °C. The BiC9 VCO with MOS varactor operates up to 70 °C and the BiC9 VCO with HBT varactor operates up to 50 °C. In contrast, the BipX1 oscillator functions up to at least 125 °C, although the center frequency at 125 °C has shifted substantially compared to the results at 100 °C in Fig. 9.

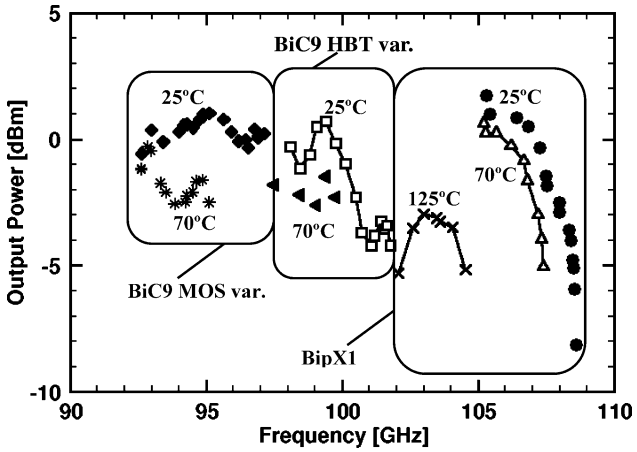
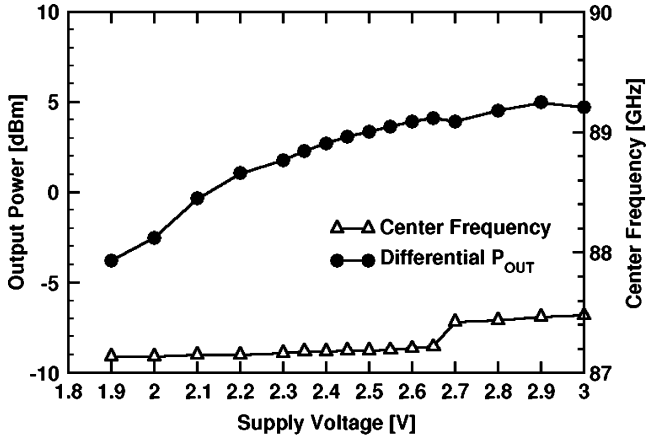
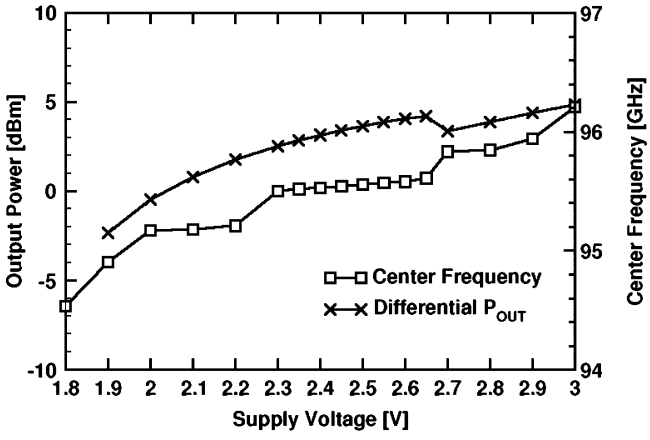


Fig. 10. Output power versus $f_{\rm osc}$ at 25 °C, 70 °C, and 125 °C.



(a)



(b)

Fig. 11. Variations in output power and center frequency with supply voltage in 87 GHz and 96 GHz VCOs with differential tuning.

E. Supply Induced Pushing $(\Delta\omega/\Delta V_{DD})$

Supply induced changes in oscillation frequency are of primary concern in low phase noise applications. Shown in Fig. 11(a) and (b) are the variations in output power and center frequency for 87 GHz and 96 GHz VCOs with differential tuning. The VCO center frequency is extremely insensitive to small fluctuations in supply voltage around the nominal

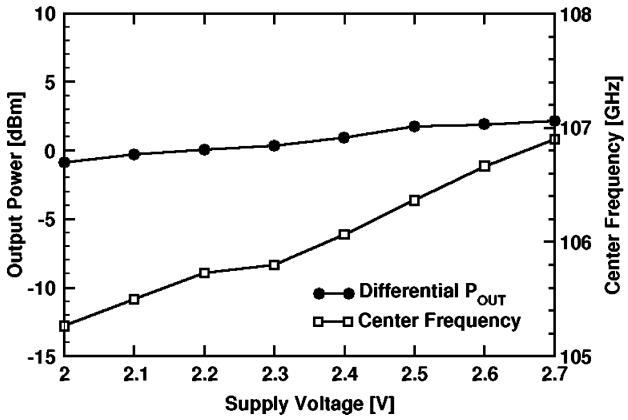


Fig. 12. Variations in output power and center frequency with supply voltage in a 105 GHz VCO with single-ended tuning.

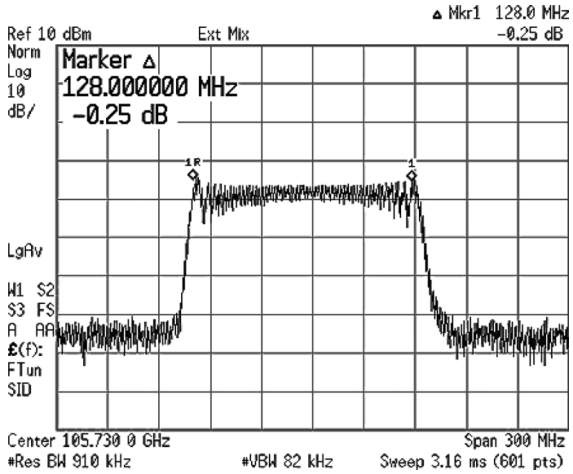


Fig. 13. Frequency modulation of 106 GHz BipX1 VCO.

value of 2.5 V. In contrast, Fig. 12 shows the variations in supply voltage and output power of the 105 GHz VCO with single-ended tuning. Clearly, differential tuning decreases supply induced pushing.

F. Direct Modulation

Frequency modulation of the VCO output can be performed by applying a triangular wave to the tuning input—a modulation technique commonly employed in FMCW radar systems. The resulting spectrum, obtained at 100 °C using the BipX1 HBT varactor VCO, is shown in Fig. 13.

G. Passive Component Performance

The lumped tank inductors (L_B) of the 100 GHz, 87 GHz, and 77 GHz VCOs were designed to be 23 pH, 28 pH, and 35 pH, respectively, as described in Section III. To demonstrate the accuracy of the inductor designs, in Fig. 14 we show simulated and measured inductance and quality factor for the base inductance used in the 87 GHz VCO.

H. Output Buffer Performance

The MOS-HBT cascode output buffer gain is illustrated in Fig. 15(a). At 86 GHz, the buffer achieves peak gains of 7 dB at

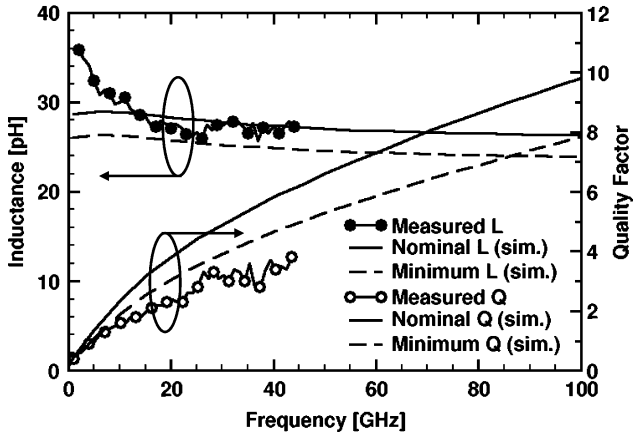
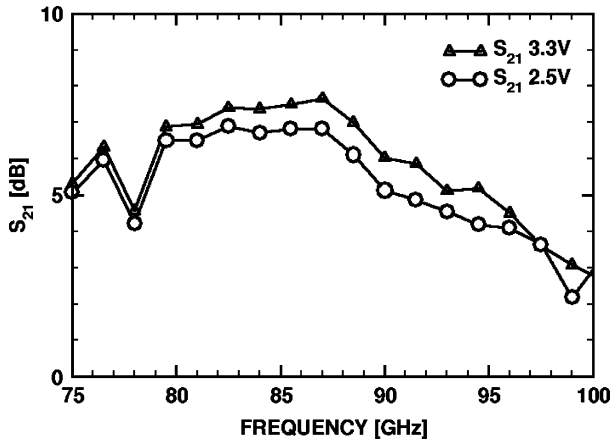
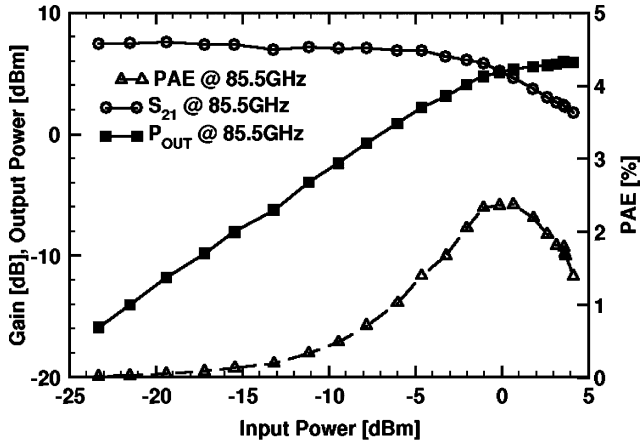


Fig. 14. Measurements of the base inductance used in the 87 GHz VCO.



(a)



(b)

Fig. 15. (a) MOS-HBT cascode output buffer gain at 2.5 V and 3.3 V and (b) large signal performance.

2.5 V supply, and 7.5 dB at 3.3 V supply, and a −3 dB bandwidth of 15 GHz. The large signal performance of the buffer is shown in Fig. 15(b). At 85.5 GHz and 2.5 V supply, the buffer achieves an output 1 dB compression point of +5 dBm, saturated output power greater than 6 dBm, and power-added efficiency (PAE) of 2.3%.

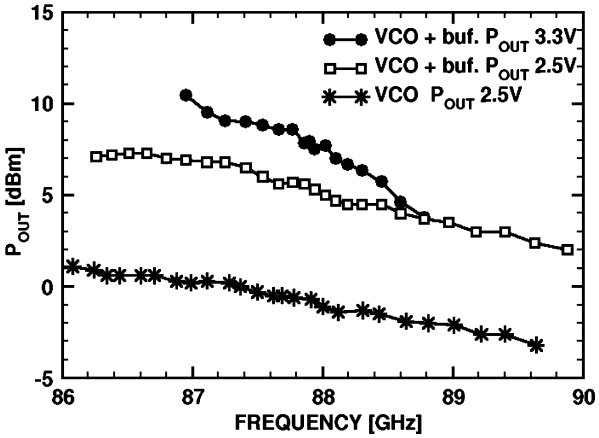


Fig. 16. 87 GHz BiC9 VCO and output buffer measurements (differential output power).

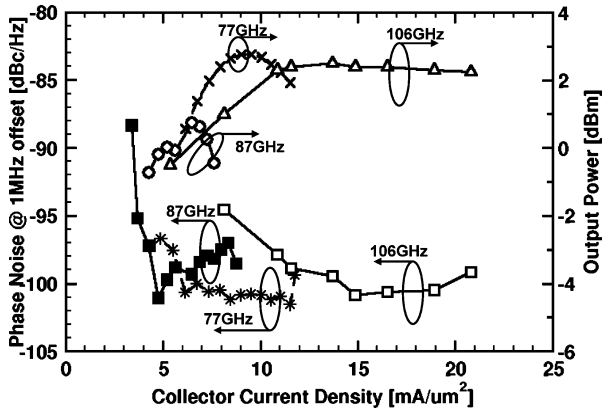


Fig. 18. Phase noise and output power as functions of bias current density in 87 GHz (BiC9) and 106 GHz (BipX1) VCOs.

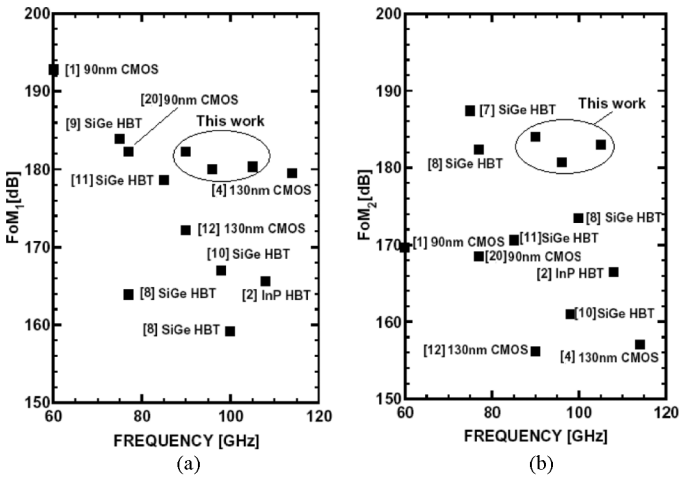


Fig. 17. VCO figures of merit (a) excluding output power, and (b) including output power.

As illustrated in Fig. 16, when the output buffer is used with the 87 GHz VCO, +7 dBm differential output power is obtained at 87 GHz using a 2.5 V supply. If the output buffer supply voltage is increased to 3.3 V, up to +10.5 dBm differential output power is obtained, also illustrated in Fig. 16. Though higher output power at 87 GHz has been obtained in SiGe HBT technologies with $f_T/f_{\rm MAX}$ greater than 200 GHz [8], [21], this output buffer represents the first time that 130 nm MOSFETs are used above 80 GHz. The MOS-HBT cascode will become even more competitive when the next generation SiGe BiCMOS processes are developed [22].

I. Figures of Merit

Shown in Fig. 17(a) are the ITRS VCO FoMs for numerous state-of-the-art VCOs, alongside the FoMs of the VCOs that constitute this work. The VCO FoM used by ITRS is given by

$$\mathrm{FoM}_1 = \left(\frac{f_{\rm osc}}{\Delta f}\right)^2 \left(\frac{1}{L[\Delta f]P_{\rm DC}}\right). \tag{16}$$

The fact that the ITRS FoM excludes output power explains why CMOS VCOs rate very highly using this figure of merit. However, in many applications, a mm-wave VCO with low output power would require amplification before becoming useful. This increases the $P_{\rm DC}$ term in the denominator of (16), effectively decreasing the figure of merit. An improved design strategy is to dissipate greater power in the VCO core, which reduces the overall circuit complexity by eliminating amplifier stages. Furthermore, increased core power dissipation ultimately improves phase noise, whereas amplifying stages do nothing to improve phase noise. As shown in Fig. 17(b), when the same state-of-the-art VCOs are compared on the basis of the FoM in

$$\mathrm{FoM}_2 = \left(\frac{f_{\rm osc}}{\Delta f}\right)^2 \left(\frac{P_{out}}{L[\Delta f]P_{\rm DC}}\right), \tag{17}$$

SiGe VCOs consistently rate higher.

J. Biasing for Minimum Phase Noise

To experimentally investigate the optimum biasing strategy for minimum phase noise in W-band VCOs, the bias currents in the 77 GHz BiC9 VCO with 0.13 μm emitter width, 87 GHz BiC9 VCO with 0.17 μm emitter width, and 106 GHz BipX1 VCO with 0.13 μm emitter width were varied, and the phase noise at 1 MHz offset was recorded at each current density. The results, illustrated in Fig. 18, show the collector currents (I_C), and collector current densities (J_C), at which each VCO reaches minimum phase noise. The 77 GHz and 100 GHz VCOs reach minimum phase noise at the same bias that corresponds to maximum output power. The 87 GHz VCO reaches minimum phase noise at a current density slightly lower than that corresponding to maximum output power.

Next, the S-parameters of the BiC9, BipX1, and BipX2 HBTs were measured, and their f_T, $f_{\rm MAX}$, and $\mathrm{NF}_{\rm min}$ were extracted using de-embedded Y-parameters up to 65 GHz. The $\mathrm{NF}_{\rm min}$ extraction was performed using the techniques in [15], with a noise transit time (τ_n) of 0.4 ps and 0.3 ps for BiC9 and BipX, respectively. The results, shown in Fig. 19, indicate that the peak $f_T/f_{\rm MAX}$ and minimum $\mathrm{NF}_{\rm min}$ current densities of the BipX1 and BipX2 HBTs are approximately double those of the BiC9 HBTs, and that the peak $f_T/f_{\rm MAX}$ current density of the BiC9 HBTs is independent of emitter width. The peak $f_T/f_{\rm MAX}$ current densities of the BiC9 and BipX1/BipX2 HBTs are, respectively, $J_C = 7.5\,\mathrm{mA}/\mu\mathrm{m}^2$, and $J_C = 15\,\mathrm{mA}/\mu\mathrm{m}^2$. The $\mathrm{NF}_{\rm min}$

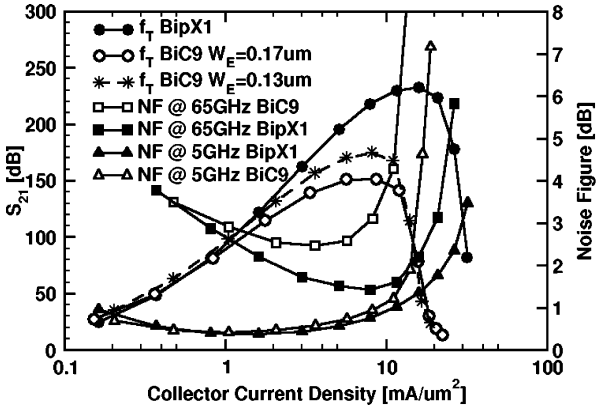


Fig. 19. Peak f_T and $\mathrm{NF}_{\min}$ as functions of bias current density in SiGe HBTs.

TABLE VII
PERFORMANCE OF BiC9 MOS VAR. VCOS AT ROOM TEMPERATURE

Wafer		1	2	3	4
Center frequency (GHz)	Mean	94.7	94.9	94.9	95.0
	Standard deviation	0.142	0.28	0.1	0.2
Tuning range (GHz)	Mean	4.6	4.6	4.6	4.6
	Standard deviation	0.19	0.4	0.2	0.2
Output power (dBm)	Mean	0.2	0.7	0.6	0.8
	Standard deviation	-20	-11	-17	-17
DC power (mW)	Mean	133.8	133.2	137.3	132.6
	Standard deviation	2.0	2.7	2.9	2.1

current densities at 65 GHz are $J_C = 3.75\ \mathrm{mA}/\mu\mathrm{m}^2$ and $J_C = 7.5\ \mathrm{mA}/\mu\mathrm{m}^2$, respectively. Note that $\mathrm{NF}_{\min}$ @ 65 GHz in BipX is only 1.7 dB, the lowest reported for a SiGe HBT at this frequency. As indicated by the minimum values of the 5 GHz and 65 GHz noise figure data, as expected the $\mathrm{NF}_{\min}$ current density varies with frequency.

Comparing the peak f_T/f_{MAX} current densities in Fig. 19 to the minimum phase noise current densities in Fig. 18, the minimum phase noise is obtained near peak f_T/f_{MAX} current density in all three VCOs. Furthermore, -100 dBc/Hz phase noise is consistently attainable across the W-band.

K. Process Monitoring

To gauge the impact of process variations on VCO performance, the mm-wave and DC characteristics of both 100 GHz BiC9 VCOs were collected from 60 dice on four different wafers. Tables VII and VIII summarize the results for the MOS varactor and HBT varactor VCOs, respectively. Of the 120 VCOs tested, four had significantly below average performance, and another two VCOs failed to oscillate. The six outlier VCOs are not included in the averages given. The standard deviation of the output power is obtained by first converting the output powers from dBm to mW, then obtaining the standard deviation, and finally converting back to dBm.

To further characterize the VCOs over process variations, output power is plotted versus oscillation frequency in Fig. 20 for one VCO on each of the four wafers, alongside simulation results. A 1.5 dB variation in output power between BiCMOS9 VCOs on different wafers is illustrated. Note however that the center frequency remains constant over the wafers.

TABLE VIII
PERFORMANCE OF BiC9 HBT VAR. VCOS AT ROOM TEMPERATURE

Wafer		1	2	3	4
Center frequency (GHz)	Mean	99.6	100.5	100.1	100.5
	Standard deviation	0.64	0.17	0.3	0.2
Tuning range (GHz)	Mean	3.4	3.6	3.6	3.7
	Standard deviation	0.78	-14.2	-14.6	-15
Output power (dBm)	Mean	-1.1	-1	-1.4	0.9
	Standard deviation	-11.7	0.2	0.2	0.1
DC power (mW)	Mean	133.0	133.0	136.2	132.8
	Standard deviation	4.4	1.6	2.5	1.6

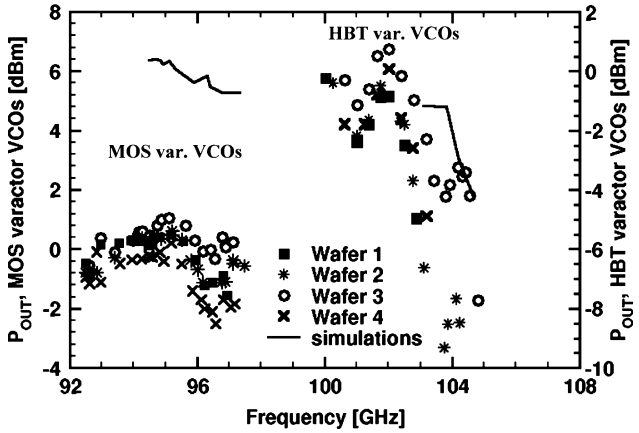


Fig. 20. Output power versus center frequency for 100 GHz BiC9 VCOs on different wafers.

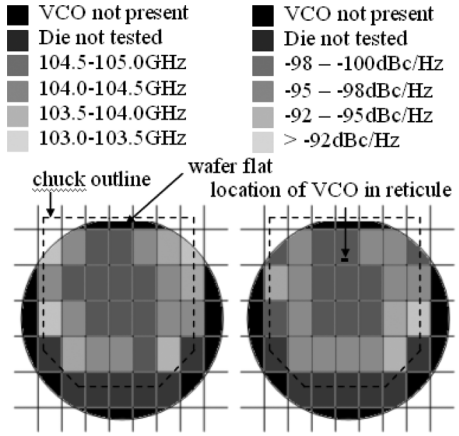


Fig. 21. BipX1 wafer maps of oscillation frequency (left) and phase noise at 1 MHz (right).

Fig. 21 reproduces wafer maps of oscillation frequency and phase noise as functions of location for BipX1 VCOs. Both plots show that dice at the center of the wafer perform better than dice on the edges.

VI. CONCLUSION

W-band low voltage VCOs have been presented with record phase noise for SiGe VCOs above 80 GHz. A design methodology for minimizing sensitivity to temperature and power supply has been presented and experimentally verified. Experimental results indicate that the optimal bias current density for low phase noise SiGe HBT W-band VCOs approaches the peak f_T/f_{MAX} current density. Additionally, differentially

tuned MOS varactors are shown to be superior to HBT varactors for achieving low phase noise. Furthermore, while VCO performance improves when SiGe technology is scaled, the oscillation frequency—determined by passive components—is insensitive to scaling. Wafer mapping and temperature data show that SiGe HBTs with over 200 GHz f_{MAX} are required to obtain production-quality W-band VCOs.

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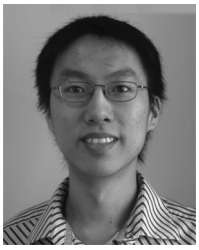

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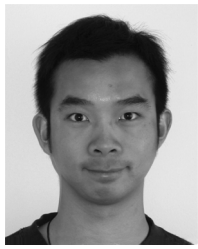

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