Methodology for Simultaneous Noise and Impedance Matching in W-Band LNAs

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***Abstract* — This paper presents a step-by-step methodology for simultaneous noise and input impedance matching in CMOS and SiGe W-band LNAs. This technique yields either increased gain or reduced power dissipation. Additionally, techniques to determine the optimum layout for MOSFETs in mm-wave LNAs are discussed. Measurement results in 90nm CMOS show a 1-stage 1.8V, 78GHz LNA with 3.8dB gain and 16mW power dissipation, and a 1.8V, 2-stage 94GHz LNA with 4.8dB gain, and 30mW power dissipation. In all cases S_{11} and S_{22} are lower than -10 dB.**

***Index terms* — Millimeter-wave circuits, LNAs, W-band, radio frequency CMOS, noise matching.**

I. Introduction

The low-noise amplifier is a critical building block in almost every radio system. Several SiGe V-band (50-75GHz) and W-band (75-110 GHz) LNAs have been reported [1]-[3]. The development of CMOS mm-wave LNAs is strictly below 60GHz and has lagged SiGe development [4]-[8]. Here, the first W-band 90nm CMOS LNAs, using improvements to an existing gigahertz-range noise and impedance matching technique, are presented.

Traditional LNA design employed lossless reactive components to transform the signal source impedance to the optimum noise impedance of a transistor biased at NF_{min} current density [9]. Unfortunately this methodology compromises the input impedance matching.

In integrated circuit LNAs, the designer can control the optimum noise impedance and bias current of the input transistor by adjusting its emitter length (or gate width). Thus, it is possible to obtain simultaneous noise and impedance match at the input of a SiGe or CMOS integrated circuit LNA. The method employed to achieve this was first presented in [10]-[11], and will be reviewed in section 2 of this paper. The methodology in [10] however, has two important limitations that arise in mm-wave LNAs.

The first limitation is caused by the pad capacitance at the LNA input, which appears in parallel with the source resistance. The pad capacitance, which might be as large as 50fF, is a negligible 530 Ω at 6 GHz, but only 53 Ω at 60 GHz. Section 3 presents an improved matching methodology that accounts for the pad capacitance. A second limitation arises because bond wires are often used to connect an LNA to an off-chip antenna. Section 4 describes how to account for the bond wire inductance from the outset of the design process, without iteration.

Section 5 discusses the effects of MOSFET finger width and gate contact arrangement on LNA performance, and presents equations which accurately model gate resistance. Finally, measurement results are summarized in section 6.

II. Original Methodology for Simultaneous Noise and Input Impedance Matching

The original methodology for achieving simultaneous noise and input impedance match in integrated LNAs can be summarized neatly in 4 steps. For a detailed description and theoretical derivation of each step, see [10]-[11]. Note that an alternate design approach for RF CMOS LNAs focuses on meeting power dissipation constraints [12].

STEP 1: Optimum Biasing

In all SiGe and CMOS technologies, there is an optimum current density that minimizes transistor NF [13]-[15]. The LNA transistors should be biased at this current density.

STEP 2: Device Size

The device size should be chosen such that the real part of the optimum noise impedance (1), is equal to the source impedance at the design frequency. Because G_{cor}, B_{cor}, and G_u increase with frequency [11], lower frequency LNAs require larger devices and therefore have higher power dissipation [15].

$$\frac{1}{Z_{sopt}} = \sqrt{G_{cor}^2 + \frac{G_u}{R_n}} - jB_{cor} \qquad (1)$$

STEP 3: Impedance matching

The input impedance of the amplifier (Z_{IN}), given by (2) is now tuned to the source impedance (Z_0) using two inductors L_S and L_G, as illustrated in Figure 1 [10,14]. Decomposing (2) into its real and imaginary parts yields the required values of L_S (3) and L_G (4). If a pad is now added at the LNA input the amplifier is no longer matched correctly. Note that L_S does not affect the real part of Z_{SOPT} [10], [11], [15].

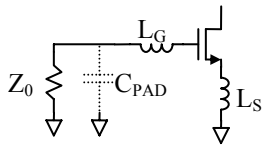

Figure 1: Schematic of LNA input.

$$Z_{IN} = \omega_T L_S + j\left(\omega L_S + \omega L_G - \frac{\omega_T}{\omega g_m}\right) \qquad (2)$$

$$L_S = \frac{Z_0}{\omega_T} \qquad (3) \qquad\qquad L_G = \frac{\omega_T}{\omega^2 g_m} - L_S \qquad (4)$$

STEP 4: Gain Optimization

Finally, an inductive load is employed to maximize amplifier gain and linearity. When the LNA is matched at *input and outp*ut the power gain is given by (5), where R_P is the output impedance of an inductively loaded LNA *at*

resonance. In cases where feedback is strong, as in SiGe HBT LNAs, the gain can be simplified as shown.

$$|G| = \frac{1}{2} R_P Z_0 \left| \frac{g_m}{1 + j(\omega/\omega_T) Z_0 g_m} \right|^2 \approx \frac{1}{2} \left(\frac{\omega_T}{\omega} \right)^2 \frac{R_P}{Z_0} \qquad (5)$$

Given that Z_0 and g_m were fixed to minimize noise figure, the only means of increasing the amplifier gain is to use a higher-Q load; ultimately, the gain is limited by the device output resistance.

III. Matching Methodology for W-Band LNAs

In the W-band, the impedance of C_{PAD} cannot be neglected in the matching process. The optimum noise impedance of the transistor must be matched to the real part of Z_S, and the input impedance Z_{IN} must be conjugately matched to Z_S. Z_S, given by (6), has a real part which is a factor of k, given by (7), smaller than Z_0.

$$Z_S = \frac{Z_0}{1 + \omega^2 C_{PAD}^2 Z_0^2} - j \frac{\omega C_{PAD} Z_0^2}{1 + \omega^2 C_{PAD}^2 Z_0^2} \qquad (6)$$

$$k = 1 + \omega^2 C_{PAD}^2 Z_0^2 \qquad (7)$$

The new emitter length ($l_{EM(new)}$) or gate width ($W_{G(new)}$) required for optimum noise match increases by the same factor k, as shown in (8). The larger device size leads to increased transconductance and bias current (9), again by a factor of k.

$$W_{G(new)} \text{ or } L_{E(new)} = kW_G \text{ or } kl_{EM} \qquad (8)$$

$$g_{m(new)} = kg_m \qquad I_{DS(new)} = kI_{DS} \qquad (9)$$

To find the the new values of L_S and L_G, consider that (10) must be satisfied for optimal impedance match.

$$Z_S^* = \omega_T L_{S(new)} + j\left(\omega L_{S(new)} + \omega L_{G(new)} - \frac{\omega_T}{\omega g_{m(new)}} \right) \qquad (10)$$

Substituting (6) into (10) and solving, the new values for L_S and L_G are given by (11) and (12) respectively.

$$L_{S(new)} = \frac{Z_0}{k\omega_T} \qquad (11)$$

$$L_{G(new)} = \frac{Z_0^2 C_{PAD}}{k} - L_{S(new)} + \frac{\omega_T}{\omega^2 g_{m(new)}} \qquad (12)$$

Note that $L_{S(new)}$ is decreased by a factor of k, resulting in weaker feedback, and correspondingly higher gain (helped also by increased g_m). The reduction in L_S and L_G results in lower series resistance and higher self-resonance frequency for these passives, and correspondingly less noise figure degradation. Table 1 provides numerical examples of the new design technique, applied to SiGe and CMOS mm-wave LNAs at 60GHz, 77GHz, and 94GHz.

IV. Accounting for Bond Wire Inductance

Often, a bond wire is used to connect the LNA input to an off-chip antenna. At mm-waves, the bondwire impedance must be accounted for to achieve noise and impedance matching. The bondwire and bondpads are represented by the π-network shown in Figure 2, which can be thought of as an impedance transformer. Note that even if C_{P1} is not present, L_W and C_{P2} still form an impedance transformer.

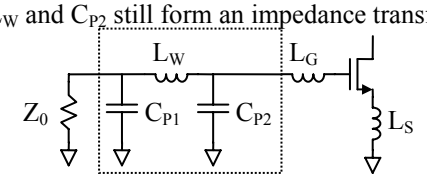

Figure 2: Noise matching with bondwire and bondpads.

The minimum values of C_{P1}, C_{P2} and L_W are set by the (packaging) technology and transform Z_0 to another real impedance n× Z_0 at the desired frequency. The input transistor size and bias current must thus be modified to match to n×Z_0. The new LNA parameters are given in Table 2, in terms of the parameters derived in section 2. The gain of the new LNA is given by (14). The designer has some limited freedom to choose *n* if larger L_w and C_{p1} and C_{p2} can be tolerated.

Table 2: LNA parameters when noise and imedance matched to n×Z_0.

Parameter	*LC transformer*
device size	$W_{G(new)} = W_G/n$
g_m	$g_{m(new)} = g_m/n$
I_{DS}	$I_{DS(new)} = I_{DS}/n$
L_S	$L_{S(new)} = nZ_0/\omega_T$
L_G	$L_{G(new)} = nL_G$

$$|G|_{(new)} = \frac{1}{2n} R_P Z_0 \left| \frac{g_m}{1 + j(\omega/\omega_T) Z_0 g_m} \right|^2 \approx \frac{1}{2n} \left(\frac{\omega_T}{\omega} \right)^2 \frac{R_P}{Z_0} \qquad (14)$$

Setting n = 1 maximizes the matching bandwidth, and minimizes the sensitivity of the match to variations in L_W, C_{P1} and C_{P2}. The matching methodology from section 2 can be applied directly.

If n < 1 the analysis is similar to that covered in section 3. The results are larger device size, greater gain, and reduced values of L_G and L_S. Note that n < 1 is impossible if C_{P1} = 0.

Choosing n > 1 leads to reduced gain, lower power consumption, and larger values of L_G and L_S. Choosing n > 1 is appropriate in applications where the design frequency is much lower that the device f_T and minimizing power consumption is important.

V. CMOS LNA Design in the W-Band

To verify the new noise and impedance matching methodology, and to evaluate CMOS for W-band applications, 77/94GHz LNAs were designed and fabricated in STM's 90nm CMOS technology. The schematics of the LNAs are shown in Figure 3, and consist of three topologies: a 1-stage cascode, a 2-stage cascode, and a 2-stage transformer-coupled cascode. The designs employ a combination of lumped inductors over substrate, allowing compact layout, and transmission lines over metal, allowing easy routing of power and ground planes. An inductor is placed between the input and cascode devices to improve the gain and noise figure by creating an artificial

transmission line with with C_{GS2}, C_{SB2}, C_{GD1} and C_{DB1} [4], [16]. Note that in SiGe mm-wave LNAs the benefits of adding this inductor are smaller because the "middle pole" is at a much higher frequency.

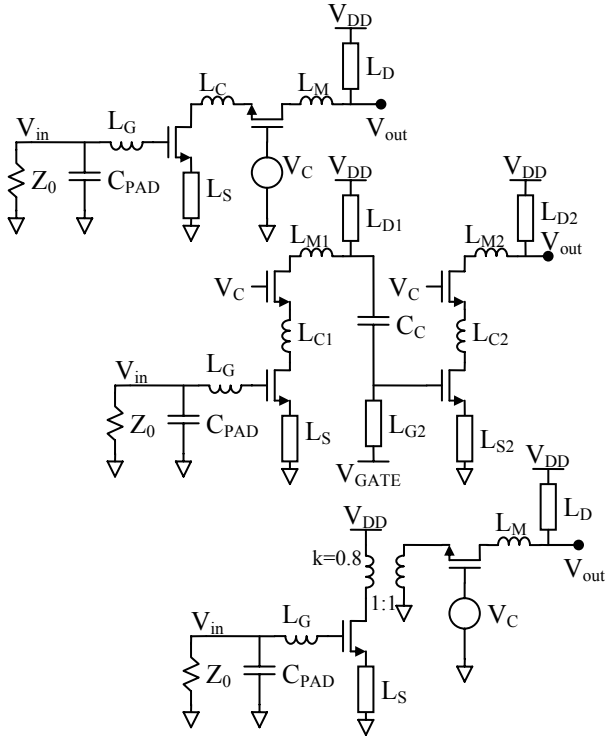

Figure 3: a) 1-stage, b) 2-stage cascode and c) transformer-coupled LNA schematics

Unlike SiGe HBTs, MOSFET performance is extremely sensitive to device layout. The f_T and f_{MAX} of MOSFETs depend upon finger width, drain and source metallization, and gate and substrate contact arrangement [15]. To investigate the effects of these layout issues upon LNA performance, three single stage cascode LNAs were designed, each with a different device layout but identical gate width. Based upon simulation results with extracted RC parasitics, the layout that yielded the best performing single stage cascode was chosen to design the remaining two LNAs. Note that although the variation of f_{MAX} with finger width is captured in simulation, the variation of f_T seen in measurements of 90nm MOSFETs is not captured [13], [15].

The three MOSFET layouts are described in Table 3 and illustrated in Figure 4. To meet electromigration rules at 100ºC, and to minimize parasitic C_{DS} caused by the closely spaced, vertically stacked metals on the drain and source regions, the metallization is tapered as shown in Figure 4.

Only digital MOSFET models were available, and therefore the impact of the gate resistance was not captured. The gate resistances for a single gate finger with single-sided and double-sided contacts are given by (16) and (17) respectively, where N_{cont} is the number of contacts per finger, R_{cont} is the contact resistance, R_{sq} is the poly resistance per square, W_{ext} is the gate extension beyond the active region, and L_{phys} is the physical gate length, typically 65nm in this technology. Double-sided contacts reduce R_{gate}, but increase parasitic capacitance and thus reduce f_T and, unbeknownst to many, also f_{MAX}.

Table 3: Description of MOSFET layouts.

	W_{finger} (μm)	Width (μm)	Contacts
A	1	36	single-sided
B	2	36	double-sided
C	1.5	36	single-sided

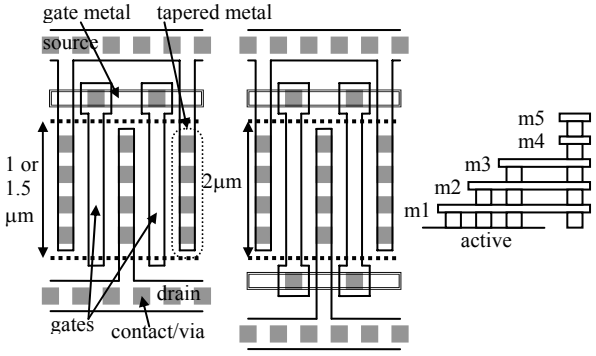

Figure 4: MOSFETs with different gate connections.

$$R_{gate} = \frac{R_{cont}}{N_{cont}} + \frac{R_{sq}}{\ell_{phys}}\left[W_{ext} + \frac{W_f}{3}\right] \quad (16)$$

$$R_{gate} = \frac{R_{cont}}{N_{cont}} + \frac{R_{sq}}{2\ell_{phys}}\left[W_{ext} + \frac{W_f}{6}\right] \quad (17)$$

Using (16) and (17), the gate resistances of the MOSFET layouts summarized in Table 3 and Figure 4 were calculated and manually added to post-layout extracted netlists of the MOSFETs. The post-layout simulation results for the three LNAs are summarized in Table 4, and indicate that layout C, with single-sided gate contacts and 1.5µm fingers is superior.

Table 4: LNA performance summary (simulations).

	S21 (dB_{20})	NF (dB_{10})
A	3.63	4.78
B	4.36	4.88
C	5.04	4.63

Table 5: LNA performance summary (measurements).

LNA	S21 (dB_{20})	frequency (GHz)	Power supply (V)	Current (mA)
1-stage	3.8	78	1.8	8
2-stage	4.8	94	1.8	16
xfmr	1.65	92	1.5	23

VI. Measurement Results

Shown in Figure 5 are the S-parameter measurements for the fabricated LNAs. To the authors' knowledge, these are the first W-band LNAs fabricated in CMOS technology. The S-parameters and DC performance of the LNAs are summarized in Table 5. Due to lack of equipment, we cannot measure the LNA noise figure above 65GHz. However, good agreement between simulations and receiver noise figure measurements was found in a 60-GHz radio receiver fabricated in the same process [8]. Die photo micrographs of the LNAs are shown in Figure 6.

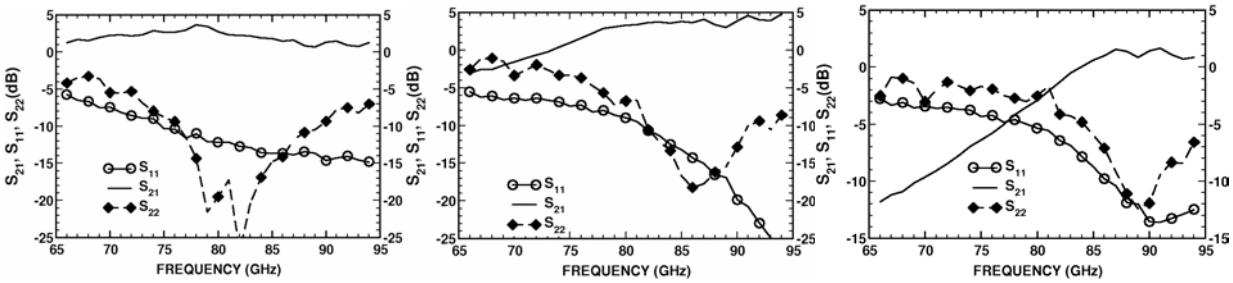

Figure 5: LNA S-parameter measurements (a) single stage cascode, (b) two-stage cascode, (c) transformer coupled cascode.

Table 1: Numerical design examples of LNAs from 60GHz to 94GHz.

Parameter	65GHz cascode 0.18µm SiGe HBT [3]	60GHz cascode 90nm CMOS [4]	77GHz cascode 90nm CMOS [this work]	94GHz cascode 90nm CMOS [this work]
Device f_T and cascode f_T	125GHz/110GHz	128GHz/80GHz	128GHz/80GHz	128GHz/80GHz
Device size	9µm by 0.18µm	34µm	30µm	26µm
C_{PAD}	12fF	20fF	20fF	20fF
k	1.06	1.142	1.234	1.349
J_{DS} (J_{CE})	2.4mA/µm^2	0.2mA/µm	0.3mA/µm	0.3mA/µm
I_{DS} (I_{CE}) and g_m	3.9mA & 110mS	6.9mA & 34mS	8.7mA & 30mS	7.8mA & 26mS
$L_{S/E}$, $L_{G/B}$	60pH, 90pH	55pH, 155pH	50pH, 110pH	45pH, 80pH
Gain	8.2dB	6.8 dB	5.0 dB	3.5 dB

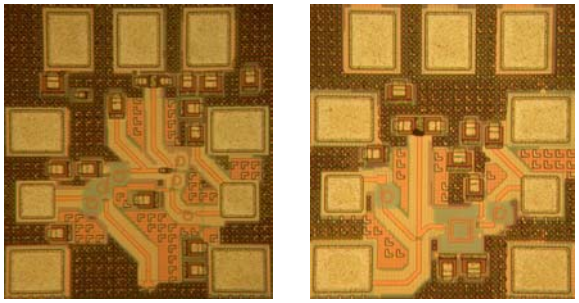

Figure 6: Die photos of a) 2-stage cascode and b) transformer-coupled CS-CG LNA.

VII. Conclusion

An algorithmic design methodology for simultaneous noise and input impedance matching in mm-wave LNAs has been presented and verified using design examples and measurement results. It directly accounts for the pad capacitance and bond wire inductance without requiring iteration. Finally, the first CMOS W-band LNAs at 77GHz and 94GHz have been experimentally demonstrated.

Acknowledgements

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