Comparison of Si CMOS, SiGe BiCMOS and InP HBT Technologies for High-Speed and Millimeter-Wave ICs

Sorin Voinigescu[1], Timothy Dickson[1],
Rudy Beerkens[2], Paul Westergaard[1], and Imran Khalid[2]

1) University of Toronto
2) STMicroelectronics, Ottawa, Canada

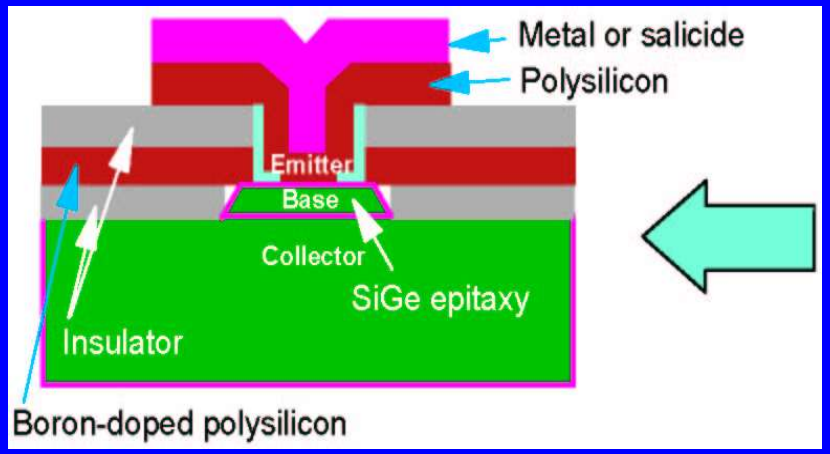
5th. SiRF Topical Meeting, Atlanta, Sept.10, 2004

Outline

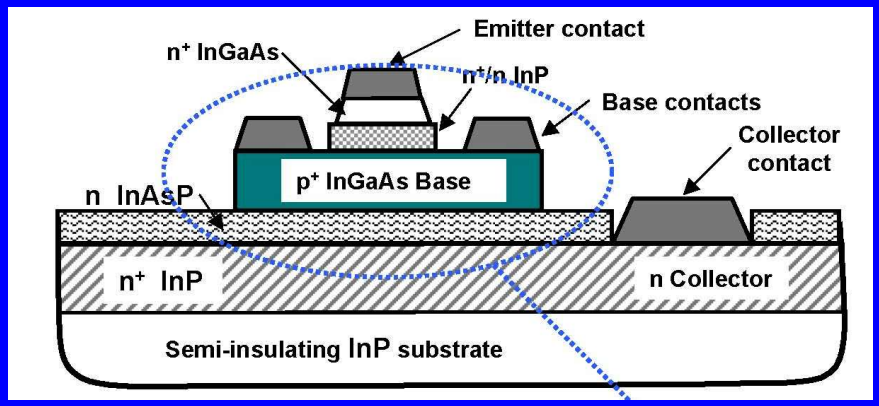
- Device Structures
- Figures of merit for mm-wave ICs and high-speed logic
- Circuit examples
- Conclusions

Device structures

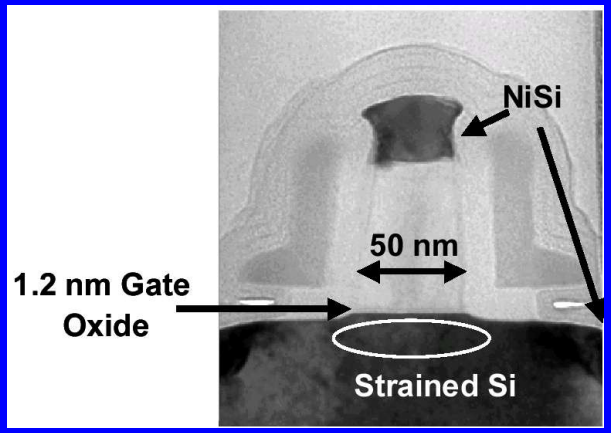
- SiGe HBT



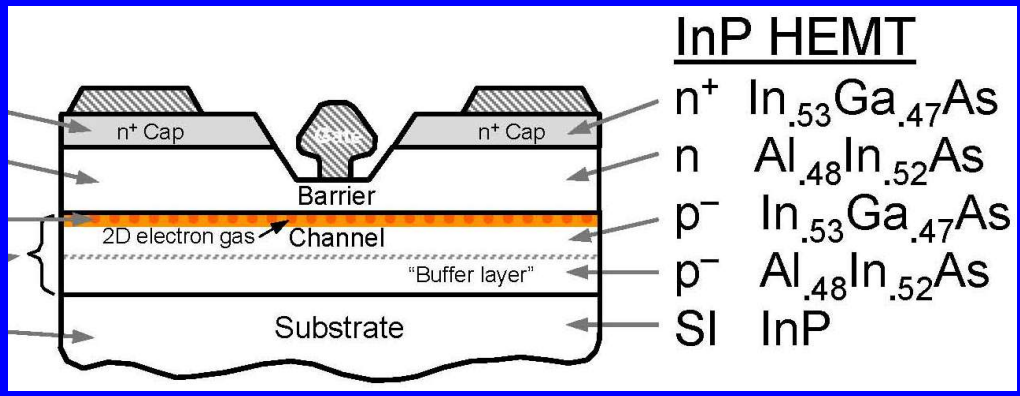
- InP (GaAs) HBT



- Si n-MOSFET



- InP(GaAs)HEMT



What drives device performance?

- Material properties
  - electron mobility (InP > SiGe > Si)
  - hole mobility (SiGe > Si > InP)
  - saturation velocity (InP > Si/SiGe)
  - breakdown field (InP > Si)
  - thermal conductivity (Si > SiGe > InP)
- Lithography (Si > InP)
- Yield & reliability (MOS > SiGe HBT > InP HBT)

FoMs for mm-wave ICs

Devices

– f_T, f_{MAX}, F_{MIN}, R_n (analog: g_m, g_o, $g_m/I_{C(DS)}$, g_m/g_o)

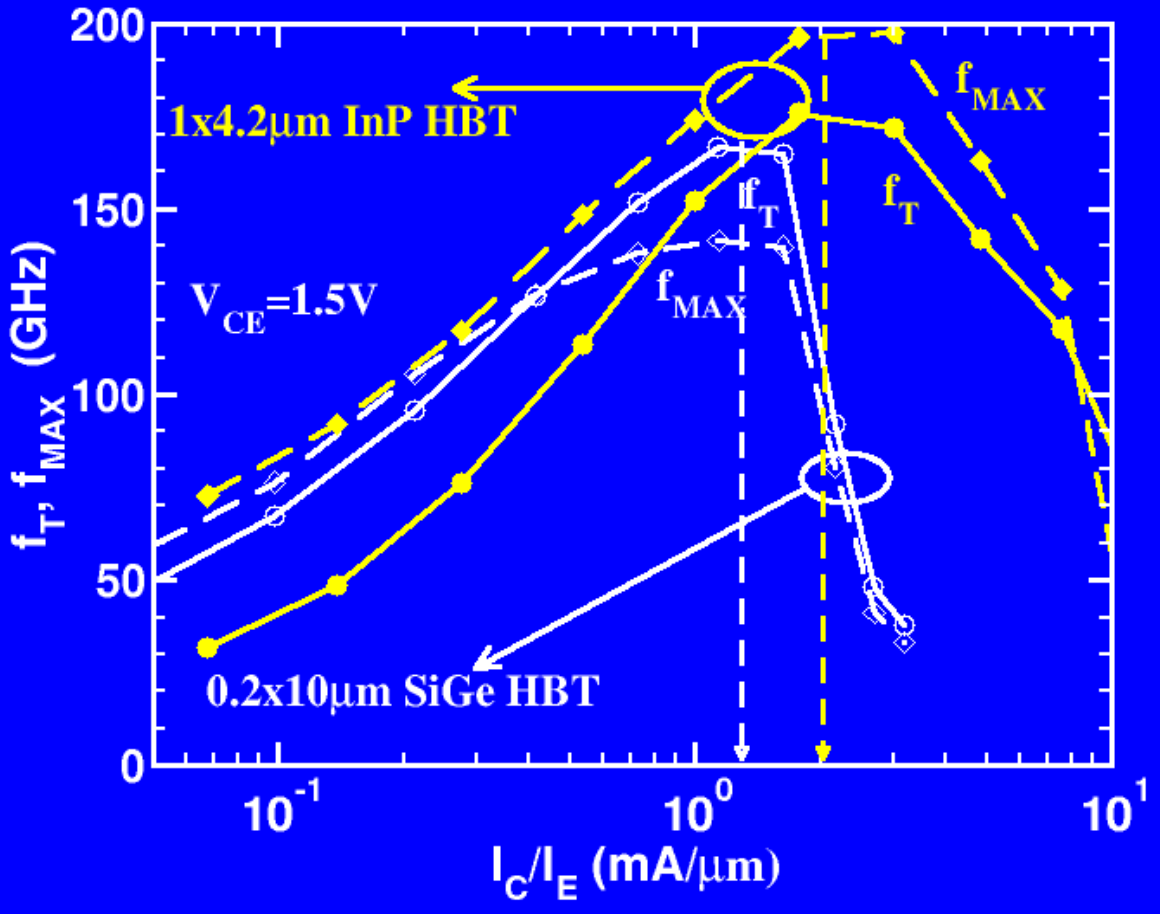
Circuits

$$FoM_{LNA} = \frac{G \times IIP3 \times f}{(F-1) \times P} = \frac{OIP3 \times f}{(F-1) \times P}$$

$$FoM_{VCO} = \left(\frac{f_o}{\Delta f}\right)^2 \frac{P_{out}}{L[\Delta f] \times P}$$

$$FoM_{PA} = P_{out} \times G \times PAE \times f^2$$

InP vs.SiGe HBT: f_T, f_{MAX}



InP HBT:

2 mA/μm

V_{BE} = 0.75V

SiGe HBT:

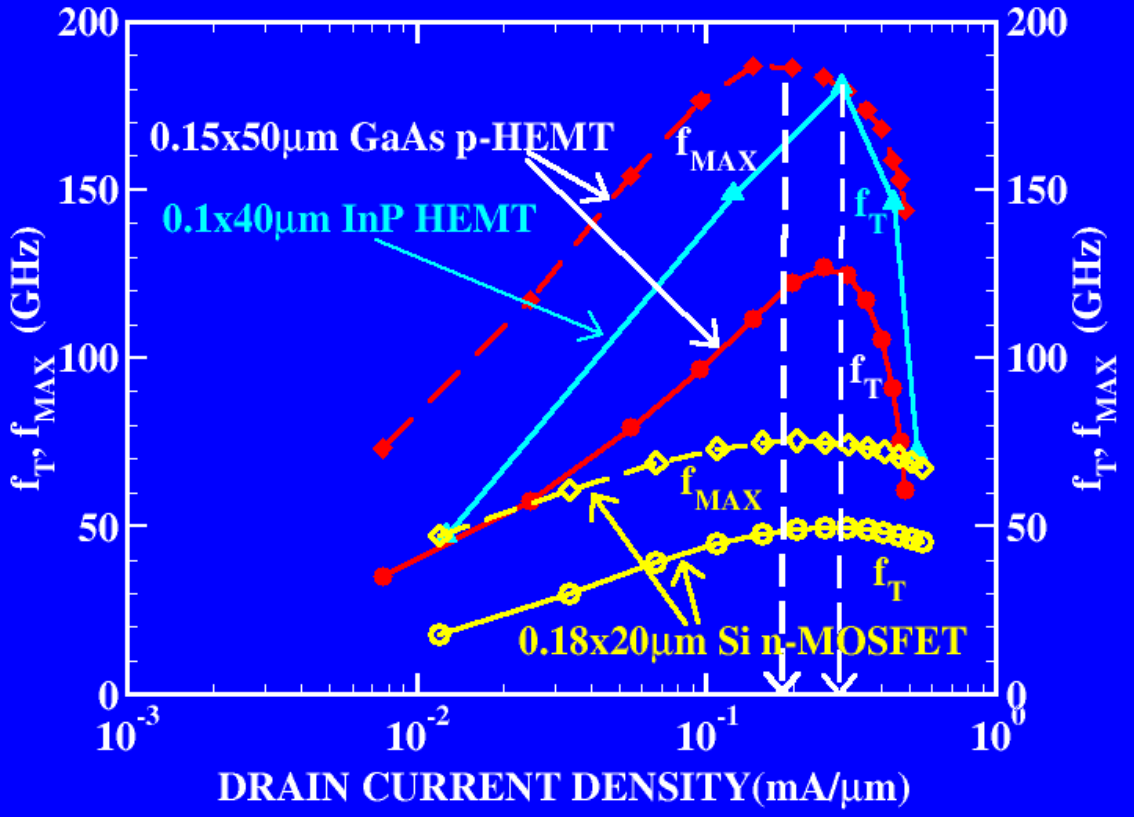
1.2 mA/μm

V_{BE} = 0.9V

$$f_{MAX} \approx \sqrt{\frac{f_T}{8\pi R'_b C'_{cb}}}$$

$$\frac{1}{2\pi f_T} = \tau_{EC}(I_C) = \tau_B + \tau_C + \frac{kT}{q I_C}(C_{je} + C_{cb}) + (R_e + R_c) C_{cb}$$

Si vs. III-V FETs: f_T, f_{MAX}



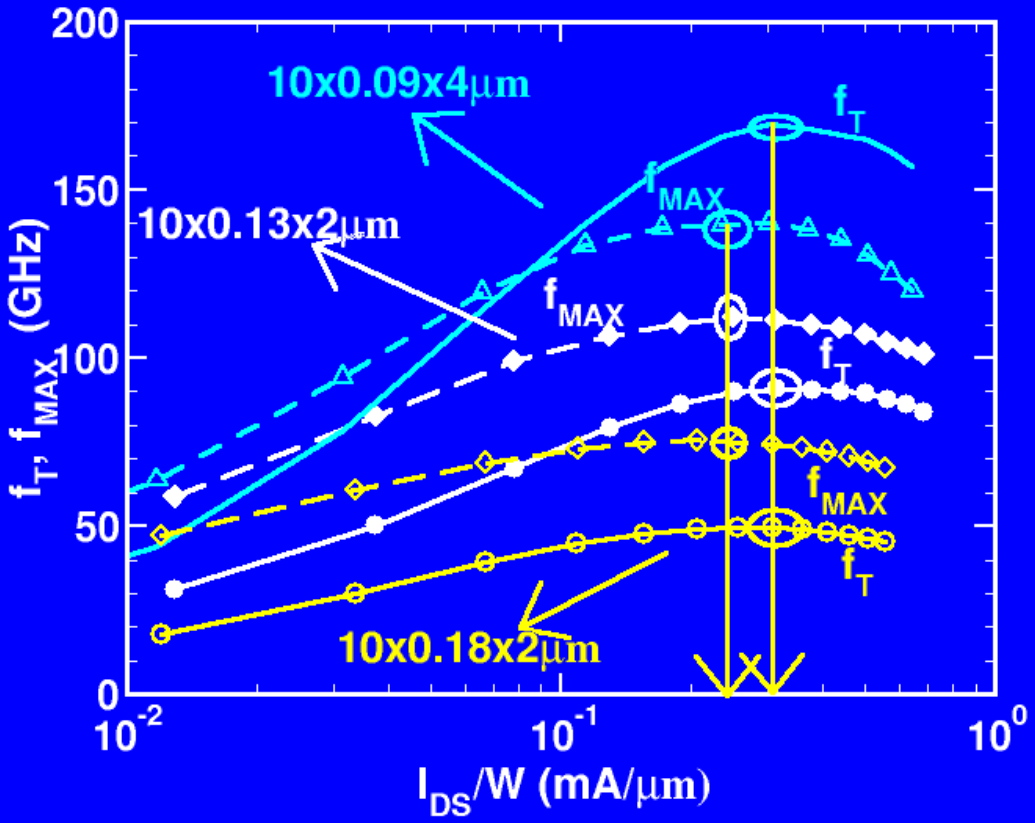
All FETs

peak f_T: 0.3 mA/μm

peak f_{MAX}: 0.2 mA/μm

$$\frac{1}{2\pi f_T} = \frac{(C_{gs}+C_{gd})}{g_m} + (R_s+R_d)C_{gd} + \left(\frac{C_{gs}}{1+g_m R_s} + C_{gd}\right) R_d \frac{g_{ds}}{g_m}$$

Impact of constant field scaling: fixed MOSFET current density!



$$f_{MAX} \approx \frac{f_T}{2\sqrt{\frac{R_{gsq} W_f^2}{12(3) l_G}\left(g'_{ds} + 2\pi f_T C'_{gd}\right) + g'_{ds}\left(R'_i + R'_s\right)}}$$

Noise parameters

HBT

$n = 1$

$$R_n \approx \frac{1}{2 g_m} + (R_E + R_b)$$

$$Y_{sopt} \approx \frac{f}{f_T R_n}\left[\sqrt{\frac{g_m}{2}(R_E + R_b)} - j\frac{n}{2}\right]$$

$$F_{MIN} \approx 1 + \frac{1}{\beta} + \frac{f}{f_T}\sqrt{\frac{g_m}{2}(R_E + R_b)}$$

FET

$$P = \frac{2}{3} .. 1$$

$$R_n \approx \frac{P}{g_m} + (R_s + R_g)$$

$$Y_{sopt} \approx \frac{f}{f_T R_n}\left[\sqrt{P g_m (R_s + R_g)} - jP\right]$$

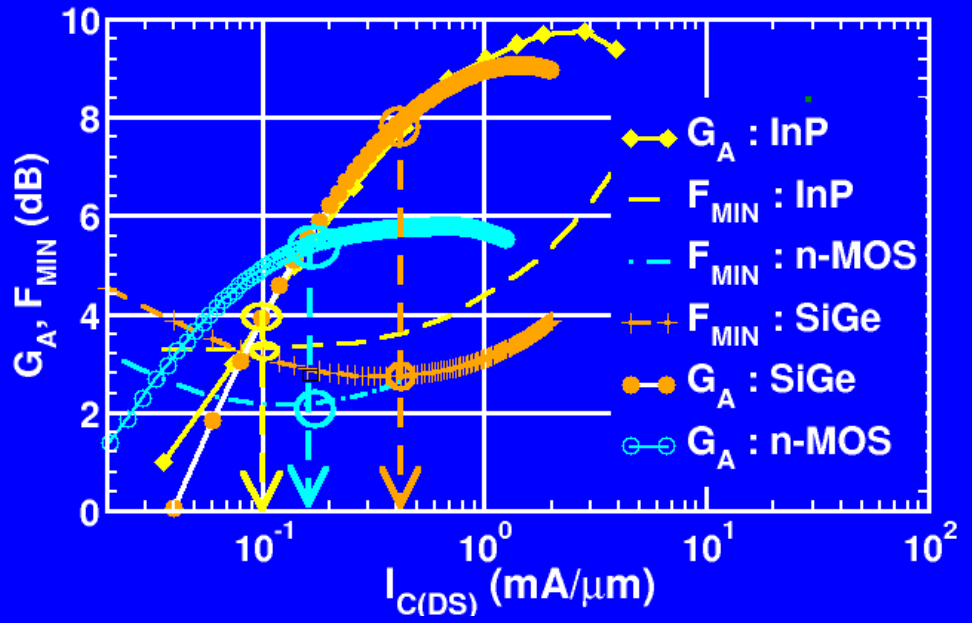
$$F_{MIN} \approx 1 + \frac{f}{f_T}\sqrt{P g_m (R_s + R_g)}$$

NF_{MIN}, f_{MAX} & linearity

- **Linearity**:

L. Larson, IEEE TED-2003

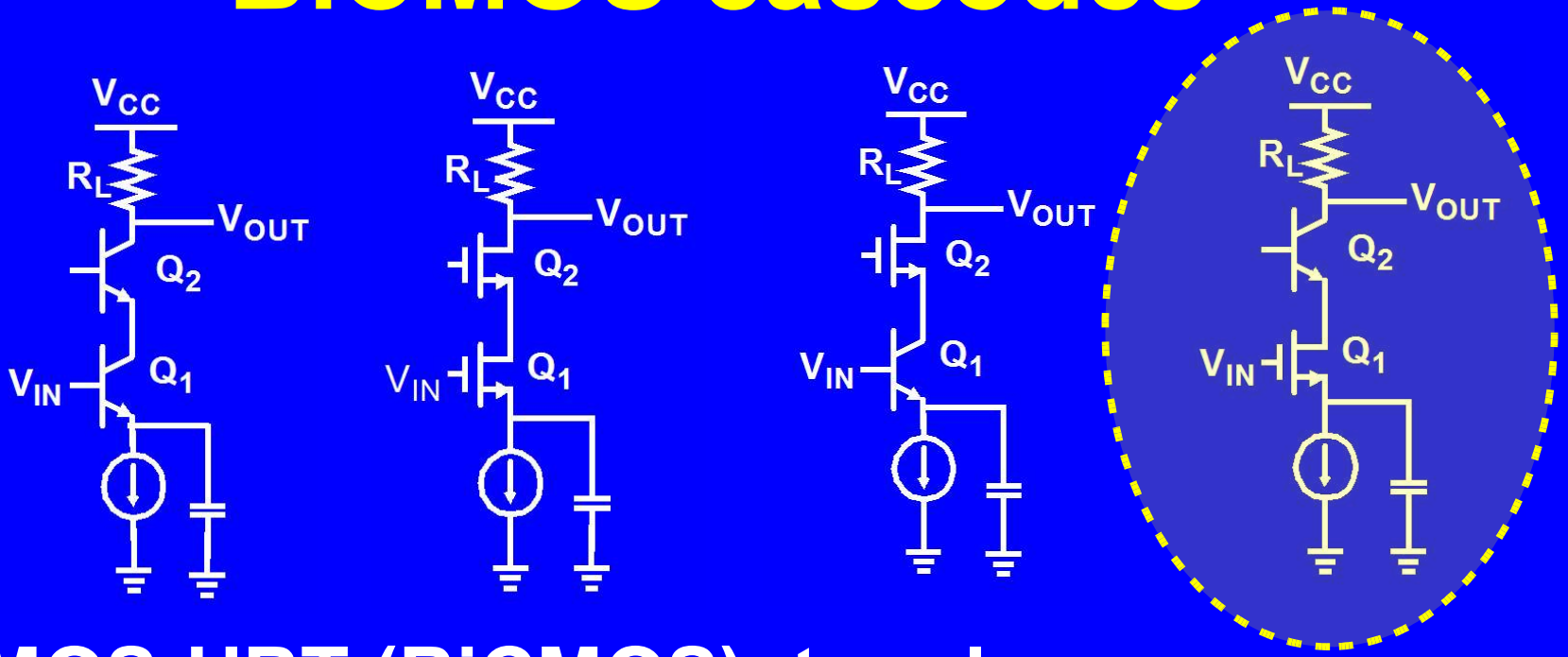
$$OIP3 \sim \frac{f_{MAX}}{\frac{\partial^2 f_{MAX}}{\partial I_{C(DS)}^2}}$$



- **MOSFET**: opt. NF_{MIN} current density = peak f_{MAX}
- **SiGe HBT**: opt. NF_{MIN} current density =1/3 peak f_{MAX}
- **InP HBT**: opt. NF_{MIN} current density << peak f_{MAX}

No compromise between NF_{MIN}, G_A and IIP3 in MOSFETs

BiCMOS cascodes



- **MOS-HBT (BiCMOS) topology:**
  - √ **lowest noise, highest linearity, highest MAG**
  - √ **low supply voltage ($V_{GS} < V_{BE}$)**
  - x **low g_m, high R_n, high sensitivity to mismatch**

High-Speed Logic FoM: CML Gate Delay

$$SL_{HBT} = \frac{I_{CpeakfT}}{C_{bc} + C_{cs}}$$

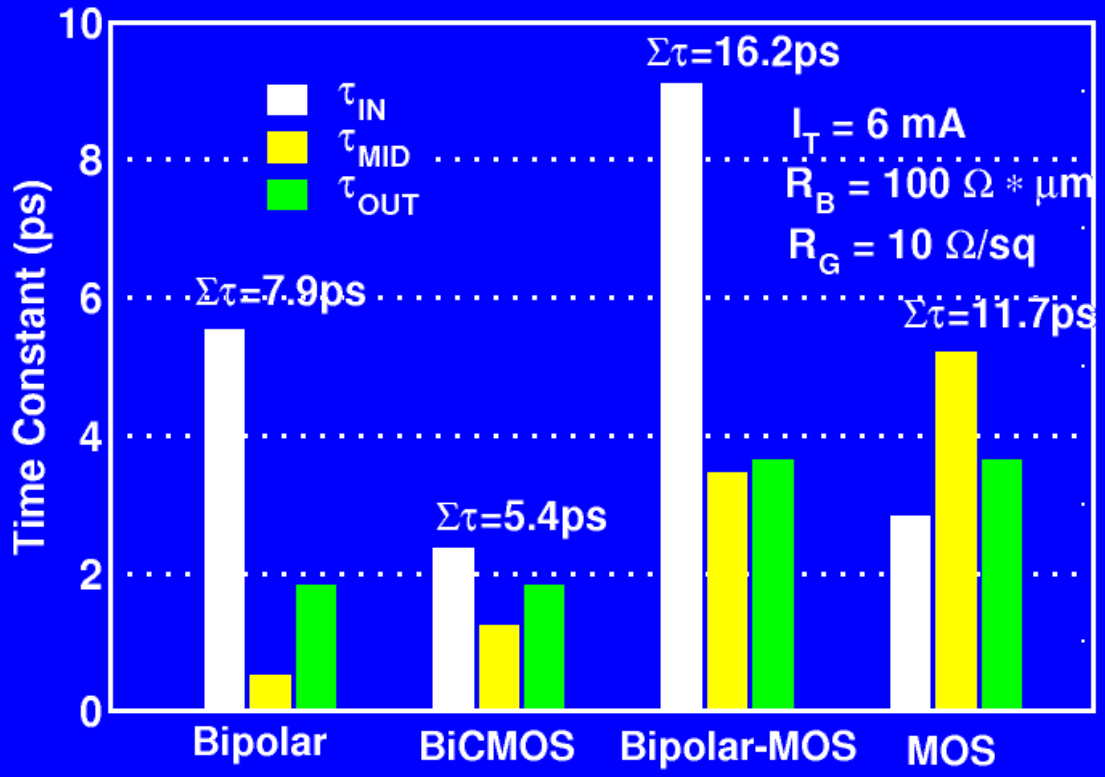
$$SL_{FET} = \frac{I_{DpeakfT}}{C_{gd} + C_{db}}$$

$$\tau_{HBT} \approx \Delta V \frac{C_{bc} + C_{cs}}{I_T} + \left(k + \frac{R_b}{R_L}\right) \Delta V \frac{C_\pi + (1 - A_V) C_{bc}}{I_T}$$

$$\tau_{FET} \approx \Delta V \frac{C_{gd} + C_{db}}{I_T} + \left(k + \frac{R_g}{R_L}\right) \Delta V \frac{C_{gs} + (1 - A_V) C_{gd}}{I_T}$$

$$\tau_{BiCMOS} \approx \Delta V \frac{C_\mu + C_{cs}}{I_T} + \left(k + \frac{R_g}{R_L}\right) \Delta V \frac{C_{gs} + C_{gd}}{I_T}$$

High-Speed CML gate delay

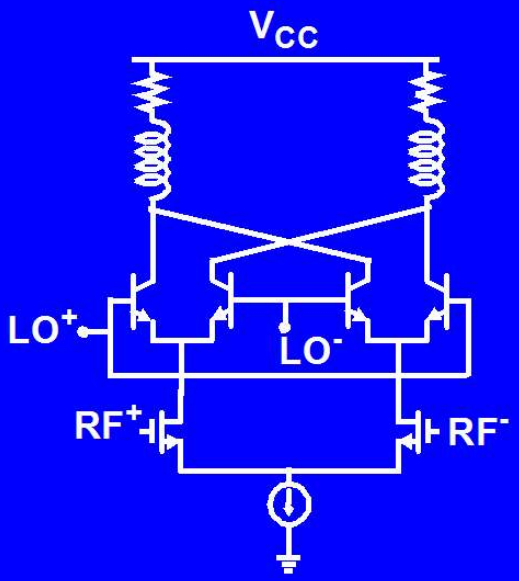


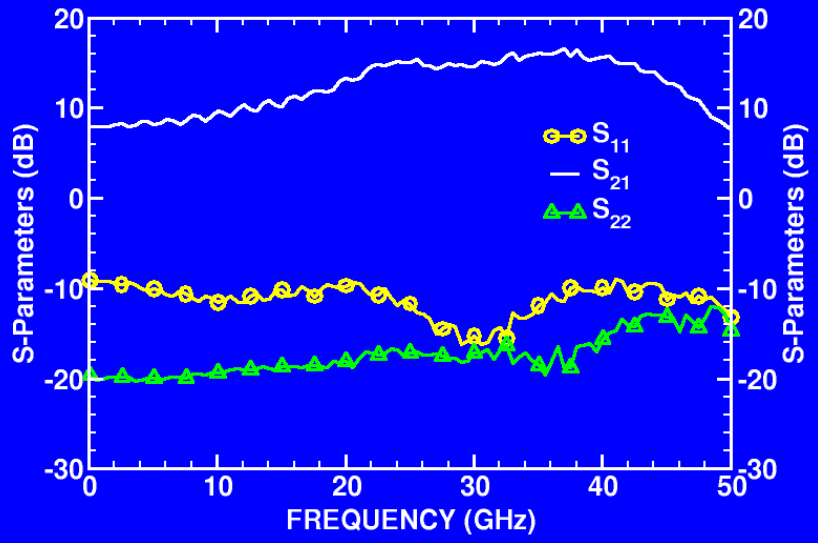
HBT-CML requires 250 .. 300 mV_{pp} swing, irrespective of node

MOS-CML requires 450 .. 300 mV_{pp} swing decreasing with node

Circuit Examples

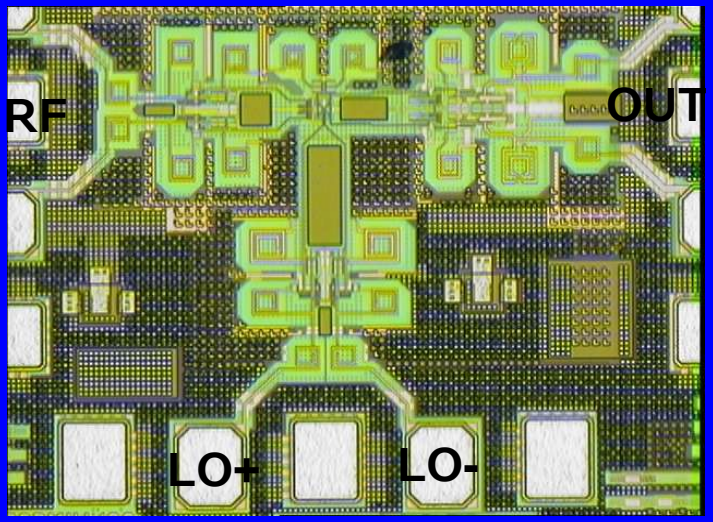
2.5-V, DC-to-45 GHz, SiGe BiCMOS Up/Downconv (T Dickson et al. IEEE Trans. MTT-2004)

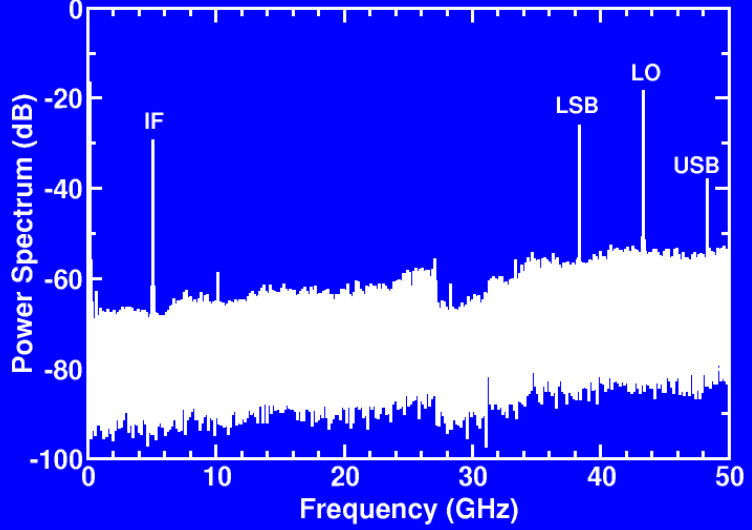




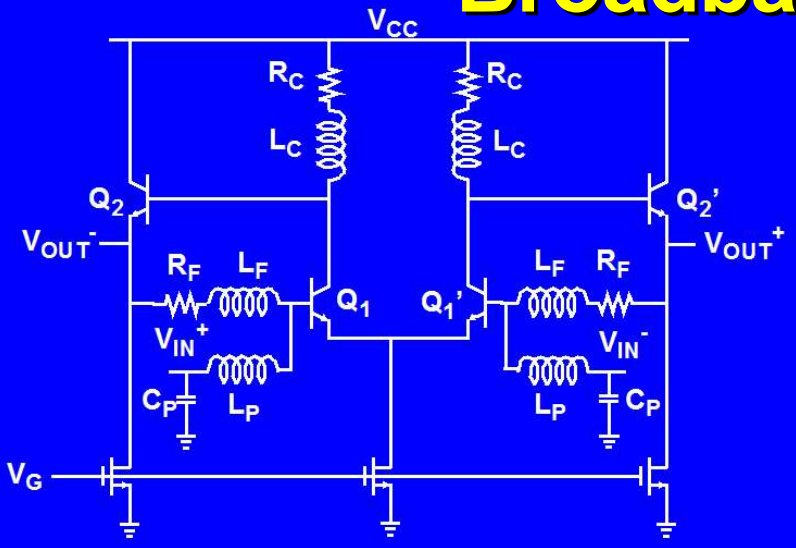
For comparison:

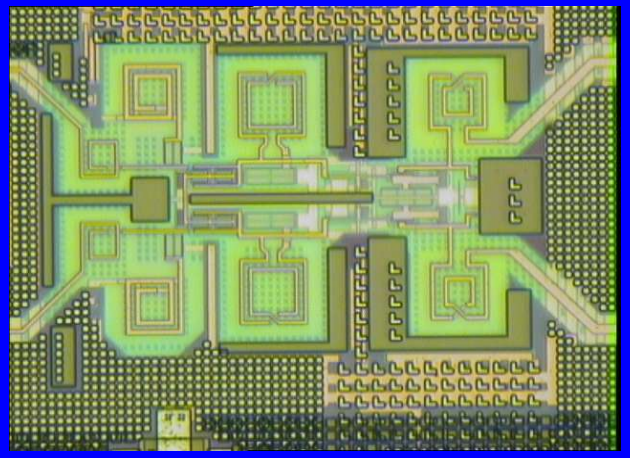
InP-HBT Mixer
Kobayashi, 2003
GaAs IC Symp.
- 3.3V,
- DC-40GHz,
- 20 dB gain

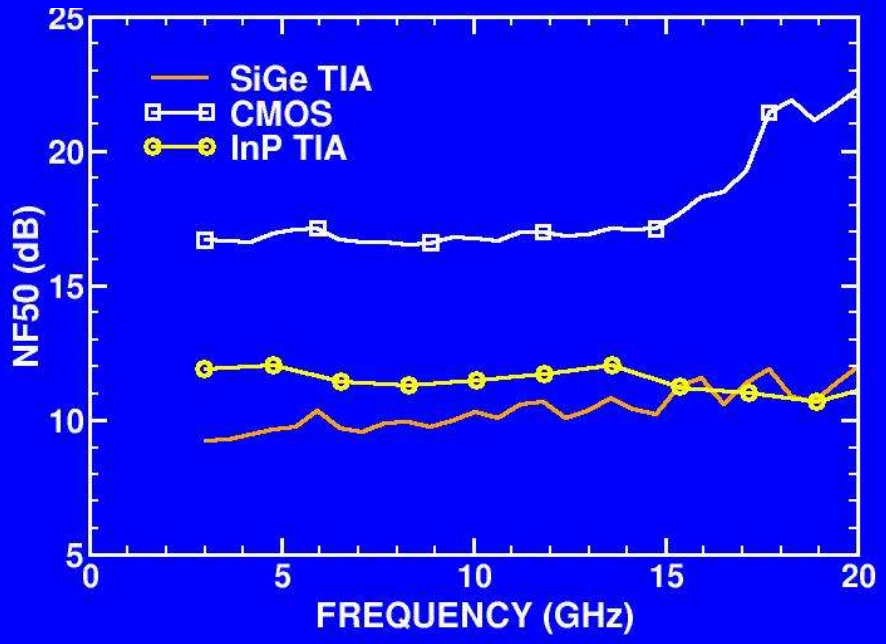


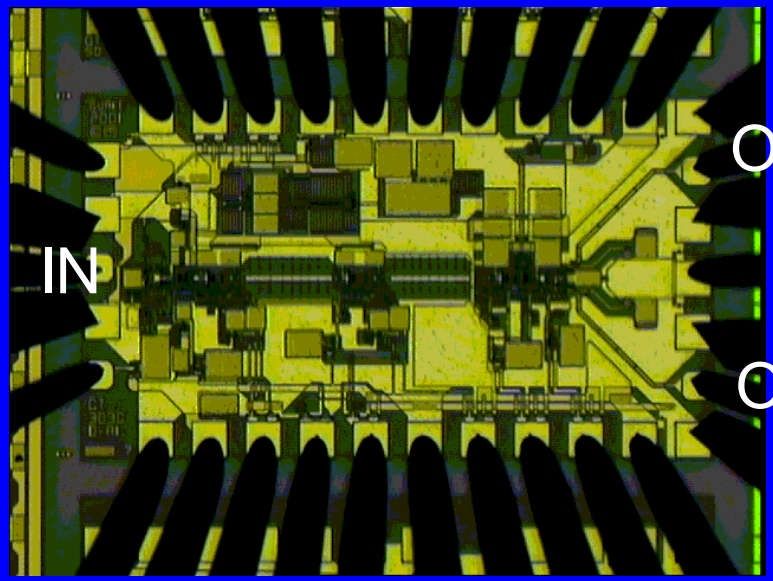


Si CMOS, SiGe BiCMOS, InP Low-noise Broadband Preamps



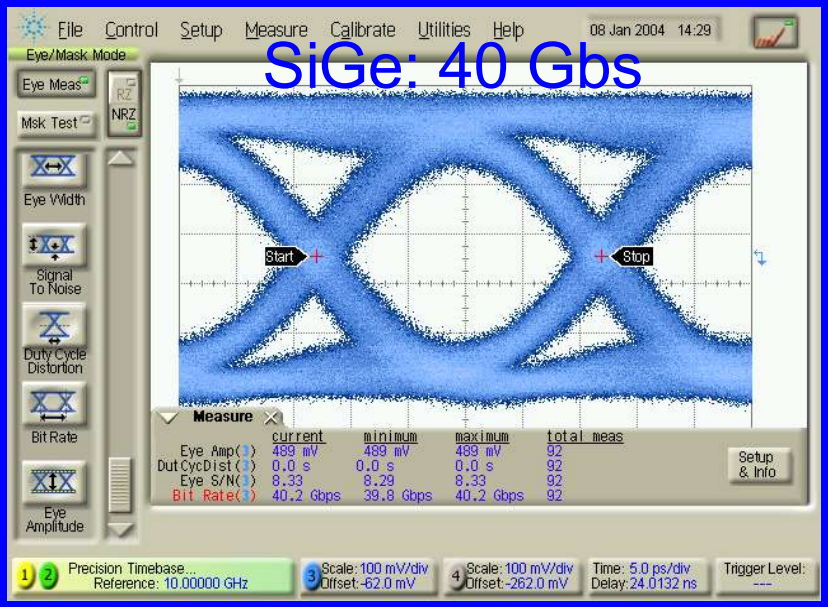


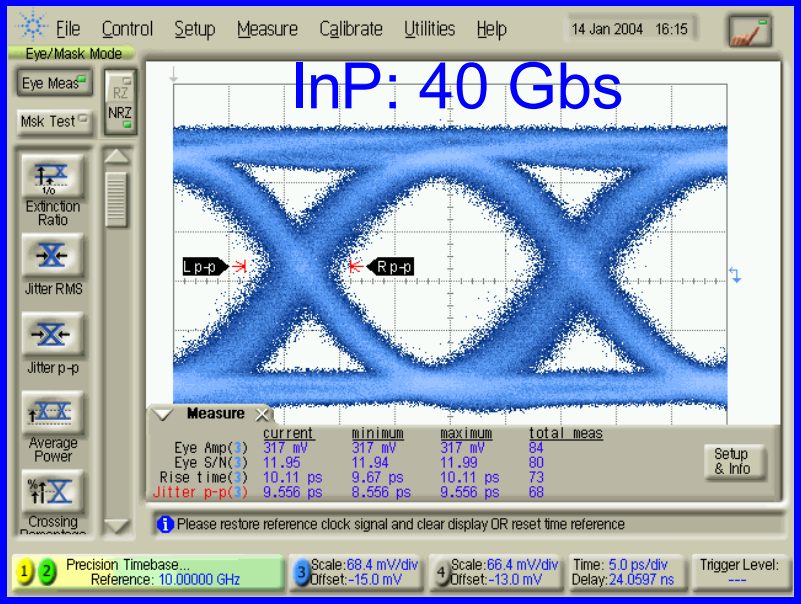




Si CMOS, SiGe BiCMOS, InP Low-noise Broadband Preamps: InP HBT

(H. Tran et al. GaAs IC Symp. 2003)

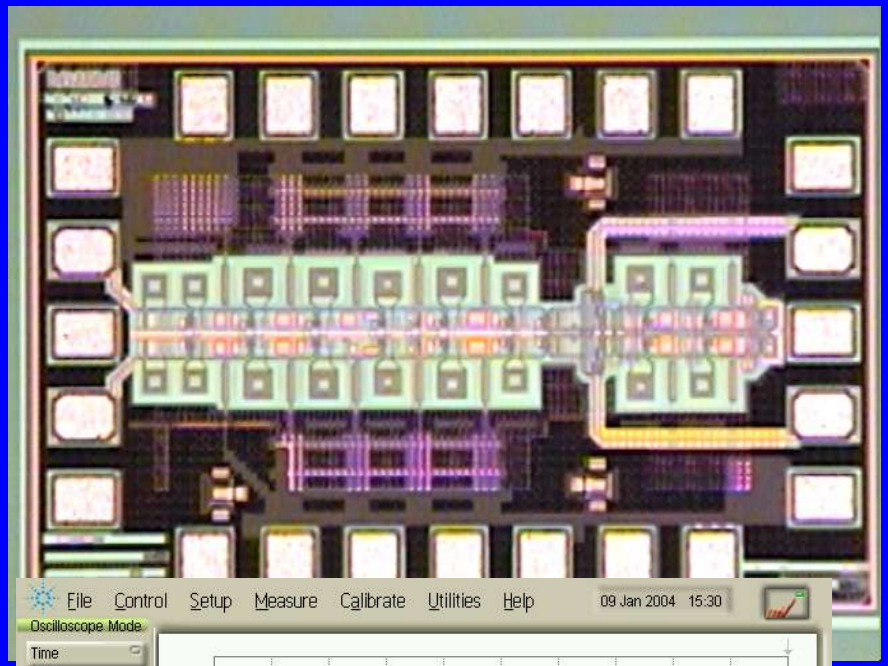




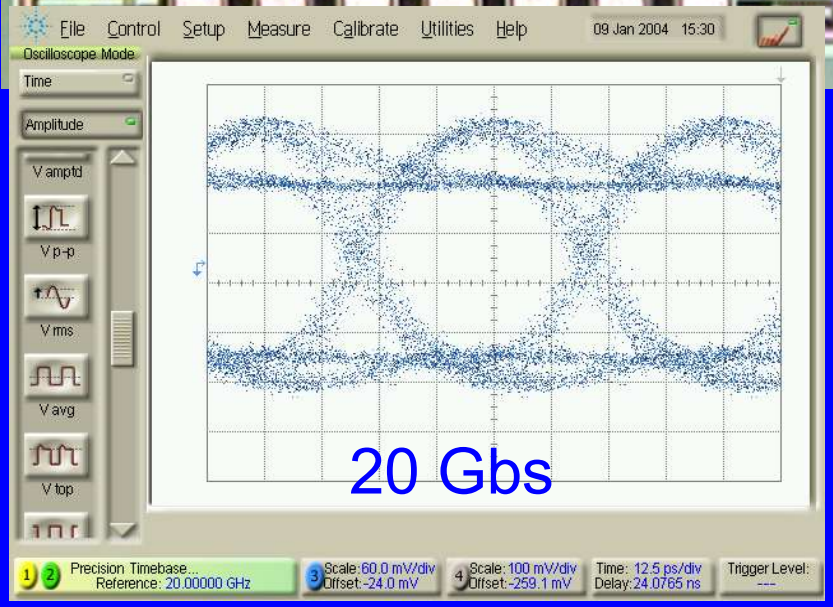
	NF at 10 Ghz	Data Rate	Sensitivity
CMOS	16.5 dB	20 Gb/s	20 mVpp
SiGe-HBT	10 dB	40 Gb/s	20 mVpp
InP-HBT	11.5 dB	40 Gb/s	8 mVpp

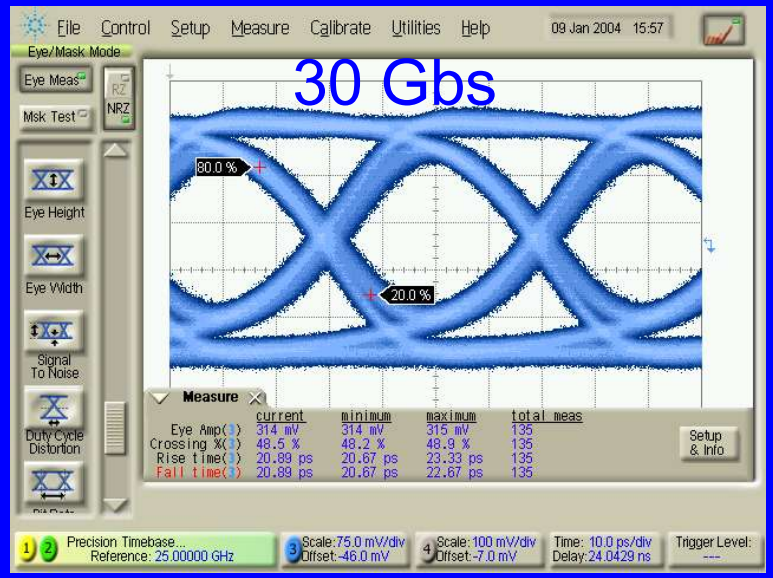
20/30 Gb/s, 1.5-V 130-nm CMOS Driver

(P. Westergaard et al. CICC-2004)



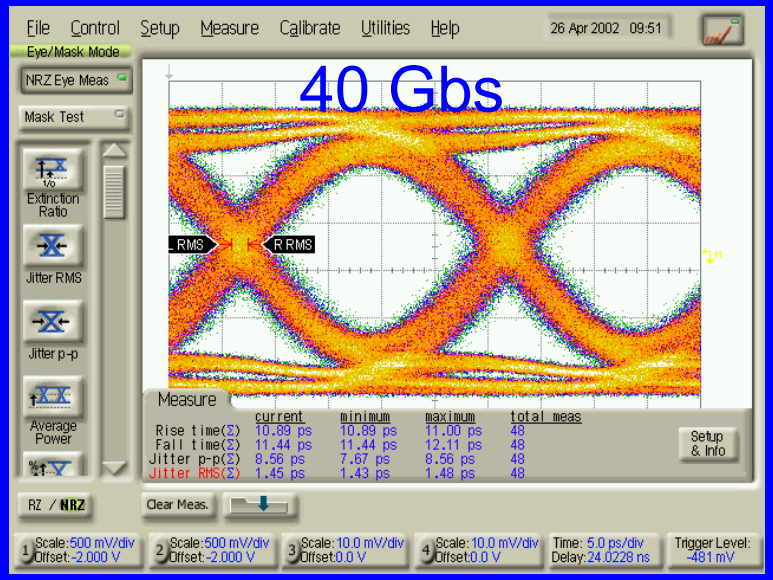
- Adjustable pre-emphasis
- Eye crossing: 40%-60%
- Output swing: $0.15V_{pp}$ to $0.35V_{pp}$
- Sensitivity: $20mV_{pp}$ @20Gb/s
- Dynamic range: 30 dB
- 1.5-V supply, 150 mW.
- 0.6 mm x 1 mm



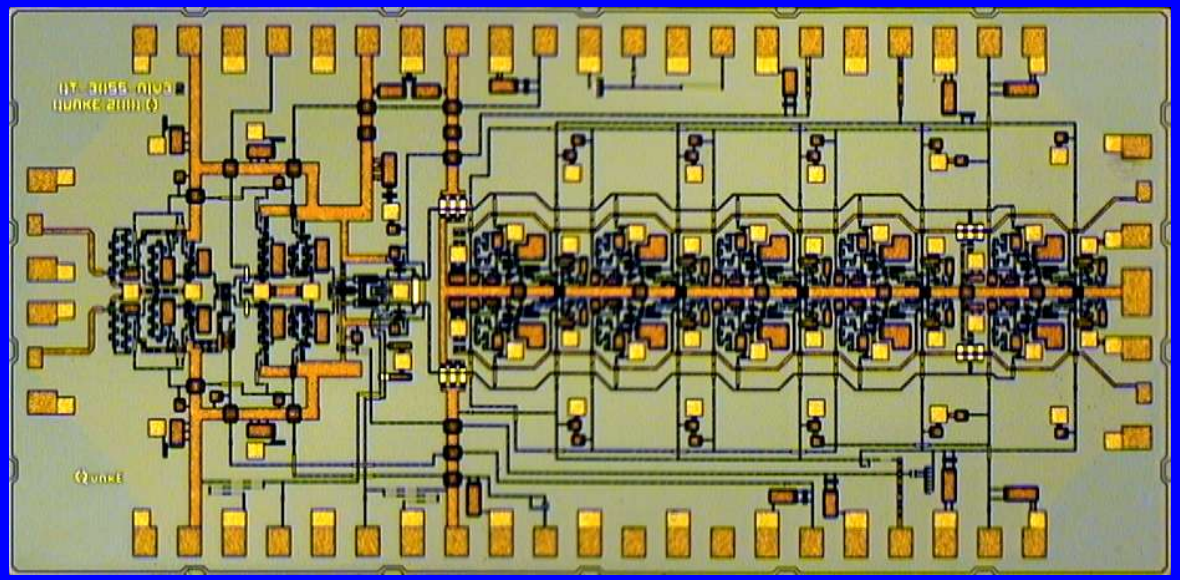


43 Gb/s,150-nm GaAs p-HEMT Driver

(D.McPherson et al. GaAs IC Symp. 2002)



- Adjustable DC offset
- Eye Crossing: 30%-70%
- Output swing: 1.7V_{pp} to 3V_{pp}
- Sensitivity: 600mV_{pp} @43Gb/s
- -5.2-V supply, 2.8 W.



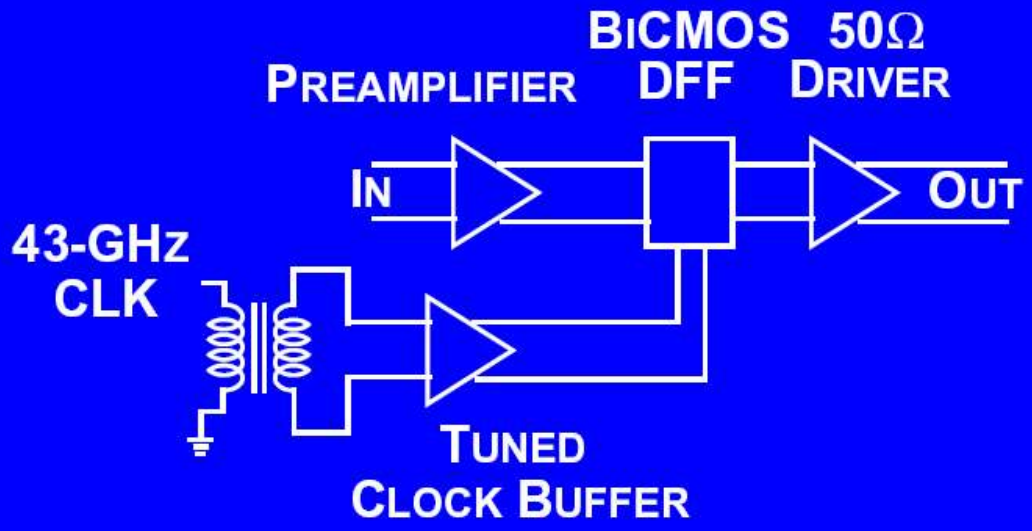
2 mm x 4 mm
1-metal + airbridge

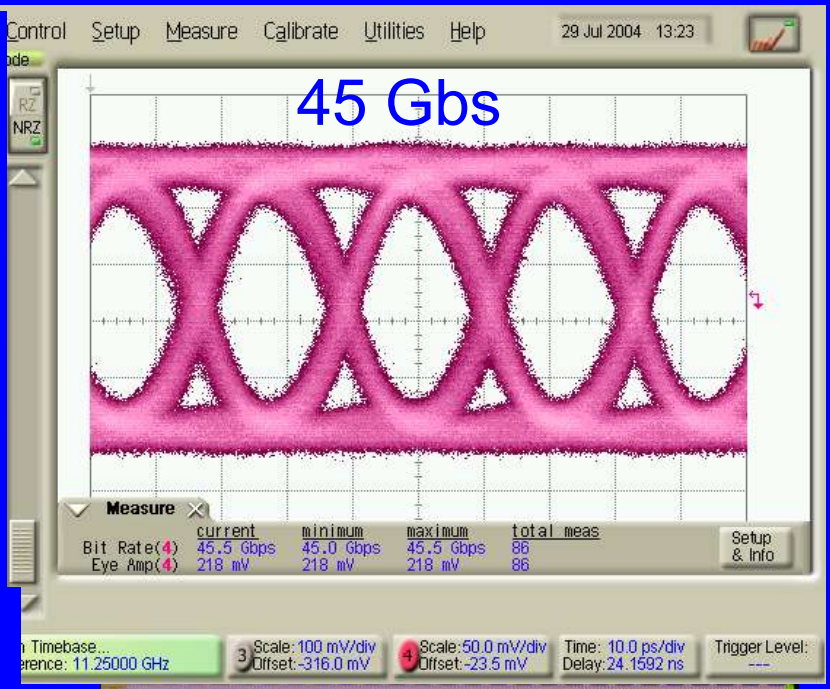
f_T=110 GHz

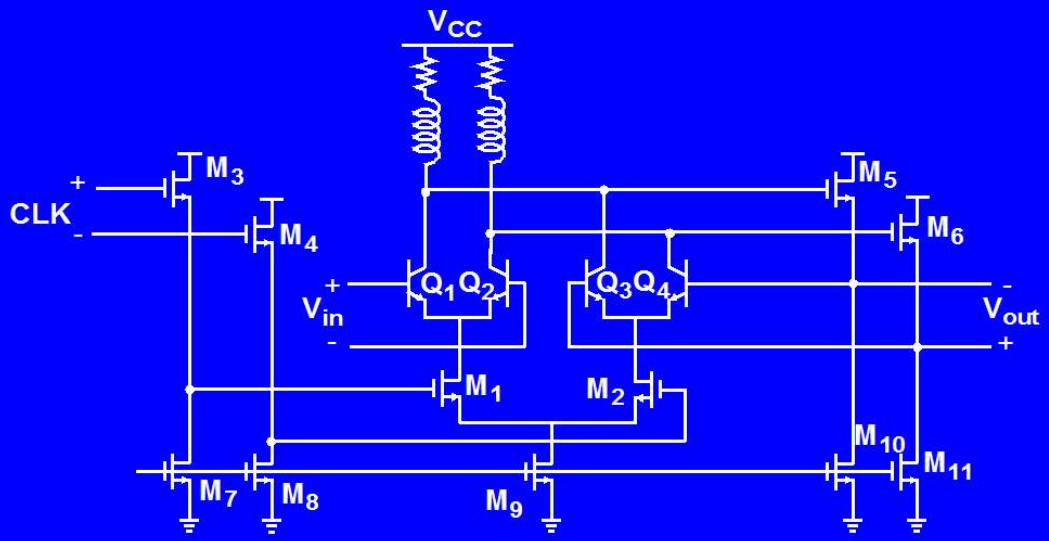
f_{MAX} = 180 GHz

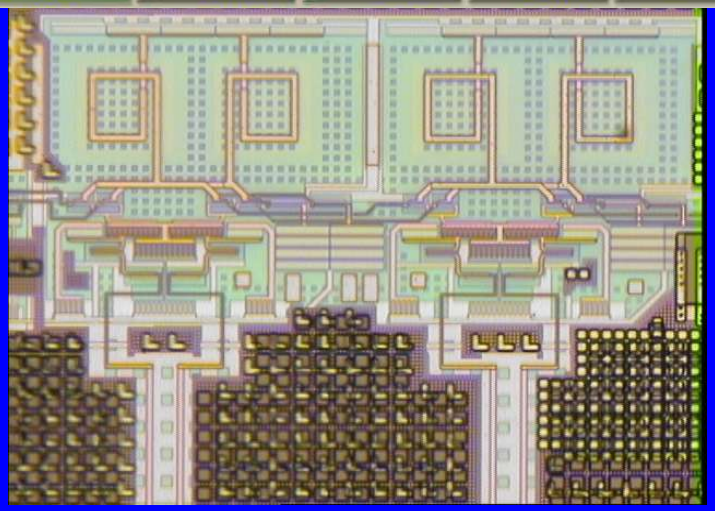
2.5-V, 58-mW, 45-GHz MS DFF

(T Dickson et al. VLSI Symp.-2004)

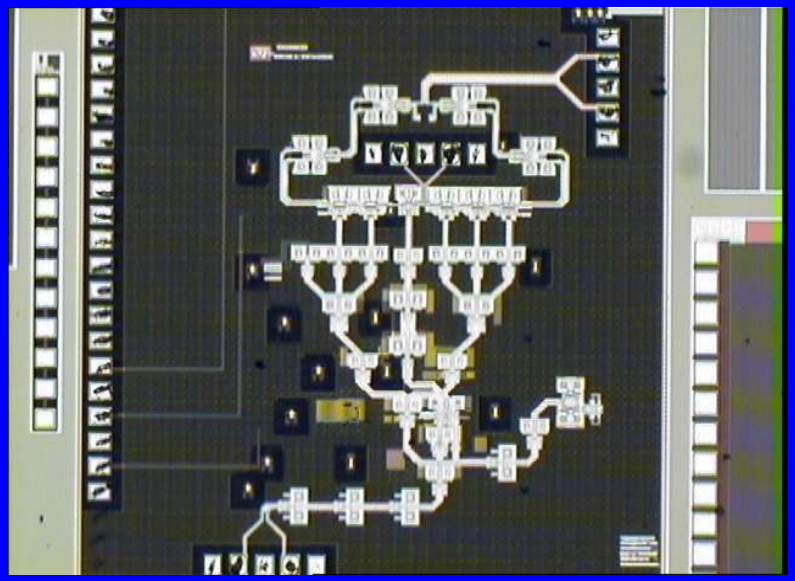


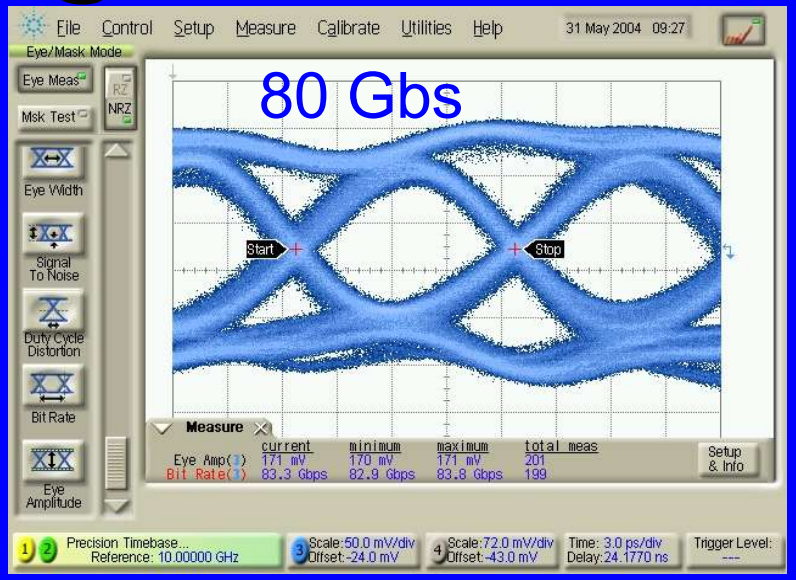






80-Gb/s 2:1 MUX in BiCMOS ECL Logic





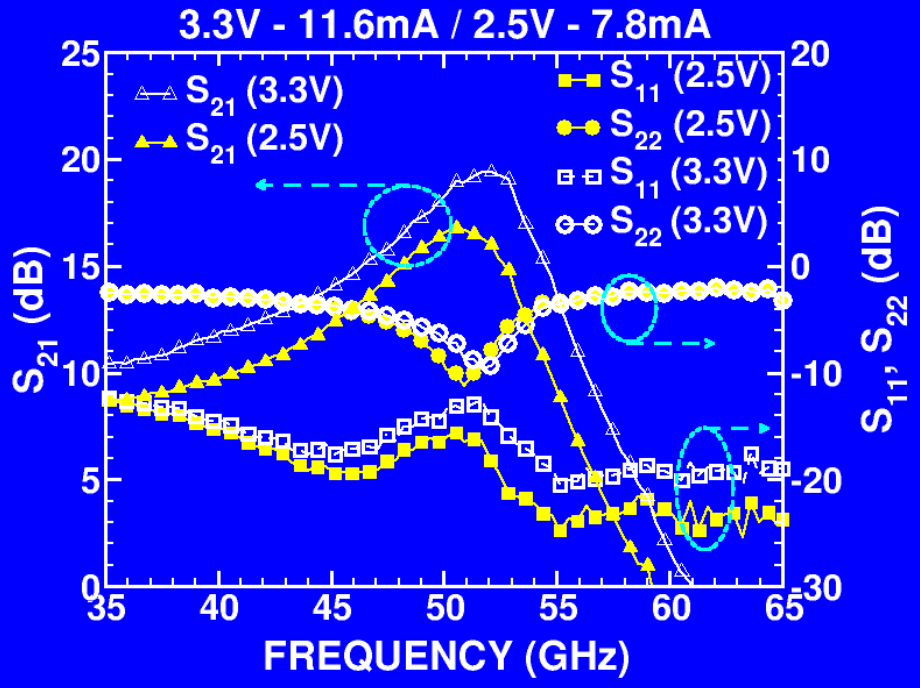
DFF	25 Ghz	60 Ghz?	60-GHz	80-GHz
2:1 MUX	60 Gbs	130 Gbs	110 Gb/s	144 Gbs
Div by 2		110 Ghz	150 Ghz	

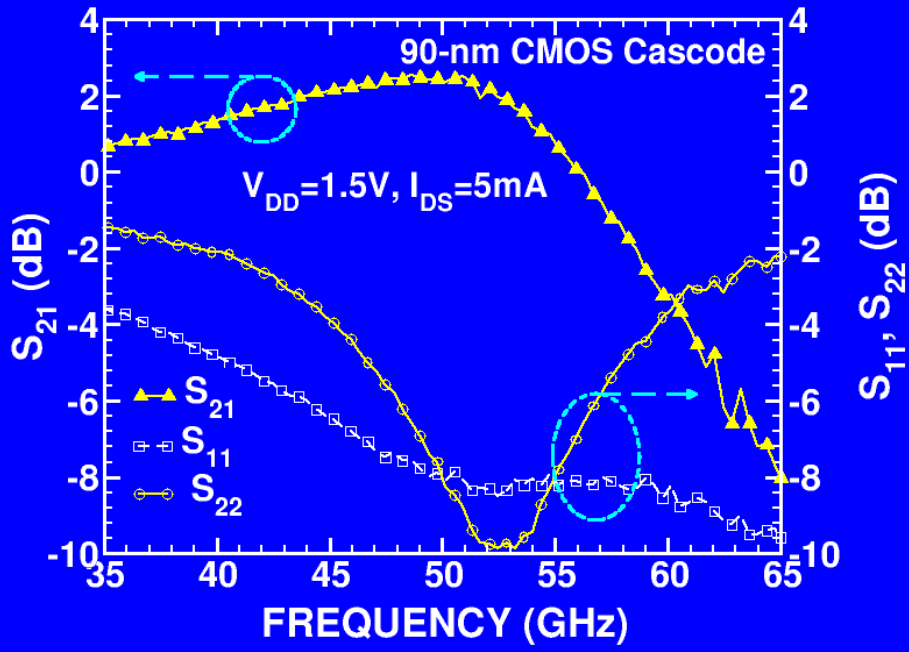
In the pipeline ...

60-GHz WLAN chipset

SiGe and CMOS LNAs @ 52 GHz

(M. Gordon and S.Voinigescu, ESSCIRC-2004)

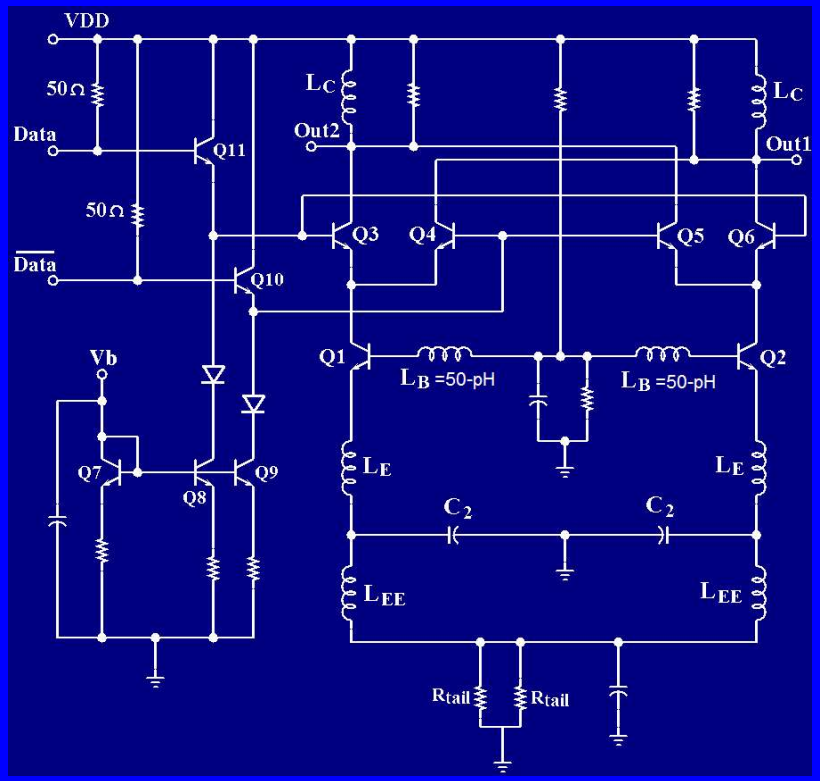


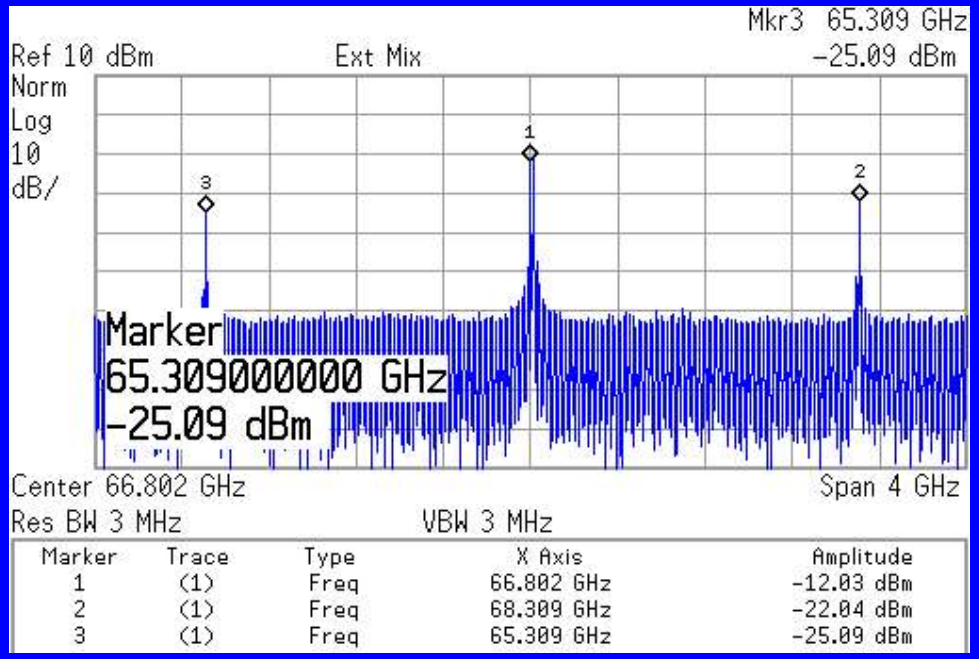


- SiGe HBT 2-stage cascode: 20-dB gain
- 90-nm MOS 1-stage cascode: 3-dB gain

SiGe HBT 65-GHz BPSK Transmitter

(C. Lee, T. Yao, et al, CSICS-2004)

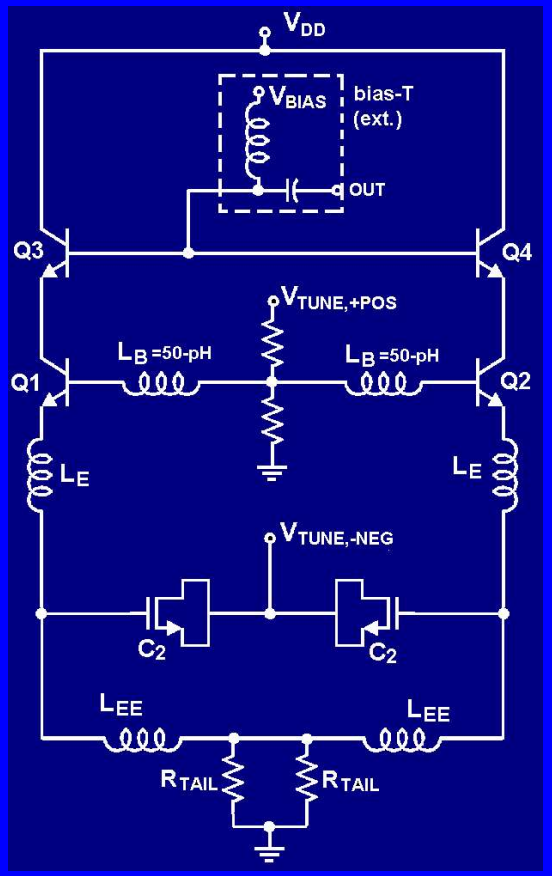


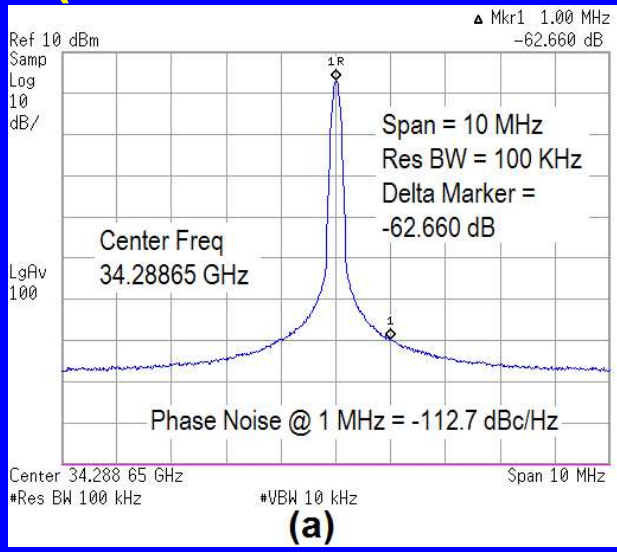


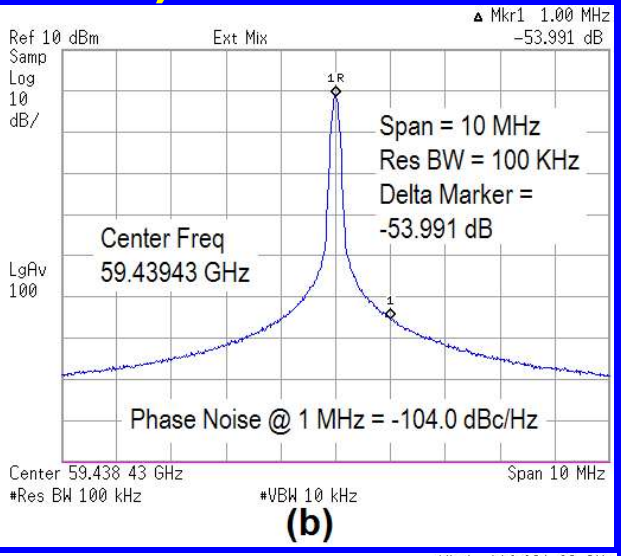
- VCO with built-in quad switch

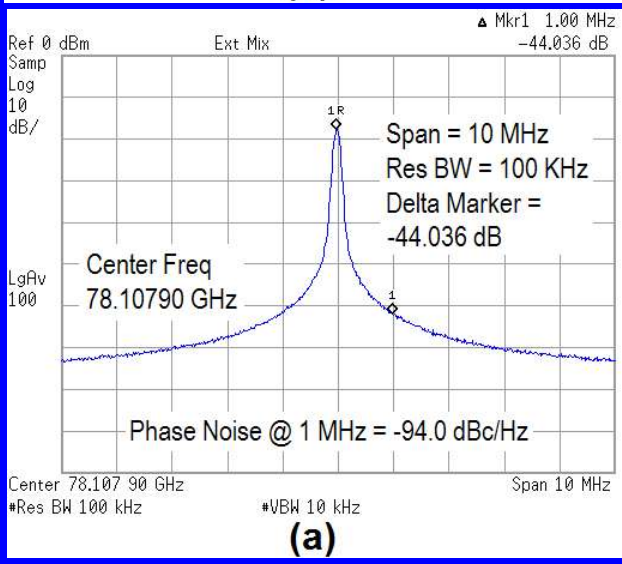
SiGe HBT VCOs to 120 GHz

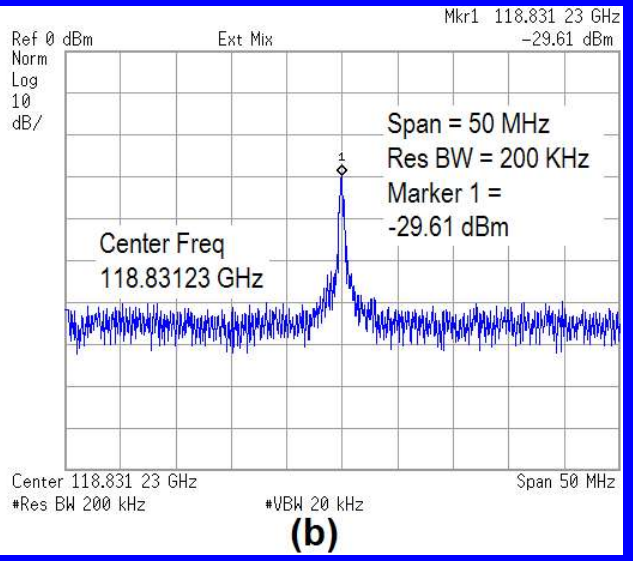
(C. Lee, et al CSICS-2004)











Conclusion

- Production 1μm InP HBT, 180-nm SiGe BiCMOS and 90-nm CMOS technologies adequate for most 50-80 GHz applications
- FETs should be biased at constant current density (0.3 mA/μm or 0.2 mA/μm)
- True BiCMOS topology ideal for tuned mm-wave and high-speed ICs
- Circuits in the 50-120 GHz range

Acknowledgments

- M. Gordon, A. Mangan, C. Lee, T. Yao, K. Yau
- M. LaCroix, B. Prokes, M. Tazlauanu, H. Tran, D. McPherson
- STMicroelectronics for fabrication
- Micronet, NSERC, Gennum Corporation and STMicroelectronics for financial support
- Quake Technologies for access to 40 Gb/s BERT, GaAs and InP data
- OIT and CFI for equipment grant
- CMC for CAD licenses

Backup

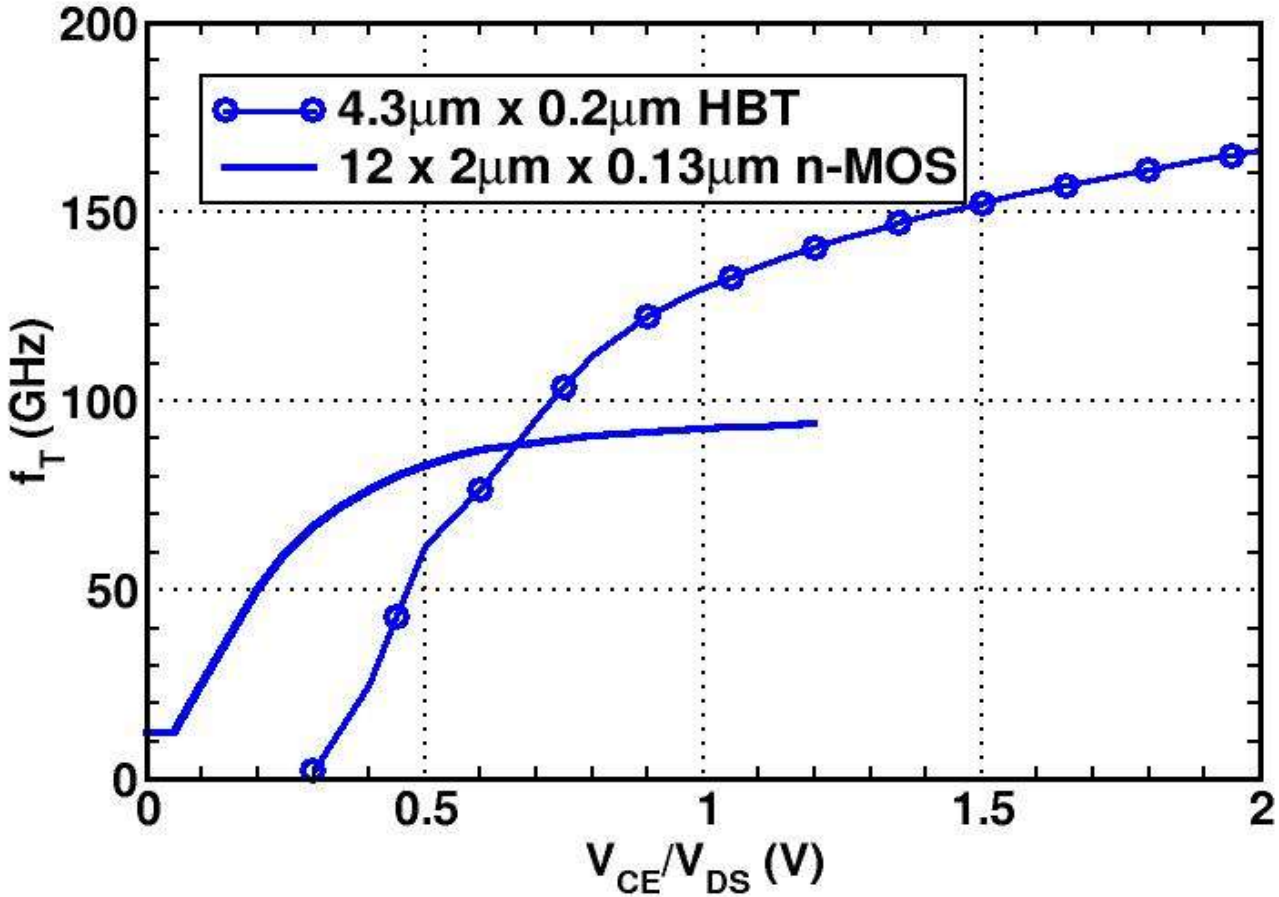
Cutoff Frequency

HBT: $$\frac{1}{2\pi f_T} = \tau_{EC}(I_C) = \tau_B + \tau_C + \frac{kT}{q I_C}(C_{je} + C_{cb}) + (R_e + R_c) C_{cb}$$

FET: $$\frac{1}{2\pi f_T} = \frac{(C_{gs} + C_{gd})}{g_m} + (R_s + R_d) C_{gd} + \left(\frac{C_{gs}}{1 + g_m R_s} + C_{gd} \right) R_d \frac{g_{ds}}{g_m}$$

$$\frac{1}{2\pi f_T} \approx \frac{\frac{2}{3} C_{ox} N_f W_f l_G + (CGDO + CGSO) N_f W_f + CGBO\, N_f l_G}{N_f C_{OX} \frac{W_f}{l_G} (V_{GS} - V_T)}$$

SiGe HBT & MOSFET V_{CE}/V_{DS}



f_{MAX}

HBT:

$$f_{MAX} \approx \sqrt{\frac{f_T}{8\pi R'_b C'_{cb}}}$$

FET:

$$f_{MAX} \approx \frac{f_T}{2\sqrt{\frac{R_{gsq} W_f^2}{12(3) l_G}(g'_{ds} + 2\pi f_T C'_{gd}) + g'_{ds}(R'_i + R'_s)}}$$

Best research results

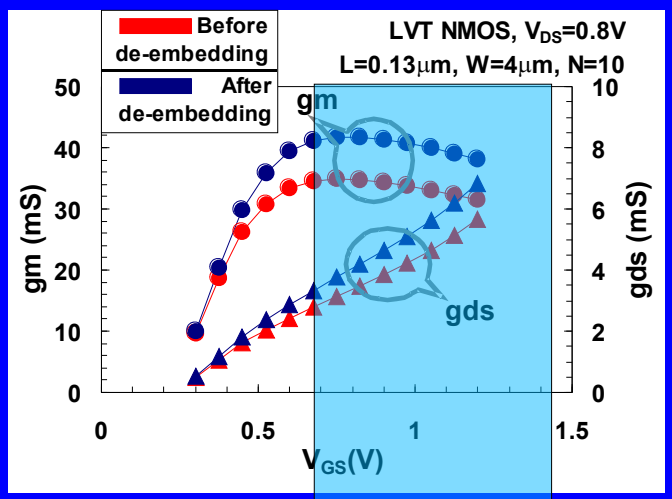
- 25-nm InP HEMT f_T/f_{MAX}: 562 GHz /330 GHz (Fujitsu, EDL 2002)
- 90-nm n-MOSFET f_T/f_{MAX}: 210(240) GHz / 250 (210) GHz (Intel, IBM, VLSI Tech. Symp. 2004)
- 0.6 μm InP HBT f_T/f_{MAX}: 420 GHz / 420 GHz (Rodwell, CSICS-2004)
- 120-nm SiGe HBT f_T/f_{MAX}: 300 GHz /300 GHz (IBM, IMS-2004)

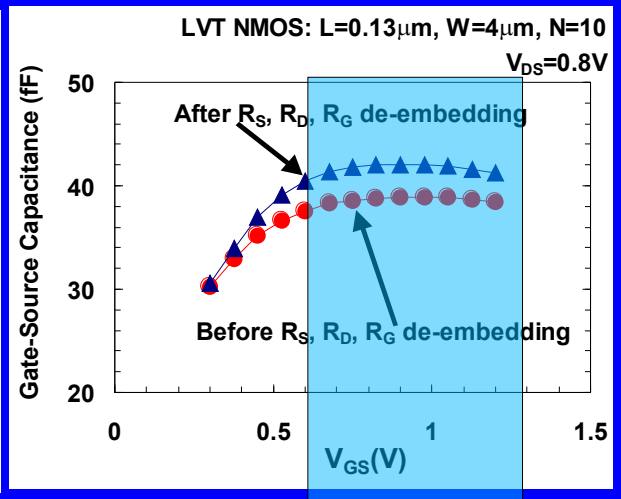
f_T, f_{MAX} summary

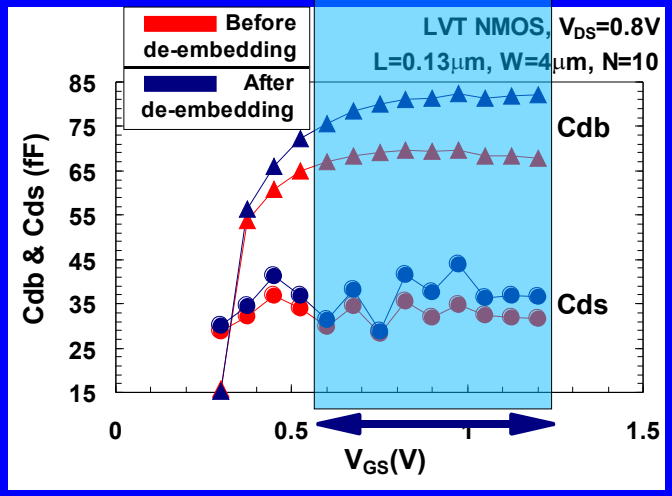
- III-V μ_n/v_{sat} advantage over Si offset by advanced lithography and processing
- HBT scaling leads to increased power density per A_E but constant per L_E
- MOSFET peak f_T/f_{MAX} current density is constant over technology nodes and foundries
  - 0.3 mA/μm for n-channel, and
  - 0.15 mA/μm for p-channel

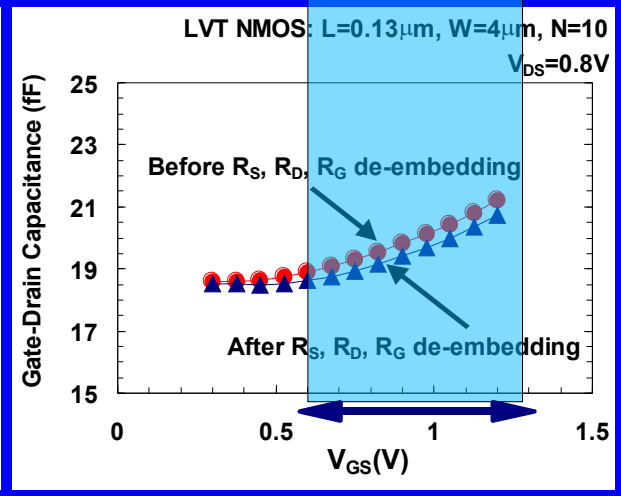
  and is de-coupled (i.e. <) from I_{ON}

MOSFET linearity: g_m, C









- Extracting capacitance from S-param meas. & de-embedding R_S, R_G, R_D critical to MOSFET model accuracy
- C_{GD}/C_{GS} = 0.45 (not captured by BSIM3/4)

Beyond peak f_T bias, g_m, C_{GS}, C_{GD}, C_{DB} are de-facto constant.

Voinigescu et al.,ICMTS-2004

F_{MIN}

$$F_{MIN(HBT)} \approx 1 + \frac{1}{\beta} + \frac{f}{f_T}\sqrt{\frac{I_C}{2V_T}(R_E + R_b)\left(1 + \frac{f_T^2}{\beta f^2}\right) + \frac{f_T^2}{4\beta f}}$$

$$F_{MIN(FET)} \approx 1 + 2k_1\frac{f}{f_T}\sqrt{g_m' R_s' + \frac{g_m' R_{gsq} W_f^2}{12(3)l_G} + k_2(1 + \omega^2 R_i^2 C_{gs}^2)}$$

$$F_{MIN(MOS)} \approx 1 + Const\frac{f}{\sqrt{g_m}} \approx 1 + Const\frac{f}{\sqrt{V_{GS} - V_T}}$$

Passives

Why inductors @mm-waves?

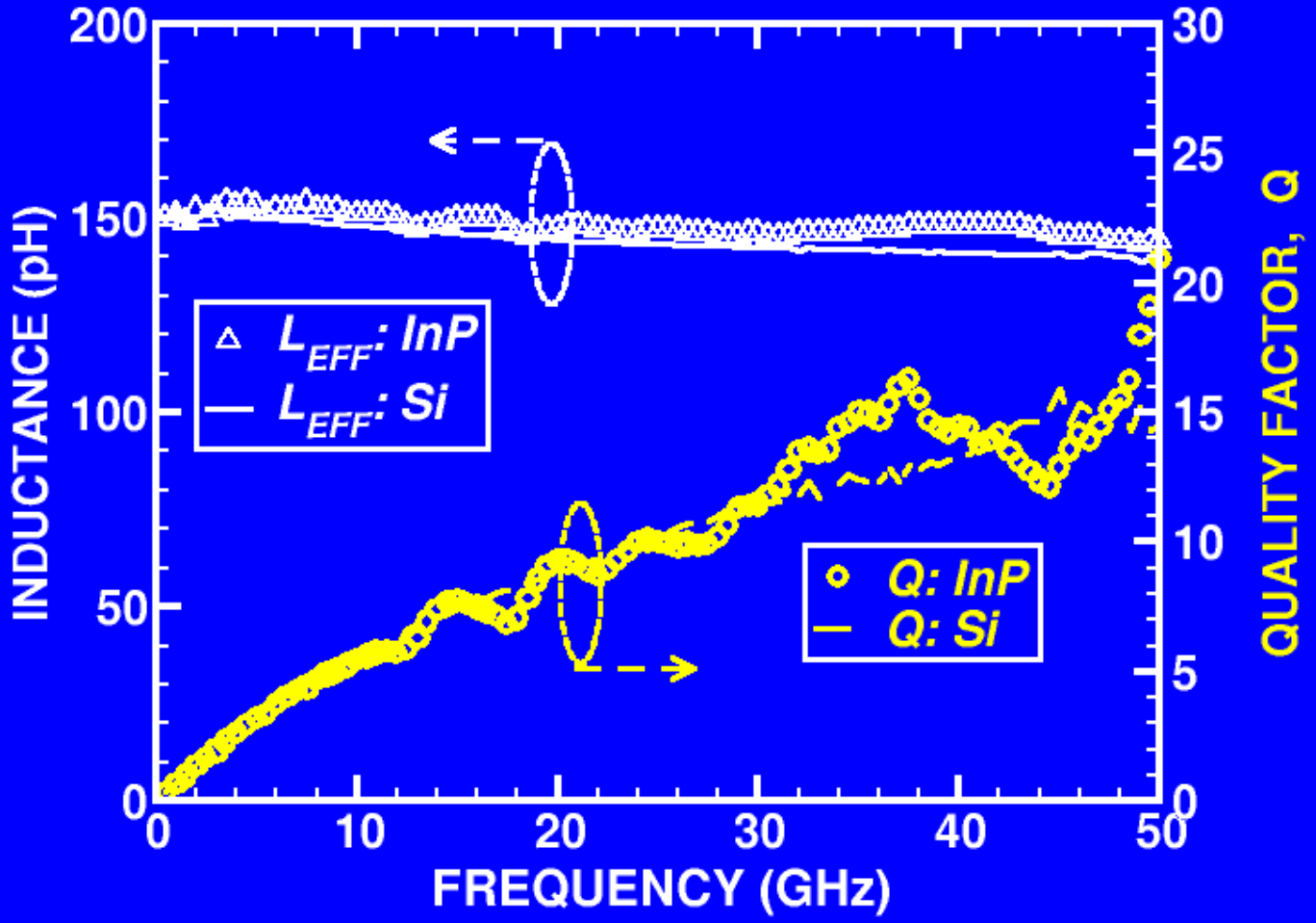
- Low-noise feedback and matching
- Shunt peaking increases bandwidth by >30% or reduces tail current by 30%

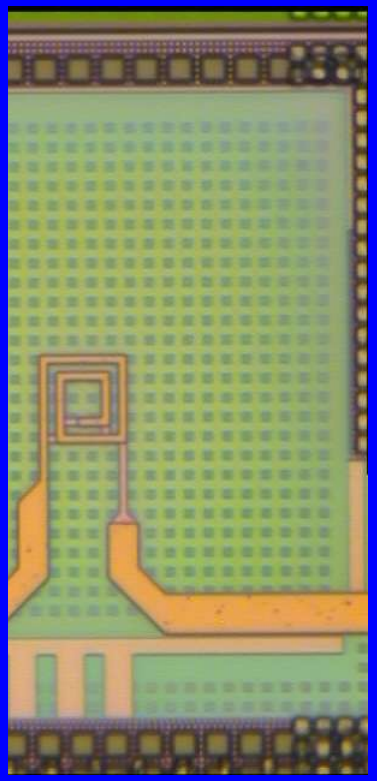
$$BW_{3dB} = \frac{1}{2\pi R_L C_L}; \quad L_p = \frac{C_L R_L^2}{3.1}; \quad R_L = \frac{\Delta V_{swing}}{I_{TAIL}}$$

- Higher Q and smaller footprint than at 2-10 GHz
- Significantly smaller area than t-lines

... but harder to measure & model

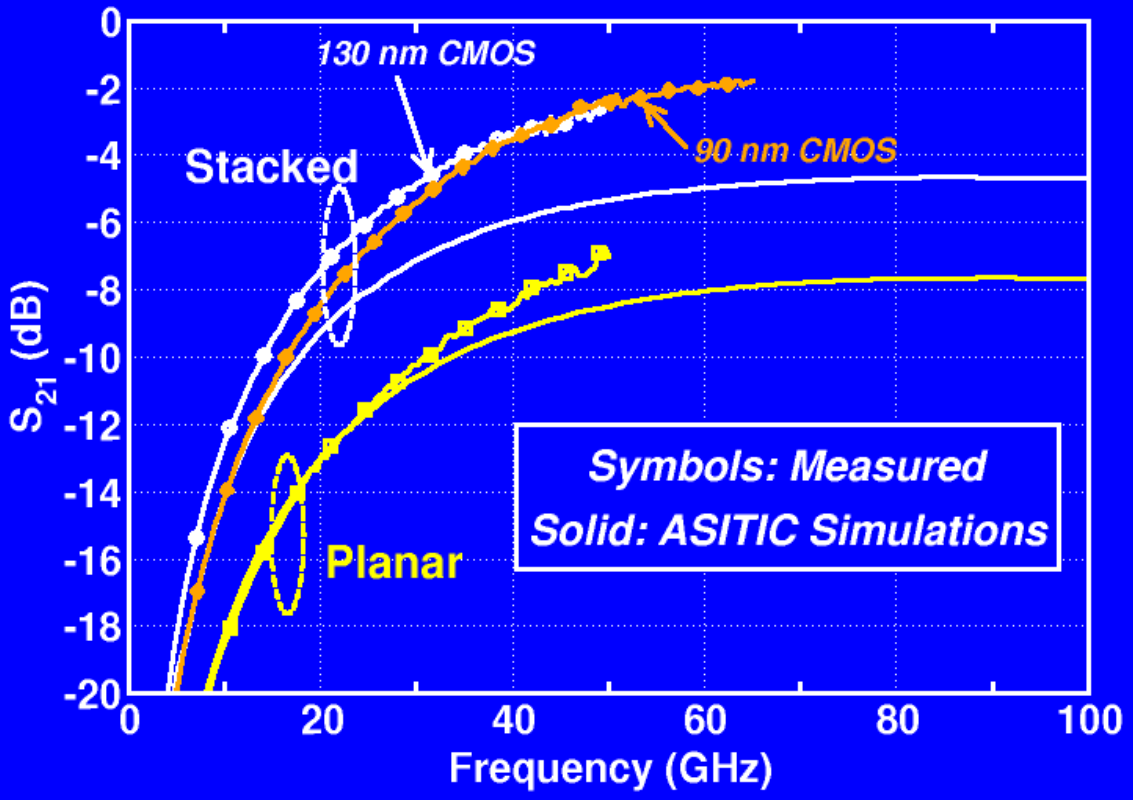
InP vs. Si inductors

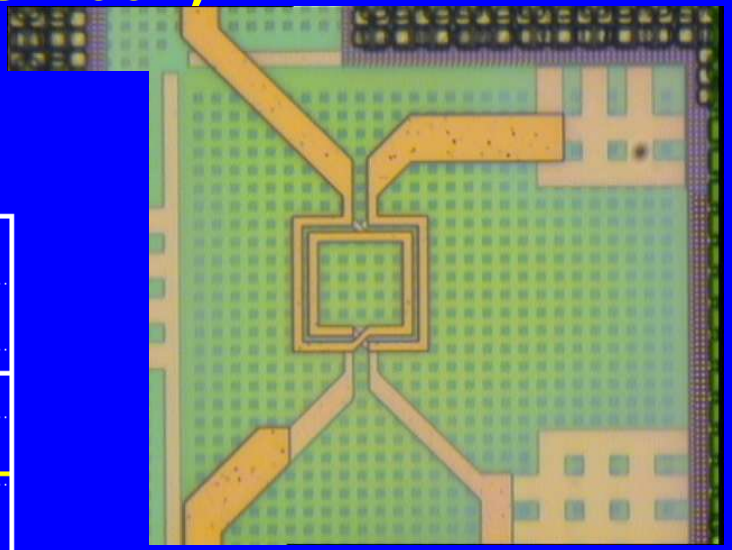


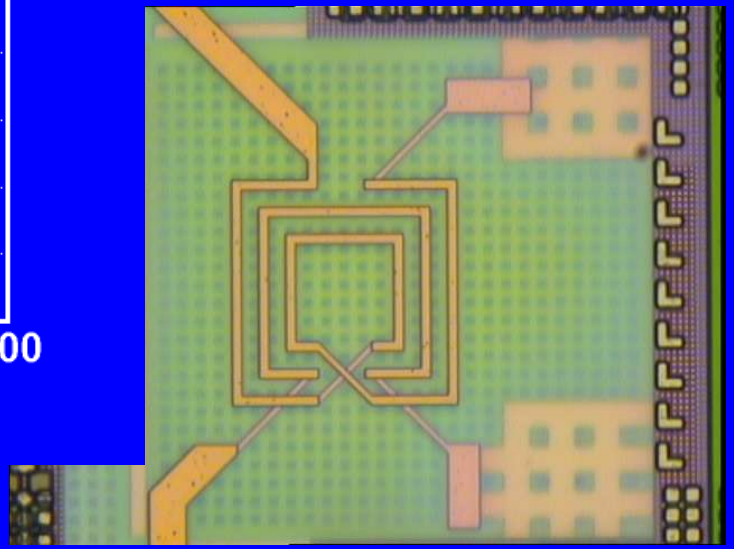


Si mm-wave transformers

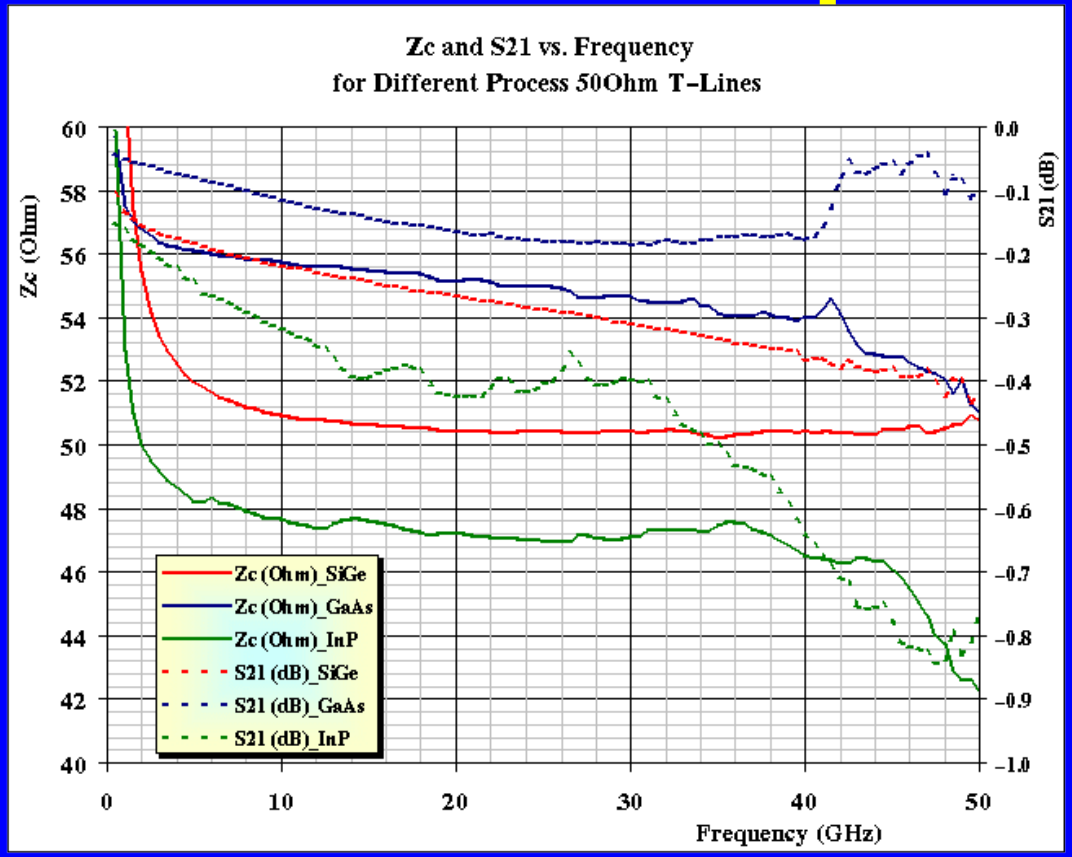
(T.Dickson et al, IMS-2004)



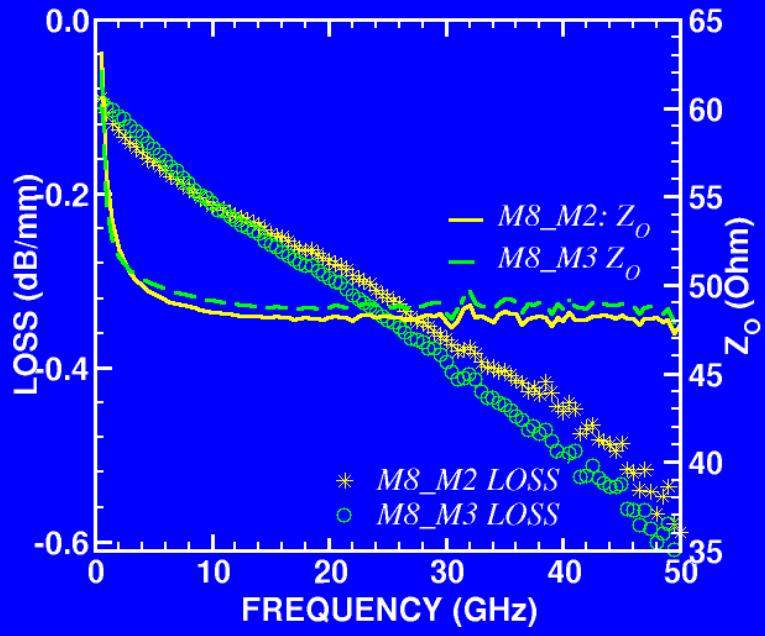




III-V vs. Si t-lines: similar performance



GaAs: 0.4 dB/mm @ 50 GHz
InP: 0.8 dB/mm @ 50 GHz
SiGe: 0.4 dB/mm @ 50 GHz

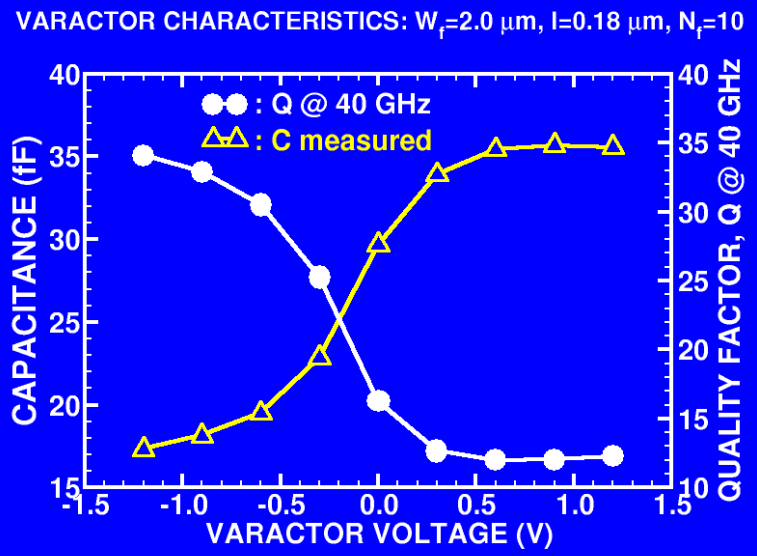


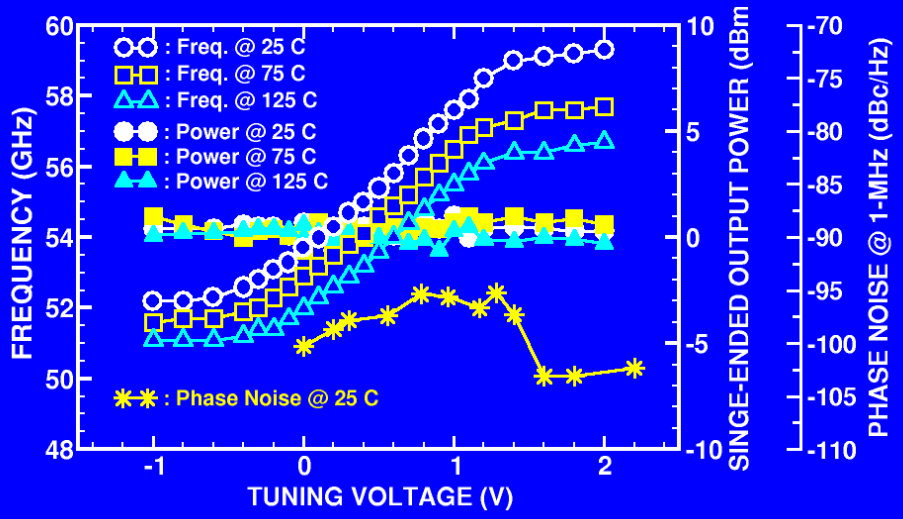
RF-CMOS: 0.6 dB/mm @ 50 GHz

Why AMOS vs. pn-junction varactors @ mm-waves?

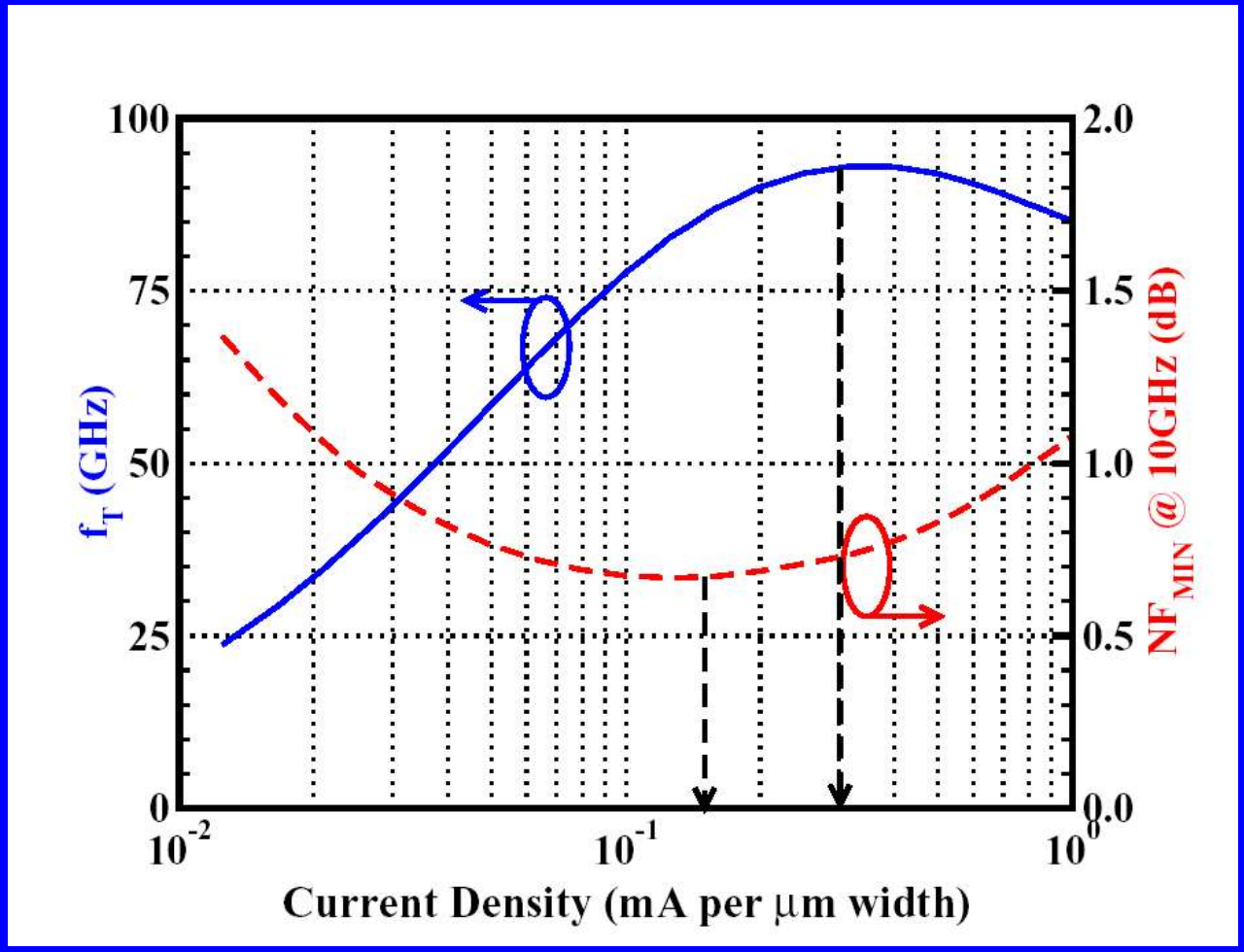
- Higher Q
- Larger cap. ratio
- Linear tuning curve
- Lower supply voltage

C. Lee et al. CSICS-2004





Biasing at I_{peakfT} (linearity), 0.5*I_{peakfT} (CML) and at optimum NF_{MIN} (LNA, VCO, MiXER)



n-MOSFET:

Peak f_T bias

0.3mA/μm

Min. NF_{MIN}

0.15mA/μm